Link Street® 88E6165

6 Port 10/100/1000 QoS Ethernet Switch with 5 Integrated Gigabit Ethernet PHYs

Datasheet Part 1 of 3: Overview, Pinout, Applications, Mechanical and Electrical Specifications

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Preface

About this Document

The 88E6165 Datasheet is a three-part set that includes the following documents:

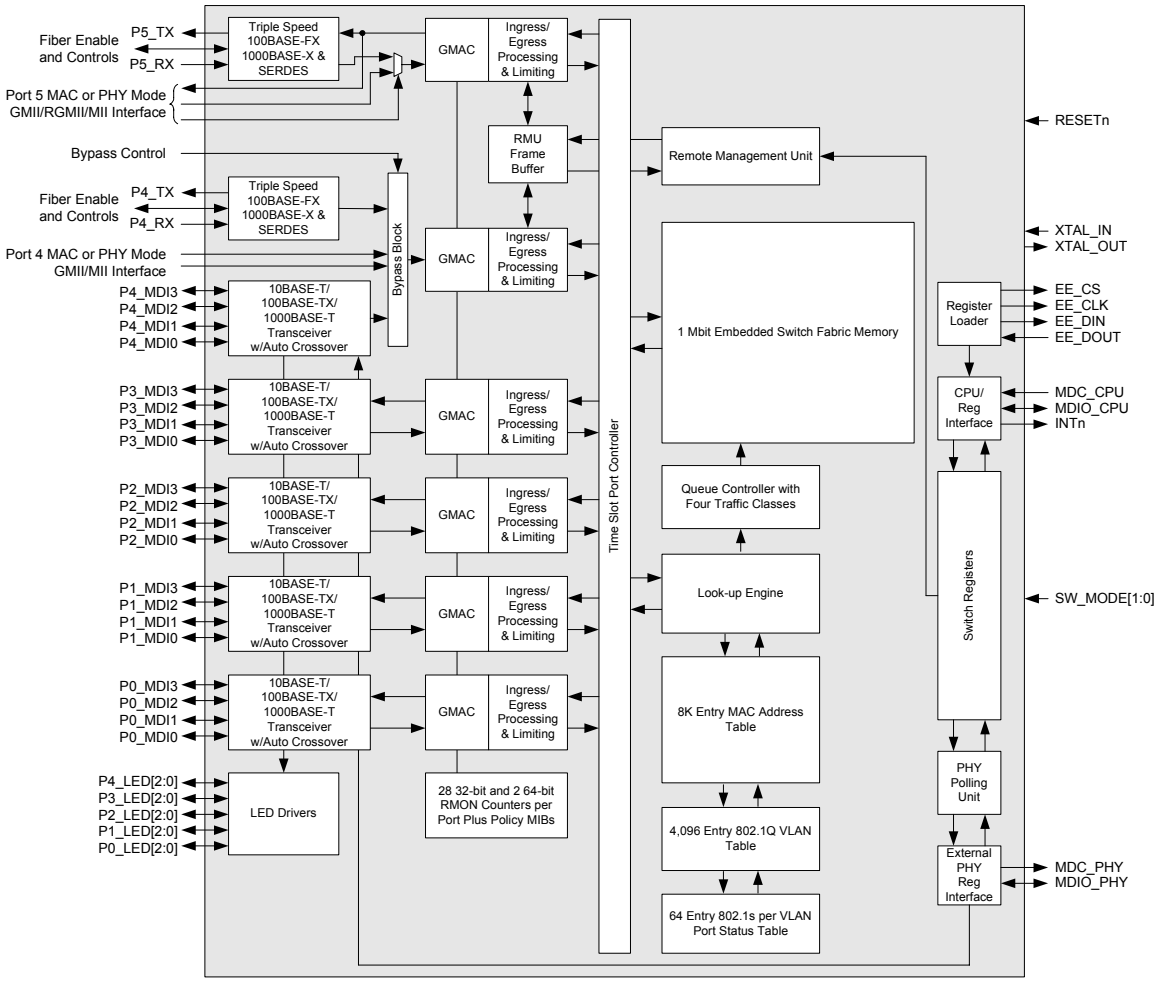
- **88E6165 Datasheet Part 1: Overview, Pinout, Applications, Mechanical and Electrical Specifications**
  Provides a feature list and overview describing the 88E6165. It also provides the pin description, pin map, mechanical drawings, and electrical specifications.

- **88E6165 Datasheet Part 2: Switch Core**
  Provides a description of the switch core of the 88E6165 and related register tables.

- **88E6165 Datasheet Part 3: Gigabit PHYs and SERDES**
  Provides a description of the Gigabit PHYs and SERDES of the 88E6165 and related register tables.

Figure 1 shows the overall block diagram for the 88E6165 device.

Figure 1: 88E6165 Block Diagram



OVERVIEW

The Marvell® 88E6165 device is a single-chip 6-port Gigabit Ethernet switch with five integrated Gigabit Ethernet transceivers. This device supports 'Best-in-Class' Quality of Service (QoS) and the highest 'real-world' performance. The device is uniquely suited for Small-to-Medium Business (SMB) and Access Switch applications.

This device contains five 10/100/1000 triple speed Ethernet transceivers (PHYs), two gigabit SERDES interfaces, and GMII interfaces. The 88E6165 device is designed to work in all environments. True Plug-and-Play is supported with Auto-Crossover, Auto-Negotiation, and Auto-Polarity in the PHYs, along with bridge loop prevention (using Port States).

The 88E6165 device includes a unique Switch Bypass mode to support router CPUs with 2 Gigabit MAC interfaces. This bypass mode provides a dedicated WAN interface that can connect to CPUs with GMII or SGMII interfaces.

The device contains six independent 802.3 media access controllers (MACs) supporting up to 10K byte JUMBO frames, a high-speed, non-blocking four traffic class QoS switch fabric that uses the unique Marvell Dynamic Queue Limit architecture. The QoS architecture switches packets into one of four traffic class queues based upon Port, IEEE 802.1p, IPv4 Type of Service (TOS) or Differentiated Services (Diff-Serv), IPv6 Traffic Class, 802.1Q VLAN ID, DA MAC address or SA MAC address. The device also contains a high-performance address lookup engine with support for up to 8K active nodes, and a 1 Mbit frame buffer memory. Back-pressure and pause frame-based flow control schemes are included to support zero packet loss under temporary traffic congestion. The MAC units in the devices comply fully with the applicable sections of IEEE 802.3.

The fifth and sixth ports' optional GMII interface supports a direct connection to Management or Router CPUs with integrated MACs. The sixth port also supports an RGMII interface that operates as a 1000 Mbps full-duplex port. These interfaces, along with BPDU handling for IEEE 802.1D Spanning Tree Protocol, 802.1w Rapid Spanning Tree, 802.1s Multiple VLAN Spanning Tree, programmable per-port VLAN configurations, 802.1Q and Port States, support fully managed switches and truly isolated WAN vs. LAN firewall applications. The device supports 4,096 802.1Q VLAN IDs which can be enabled on a per port basis. Three levels of 802.1Q security is supported with error frame trapping and logging.

The device supports multiple address databases (up to 4096), which allows packet routing without modification of the MAC address. This allows the same MAC address to exist multiple times in the MAC Address database with multiple port mappings, to completely isolate the WAN from the LAN database.

The PHY and SERDES units in the device are designed with the Marvell® cutting-edge mixed-signal processing technology for digital implementation of adaptive equalization and clock data recovery. The device integrates MDI interface termination resistors into the PHYs. This resistor integration facilitates board layout and reduces board cost by reducing the number of external components. Special power management techniques are used to facilitate low power dissipation and high port count integration. Both the PHY and MAC units in the devices comply fully with the applicable sections of IEEE 802.3, IEEE 802.3u, and IEEE 802.3x standards.

The PHYs also include an integrated Advanced Virtual Cable Tester® (VCT™) enabling fault detection and advanced cable performance monitoring.

The device's many operating modes can be configured using SMI (serial management interface - MDC/MDIO) or through in-band management via an Ethernet frame. The device also supports a standalone QoS mode or configuration via a low cost serial EEPROM.

The device is designed for cost-sensitive Gigabit Ethernet switch systems that require Quality of Service, Trunking, Stacking, and/or Spanning Tree.

APPLICATIONS

- Gigabit Ethernet firewall router with four 10/100/1000BASE-T LAN ports and one 10/100/1000 BASE-T WAN port
- Gigabit Ethernet firewall router with 100BASE-FX or 1000BASE-X fiber WAN port
- 5 port Gigabit Ethernet SMB Switch
- Multi-dwelling unit interface gateway
- Media converter for 100BASE-FX/1000BASE-X fiber to 10/100/1000BASE-T copper

HIGHLIGHTED FEATURES

- Supports up to 10K Byte Jumbo frames
- 'Best-in-Class' per port TCP/IP Ingress Rate Limiting along with independent Storm Prevention
- 5 Ingress Rate Limiting buckets per port, supporting Rate-based and Priority-based rate limiting
- Non-Rate Limited frames based on SA or DA
- Layer 2 Policy Control List (PCL) enables drop, trap, or mirroring based on SA, DA, VID, Ethertype, VBAS, PPPoE, UDP, and DHCP Option 82
- Remote Management capabilities allow device configuration and readback via Ethernet frames
- Per port, programmable MAC hardware address learn limiting
- Quality of Service support with four traffic classes
- QoS determined by Port, IEEE 802.1p tagged frames, IPv4's Type of Service (TOS) & Differentiated Services (DS), IPv6's Traffic Class 802.1Q VID, Destination MAC address, or Source MAC address
- Frame priority overrides based on SA, DA, or VID
- Queue priority overrides based on SA, DA, VID, ARP, or Snoop
- Strict, Weighted, or mixed mode QoS selectable per port
- Globally Programmable QoS weighting via a 128-entry table
- 802.1Q VLAN support for the full 4,096 VLAN IDs
- Supports multiple provider ports within a single chip via a programmable Ethertype per port
- Enhanced 802.1s Per VLAN Spanning Tree supporting up to 64 spanning tree instances
- Integrated MDI interface termination resistors
- Integrated Advanced Virtual Cable Tester® (VCT™) cable diagnostic feature

FEATURES

- Marvell® Header for increased Routing performance
- Shared 1 Mbit on-chip memory-based switch fabric with true non-blocking switching performance
- High performance lookup engine with support for up to 8K MAC address entries with automatic learning and aging
- Supports the Marvell Distributed Switching Architecture (DSA) for STP, up to 32 cascaded devices, and CPU-directed packet processing
- MAC SA based 802.1X authentication
- Port Trunking and Port Monitoring/Mirroring across chips
- Egress tagging/untagging selectable per port or by 802.1Q VLAN ID
- Port based VLANs supported in any combination across multiple chips
- Port States & BPDU handling for Spanning Tree
- 28 32-bit and 2 64-bit RMON Counters per port
- Ports 4 & 5 have independent triple speed SERDES transceivers to interface with Marvell® Alaska® gigabit copper PHYs and can optionally be configured as fiber ports (100BASE-FX or 1000BASE-X) with direct connection to lasers
- Ports 4 and 5 can support GMII Mode (full-duplex), MII-MAC Mode (Forward) or MII-PHY Mode (Reverse—full-duplex) interface options for management and firewall applications
- Port 5 supports an additional RGMII Mode
- Integrated with five independent Auto-Crossover Gigabit Ethernet transceivers fully compliant with the applicable sections of IEEE802.3 and IEEE802.3u
- Flexible LED support for Link, Speed, Duplex Mode, Collision, and Tx/Rx Activities
- Supports a low-cost 25 MHz XTAL clock source
- Supports 4-Wire 93C56/93C66 or 2-Wire 24C01/24C02/24C04 EEPROMs
- Single chip integration of an 6 port GE QoS switch and memory in a 24 x 24 mm 216-pin LQFP package
- Low power dissipation P_{AVE} = 2.5W

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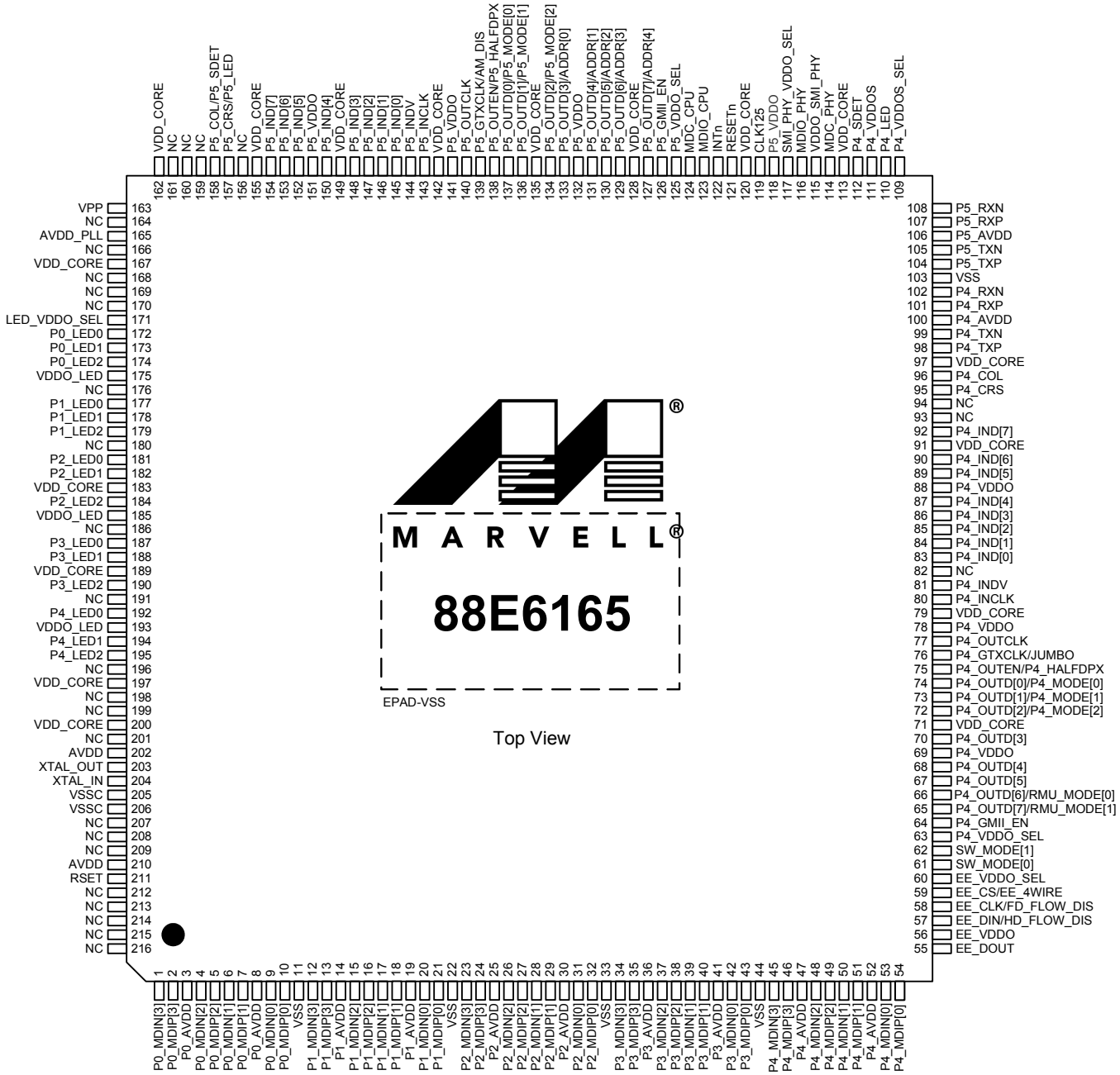
Figure 2: 88E6165 Device Pinout



Top View

1.1 Pin Description

1.1.1 Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability
Analog	Analog pin

Table 1: Network 10/100/1000 PHY Interface (Ports 0 to 4)

Pin #	Pin Name	Pin Type	Description
54 43 32 21 10 53 42 31 20 9	P4_MDIP[0] P3_MDIP[0] P2_MDIP[0] P1_MDIP[0] P0_MDIP[0] P4_MDIN[0] P3_MDIN[0] P2_MDIN[0] P1_MDIN[0] P0_MDIN[0]	I/O	Media Dependent Interface [0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] corresponds to BI_DA±. In MDIX configuration, MDIP/N[0] corresponds to BI_DB±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. MDIP/N[0] should be tied to VSS if not used.
51 40 29 18 7 50 39 28 17 6	P4_MDIP[1] P3_MDIP[1] P2_MDIP[1] P1_MDIP[1] P0_MDIP[1] P4_MDIN[1] P3_MDIN[1] P2_MDIN[1] P1_MDIN[1] P0_MDIN[1]	I/O	Media Dependent Interface [1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] corresponds to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T mode in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. MDIP/N[1] should be tied to VSS if not used.
49 38 27 16 5 48 37 26 15 4	P4_MDIP[2] P3_MDIP[2] P2_MDIP[2] P1_MDIP[2] P0_MDIP[2] P4_MDIN[2] P3_MDIN[2] P2_MDIN[2] P1_MDIN[2] P0_MDIN[2]	I/O	Media Dependent Interface [2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] corresponds to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. MDIP/N[2] should be tied to VSS if not used.
46 35 24 13 2 45 34 23 12 1	P4_MDIP[3] P3_MDIP[3] P2_MDIP[3] P1_MDIP[3] P0_MDIP[3] P4_MDIN[3] P3_MDIN[3] P2_MDIN[3] P1_MDIN[3] P0_MDIN[3]	I/O	Media Dependent Interface [3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] corresponds to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. MDIP/N[3] should be tied to VSS if not used.

Table 2: Port Status LEDs (Ports 0 to 4)

Pin #	Pin Name	Pin Type	Description
195 190 184 179 174	P4_LED2 P3_LED2 P2_LED2 P1_LED2 P0_LED2	O	Parallel LED outputs – one for each port. It can be configured to display many options as shown in “88E6165 Datasheet Part 3 of 3: Gigabit PHYs and SERDES”.
194 188 182 178 173	P4_LED1 P3_LED1 P2_LED1 P1_LED1 P0_LED1	O	Parallel LED outputs – one for each port. It can be configured to display many options as shown in “88E6165 Datasheet Part 3 of 3: Gigabit PHYs and SERDES”.
192 187 181 177 172	P4_LED0 P3_LED0 P2_LED0 P1_LED0 P0_LED0	O	Parallel LED outputs – one for each port. It can be configured to display many options as shown in “88E6165 Datasheet Part 3 of 3: Gigabit PHYs and SERDES”.

Table 3: SERDES/1000BASE-X/SGMII Interface (Port 4 and Port 5)

Pin #	Pin Name	Pin Type	Description
107 101	P5_RXP P4_RXP	I	Receiver input – Positive. Px_RXP connects directly to another device's TXP (Transmitter output – Positive) pins. These pins support 1000BASE-X, SGMII, or 100BASE-FX symbol codings.
108 102	P5_RXN P4_RXN	I	Receiver input – Negative. Px_RXN connects directly to another device's TXN (Transmitter output – Negative) pins. These pins support 1000BASE-X, SGMII, or 100BASE-FX symbol codings.
104 98	P5_TXP P4_TXP	O	Transmitter output – Positive. Px_TXP connects directly to another device's RXP (Receiver input – Positive) pins. These pins support 1000BASE-X, SGMII, or 100BASE-FX symbol codings.
105 99	P5_TXN P4_TXN	O	Transmitter output – Negative. Px_TXN connects directly to another device's RXN (Receiver input – Negative) pins. These pins support 1000BASE-X, SGMII, or 100BASE-FX symbol codings.
112	P4_SDET	I, PD	Port Signal Detect input when P4_MODE is configured to be either 101 or 111. If the port is configured to be in 1000BASE-X/100BASE-FX mode (using P4_MODE pins) P4_SDET indicates whether a signal is detected by the fiber-optic transceiver. A positive level indicates that a signal is detected. P4_SDET is internally pulled low via a resistor so the pin can be left floating when unused.
110	P4_LED		Port 4 SERDES LED Output. If the Port is configured for 1000BASE-X/100BASE-FX mode (using P4_MODE pins), P4_LED indicates whether a link signal is detected. A low output indicates that P4_SDET is active and the port's PCS has determined link. P4_LED indicates activity by blinking high when the port receives or transmits a frame. P4_LED is internally pulled low via a resistor so the pin can be left floating when unused.

Table 4: GMII/MII Interface Enable (Port 4)

Pin #	Pin Name	Pin Type	Description
64	P4_GMII_EN	I, PU	Port 4's GMII/MII interface. Leaving this pin unconnected will enable the drivers on Port 4's GMII interface pins, bring up link on Port 4 if the P4_MODE pins are set to either 000, 001, 010, or 011, and enables the GMII/MII interface to transmit and receive data if the port's PortState bits allow it. P4_GMII_EN is internally pulled high via a resistor. To disable Port 4's GMII/MII interface, this pin must be connected to VSS. P4_GMII_EN acts as Link status (Port register, offset 0x0) if Port 4's MAC is connected to the GMII/MII interface.

Table 5: GMII/MII Receive Interface (Port 4)

Pin #	Pin Name	Pin Type	Description
80	P4_INCLK	I, PD	Input Clock. INCLK is a reference for INDV and IND[7:0]. The speed of INCLK is expected to be 125 MHz, 50 MHz, 25 MHz, or 2.5 MHz depending upon the speed of the port. INCLK is internally pulled low so the pin can be left unconnected if not used.
92 90 89 87 86 85 84 83	P4_IND[7] P4_IND[6] P4_IND[5] P4_IND[4] P4_IND[3] P4_IND[2] P4_IND[1] P4_IND[0]	I, PD	Input Data. IND[7:0] receives the data octet or nibble to be sent into the switch. IND[7:0] must be synchronous to INCLK. In 1000BASE GMII mode, IND[7:0] is used. In 200BASE, 100BASE, and 10BASE modes IND[3:0] is used and IND[7:4] is ignored. IND[7:0] are internally pulled low via resistor so the pins can be left unconnected when they are not used.
81	P4_INDV	I, PD	Input Data Valid. Input Data Valid is used to indicate when IND[7:0] (or IND[3:0] where appropriate) contains frame information. INDV must be synchronous to INCLK. INDV is internally pulled low via resistor so the pin can be left unconnected when it is not used.
95	P4_CRS	I/O, PD	Carrier Sense.Carrier sense is used to indicate carrier has been detected on the line. CRS is not synchronous to INCLK. CRS is used for half-duplex modes only and is ignored when the port is in full-duplex. This pin becomes an output if the P4_MODE pins are set to either 100, 101, 110, or 111. This pin is internally pulled low via resistor so the pin can be left unconnected when it is not used.
96	P4_COL	I/O, PD	Collision. Collision is used to indicate both transmit and receive are occurring at the same time in half-duplex mode. P4_COL is not synchronous to INCLK. P4_COL is used for half-duplex modes only and is ignored when the port is in full-duplex. If the P4_MODE bits are set to either 000, 001, 010, 011, or 100, then this pin indicates the P4_COL if the port is in half-duplex mode. This pin becomes an output if the P4_MODE pins are set to either 100, 101, 110, or 111. This pin is internally pulled low via resistor so the pin can be left unconnected when it is not used.

Table 6: GMII/MII Transmit Interface (Port 4)

Pin #	Pin Name	Pin Type	Description
76	P4_GTXCLK/ JUMBO	O, PU	Transmit Clock. GTXCLK is a reference for OUTEN and OUTD[7:0] when the port is in GMII mode. The speed of GTXCLK is 125 MHz and is normally only driven when the speed of the port is 1000 Mbps. GTX-CLK can be configured to output a 25 MHz or a 2.5 MHz clock so it can be used as a clock source for P4_OUTCLK and P4_INCLK when no other clock sources are available (see P4_MODE[2:0]). GTXCLK is tri-stated during RESETn when P4_GMII_EN is low. GTX-CLK is internally pulled high so the pin can be left unconnected if not used. This pin is a multi-function pin with Jumbo mode setting as the other function. JUMBO: Global JumboMode bit determines the maximum frame size (i.e., MTU) allowed to be received or transmitted from or to any of the 6 ports supported in this device. 0 = It indicates that the JumboMode (receive and transmit 10,240 Byte frames) is disabled for all ports on the device (max frame size is 1522 bytes). 1 = It indicates that the JumboMode (receive and transmit 10,240 Byte frames) is enabled for all ports on the device. The value of this pin is captured on the rising edge of RESETn. The captured value gets transferred into the Port Control 2 Register (Port, Offset 0x08). If this pin is tied low, the register bits get a value of 0x0 and if this pin is tied high, the register bits get a value of 0x2. **NOTE:** The per-port register bits defined in Port Control 2 Register (Offset 0x08, bits[13:12]) are still valid. If the device is attached to either a EEPROM or a CPU, then it provides flexibility to override the above setting by writing into the Port Control 2 Register (Port, Offset 0x08).
77	P4_OUTCLK	I/O, PU	Output Clock. OUTCLK is an input clock reference for OUTEN and OUTD[3:0] when the port is in MII mode. The speed of OUTCLK is 50 MHz, 25 MHz, or 2.5 MHz depending on the speed of the port. This pin becomes an output if the P4_MODE[2:0] pins are set to either 100, 101, or 111; otherwise, it is an input. P4_OUTCLK is tri-stated during RESETn when P4_GMII_EN is low. P4_OUTCLK is internally pulled high so the pin can be left uncon-nected if not used.

Table 6: GMII/MII Transmit Interface (Port 4) (Continued)

Pin #	Pin Name	Pin Type	Description
65 66 67 68 70 72 73 74	P4_OUTD[7] / RMU_MODE[1] P4_OUTD[6] / RMU_MODE[0] P4_OUTD[5] / LED_MODE P4_OUTD[4] P4_OUTD[3] P4_OUTD[2] / P4_MODE[2] P4_OUTD[1] / P4_MODE[1] P4_OUTD[0] / P4_MODE[0]	Typically O	Output Data. OUTD[7:0] outputs the data octet to be transmitted from the switch. OUTD[7:0] is synchronous to GTXCLK in 1000 Mbps mode. In 200BASE, 100BASE, and 10BASE modes, OUTD[3:0] is synchronous to OUTCLK and OUTD[7:4] is ignored. P4_OUTD[7:0] are multi-function pins used to configure the devices during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn: OUTD[7:6] = RMU_MODE[1:0] OUTD[5] = LED_MODE OUTD[2:0] = P4_MODE[2:0] RMU_MODE[1:0]: 00 = RMU feature is disabled. 01 = Port 4 is enabled to be the RMU (Remote Management Unit) port for the switch. 10 = Port 5 is enabled to be the RMU port for the switch. 11 = Reserved The reset value of the RMU_MODE pins are captured in Global Control 2 register (Port, Offset 0x1C).

Table 6: GMII/MII Transmit Interface (Port 4) (Continued)

Pin #	Pin Name	Pin Type	Description
(Cont. from above)	(Cont. from above)	Typically O	LED_MODE: 0 = Select LED mode 0 for the GPHY LED operation. Refer to "88E6165 Datasheet Part 3 Gigabit PHYs and SERDES" for further details. 1 = Select LED mode 3 for the GPHY LED operation. Refer to "88E6165 Datasheet Part 3 Gigabit PHYs and SERDES" for further details. P4_MODE[2:0] definition: 000 = Port 4 of the switch core is configured to be connected to the GMII interface pins. P4_GTXCLK = 125 MHz (1000BASE) Port 4's GPHY is connected to Port 4's SGMII interface pins directly. 001 = Reserved 010 = Port 4 of the Switch core is configured to be connected to the MII 100 interface pins P4_GTXCLK = 25 MHz Port 4's GPHY is connected to Port 4's SGMII interface pins directly. 011 = Port 4 of the Switch core is configured to be connected to the MII 10 interface pins. P4_GTXCLK = 2.5 MHz Port 4's GPHY is connected to Port 4's SGMII interface pins directly. 100 = Port 4 of the switch core is configured to be in PHY mode using the internal GPHY. Port 4's GMII interface is connected to the Port 4's SGMII interface pins directly. 101 = Port 4 of the switch core is configured to be connected to the 1000BASE X interface pins. Port 4's GPHY is connected to Port 4's GMII interface pins directly. 110 = Port 4 of the Switch core is configured to be connected to the SGMII/MGMII mode interface pins. Port 4's GPHY is connected to Port 4's GMII interface pins directly. 111 = Port 4 of the Switch core is configured to be connected to the 100BASE-FX mode interface pins. Port 4's GPHY is connected to Port 4's GMII interface pins directly.

Table 6: GMII/MII Transmit Interface (Port 4) (Continued)

Pin #	Pin Name	Pin Type	Description
(Cont. from above)	(Cont. from above)	Typically O	Note that when the P4_MODE is either set to 101 or 110 or 111, the GMII/MII OUT pins are internally connected to the GPHY's IN pins and GMII/MII IN pins are internally connected to the GPHY's OUT pins. Note that in the above described bypass modes, if the Port 4's internal PHY is not connected to the switch core, then the internal Port 4's PHY can be addressed using an SMI device address of 0x6. Any external PHY that gets connected to either the GMII or the SERDES interface on Port 4 must be addressed using the SMI device address of 0x4 so the PPU will work. P4_OUTD[7:0] are tri-stated during RESETn when P4_GMII_EN is low. P4_OUTD[7:3] are internally pulled low via resistor so the pins can be left unconnected when they are not used. P4_OUTD[2:0] are internally set to 100 using internal resistors. Use a 4.7 kohm resistor to VDDO for a configuration high.
75	P4_OUTEN / P4_HALFDPX	Typically O, PD	Output Enable. Output enable is used to indicate when OUTD[7:0] (or OUTD[3:0] where appropriate) contains frame information. OUTEN is synchronous to GTXCLK in 1000BASE mode and its synchronous to OUTCLK in 100BASE and 10BASE modes. P4_OUTEN is a multi-function pin used to configure the devices during a hardware reset. When reset is asserted, this pin becomes an input and the configuration information below is latched at the rising edge of RESETn: 0 = Sets P4 in full-duplex operation 1 = Sets P4 in half-duplex operation OUTEN is tri-stated during RESETn when P4_GMII_EN is low. OUTEN is internally pulled low via resistor so the pin can be left unconnected to select full-duplex on Port 4 or when it is not used.

Table 7: GMII/RGMII/MII Interface Enable (Port 5)

Pin #	Pin Name	Pin Type	Description
126	P5_GMII_EN	I, PD	Port 5's GMII interface enable. Setting this pin high will enable the output drivers on Port 5's GMII interface pins, brings link up on Port 5 when P5_MODE[2:0] pins are set to either 000, 001, 010, or 011 and enable the GMII/RGMII/MII interface to transmit and receive data if the port's PortState bits allow it. When this pin is low, Port 5's GMII output pins will be disabled (i.e., they are tri-stated). P5_GMII_EN is internally pulled high so the pin can be left unconnected to enable Port 5's GMII/RGMII/MII interface. P5_GMII_EN acts as Link status (Port, Offset 0x0) if the Port 5 is connected to the GMII/RGMII/MII interface.

Table 8: GMII/RGMII/MII Receive Interface (Port 5)

Pin #	Pin Name	Pin Type	Description
143	P5_INCLK	I, PD	Input Clock. INCLK is a reference for INDV, IN_ER, and IND[7:0]. The speed of INCLK is expected to be 125 MHz, 50 MHz, 25 MHz, or 2.5 MHz depending upon the speed of the port. In RGMII mode INCLK is used as RXC. INCLK is internally pulled low so the pin can be left unconnected if not used.
154 153 152 150 148 147 146 145	P5_IND[7] P5_IND[6] P5_IND[5] P5_IND[4] P5_IND[3] P5_IND[2] P5_IND[1] P5_IND[0]	I, PD	Input Data. IND[7:0] receives the data octet or nibble to be sent into the switch. IND[7:0] must be synchronous to INCLK. In 1000BASE GMII mode, IND[7:0] is used. In 1000BASE RGMII mode, 200BASE, 100BASE, and 10BASE modes IND[3:0] is used and IND[7:4] is ignored. In RGMII mode IND[3:0] are used as RXD[3:0]. IND[7:0] are internally pulled low via resistor so the pins can be left unconnected when they are not used.
144	P5_INDV	I, PD	Input Data Valid. Input Data Valid is used to indicate when IND[7:0] (or IND[3:0] where appropriate) contains frame information. RXDV must be synchronous to INCLK. In RGMII mode INDV is used as RX_CTL. INDV is internally pulled low via resistor so the pin can be left unconnected when it is not used.
157	P5_CRS/P5_LED	I, PD	This is a multi-function pin indicating either the port carrier sense information or the port 5's LED information. When P5_MODE[2:0] are set to either 000, 001, 010, or 011 then this pin is P5_CRS and it is an input. Carrier Sense. Carrier sense is used to indicate carrier has been detected on the line. P5_CRS is not synchronous to INCLK. P5_CRS is used for half-duplex modes only and is ignored when the port is in full-duplex. When P5_MODE[2:0] are set to either 100, 101, 110, or 111 then this pin is P5_LED and it is an output. P5_LED indicates the Link Activity information for the Port 5's SERDES core. This pin is internally pulled low via resistor so the pin can be left unconnected when it is not used.

Table 8: GMII/RGMII/MII Receive Interface (Port 5) (Continued)

Pin #	Pin Name	Pin Type	Description
158	P5_COL/ P5_SDET	I, PD	This is a multi-function pin indicating either the port collision information or the port signal detect information. If P5_MODE pins are set to either 000, 001, 010, 011, or 100, then this pin indicates the P5_COL if the port is operating in half-duplex mode. Collision is used to indicate both transmit and receive are occurring at the same time in half-duplex mode. P5_COL is not synchronous to INCLK. P5_COL is used for half-duplex modes only and is ignored when the port is in full-duplex. If the P4_MODE pins are set to either 101 or 111 then this pin indicates the P4_SDET i.e., Port Signal Detect input. If the port is configured for 1000BASE-X/100BASE-FX mode, P4_SDET indicates whether a signal is detected by the fiber-optic transceiver. A positive level indicates that a signal is detected unless this phase is inverted (see Global 2, Offset 0x1D). This pin is internally pulled low via resistor so the pin can be left unconnected when it is not used.

Table 9: GMII/RGMII/MII Transmit Interface (Port 5)

Pin #	Pin Name	Pin Type	Description
119	CLK125	O	125 MHz Clock. CLK125 is a free running 125 MHz clock that is asynchronous from GTXCLK if GTXCLK is running at 125 MHz. CLK125 will always be 125 MHz even if GTXCLK is disabled or at some other frequency. CLK125 is free running during RESETn and after RESETn.
139	P5_GTXCLK/ AM_DIS	O, PU	Transmit Clock. GTXCLK is a reference for OUTEN and OUTD[7:0] when the port is in GMII mode or RGMII mode. The speed of GTXCLK is 125 MHz and is normally only driven when the speed of the port is 1000 Mbps. GTXCLK can be configured to output a 25 MHz or a 2.5 MHz clock so it can be used as a clock source for P5_OUTCLK and P5_INCLK when no other clock sources are available (see P5_MODE). In RGMII mode GTXCLK is used as TXC. GTXCLK is tri-stated during RESETn when P5_GMII_EN is low. GTXCLK is internally pulled high so the pin can be left unconnected if not used. P5_GTXCLK is a multi-function pin used to configure the device during a hardware reset. When reset is asserted, this pin becomes an input and the configuration information below is latched at the rising edge of RESETn: 0 = Marvell® Auto-Media Detect capable PHYs are attached through a SERDES interface and the Auto-Media Detect function is to be enabled in the PPU 1 = Marvell Auto-Media Detect capable PHYs are not attached, or they are attached but the Auto-Media Detect function is to be disabled in the PPU
140	P5_OUTCLK	I/O, PU	Output Clock. OUTCLK is an input clock reference for OUTEN and OUTD[3:0] when the port is in MII mode. The speed of OUTCLK is 50 MHz, 25 MHz, or 2.5 MHz depending the speed of the port. P5_OUTCLK is tri-stated during RESETn when P5_GMII_EN is low. P5_OUTCLK is internally pulled high so the pin can be left unconnected if not used.

Table 9: GMII/RGMII/MII Transmit Interface (Port 5) (Continued)

Pin #	Pin Name	Pin Type	Description
127 129 130 131 133 134 136 137	P5_OUTD[7] / ADDR[4] P5_OUTD[6] / ADDR[3] P5_OUTD[5] / ADDR[2] P5_OUTD[4] / ADDR[1] P5_OUTD[3] / ADDR[0] P5_OUTD[2] / P5_MODE[2] P5_OUTD[1] / P5_MODE[1] P5_OUTD[0] / P5_MODE[0]	Typical O	Output Data. OUTD[7:0] outputs the data octet to be transmitted from the switch when the port is in 1000BASE mode, but OUTD[7:4] are not used in RGMII mode. OUTD[7:0] is synchronous to GTXCLK in 1000BASE mode. In 200BASE, 100BASE, and 10BASE modes, OUTD[3:0] is synchronous to OUTCLK and OUTD[7:4] is ignored. In RGMII mode OUTD[3:0] are used as TXD[3:0]. P5_OUTD[7:0] are multi-function pins used to configure the devices during a hardware reset. When reset is asserted, these pins become inputs and the configuration information below is latched at the rising edge of RESETn: OUTD[7:3] = ADDR[4:0] OUTD[2:0] = P5_MODE[2:0] ADDR[4:0] sets the device's SMI address and its addressing mode as well as the devices initial DeviceNumber. If ADDR[4:0] are all 0's the device is configured in single device addressing mode. P5_MODE[2:0] definition: 000 = Port 5 is configured to be in GMII mode P5_GTXCLK = 125 MHz (1000Base) 001 = Port 5 is configured to be in RGMII mode (1000 Mbps, full-duplex only) 010 = Port 5 is configured to be in MII 100, P5_GTXCLK = 25 MHz 011 = Port 5 is configured to be in MII 10, P5_GTXCLK = 2.5 MHz 100 = Reserved 101 = Port 5 is configured to be in 1000BASE-X mode 110 = Port 5 is configured to be in SGMII mode 111 = Port 5 is configured to be in 100BASE-FX mode P5_OUTD[7:0] are tri-stated during RESETn when P5_GMII_EN is low. P5_OUTD[7:0] are internally pulled low via resistor so the pins can be left unconnected when they are not used. Use a 4.7 kohm resistor to VDDO for a configuration high.

Table 9: GMII/RGMII/MII Transmit Interface (Port 5) (Continued)

Pin #	Pin Name	Pin Type	Description
138	P5_OUTEN/ P5_HALFDPX	Typically O, PD	Output Enable. Output enable is used to indicate when OUTD[7:0] (or OUTD[3:0] where appropriate) contains frame information. OUTEN is synchronous to GTXCLK in 1000BASE mode and its synchronous to OUTCLK in 100BASE and 10BASE modes. In RGMII mode OUTEN is used as TX_CTL. P5_OUTEN is a multi-function pin used to configure the devices during a hardware reset. When reset is asserted, this pin becomes an input and the configuration information below is latched at the rising edge of RESETn: 0 = Sets P5 in full-duplex operation 1 = Sets P5 in half-duplex operation OUTEN is tri-stated during RESETn when P5_GMII_EN is low. OUTEN is internally pulled low via resistor so the pin can be left unconnected to select full-duplex on Port 5 or when it is not used.

Table 10: Regulators and Reference

Pin #	Pin Name	Pin Type	Description
211	RSET	Analog	Resistor Current reference. A 5 kohm 1% resistor is placed between the RSET and VSS. This resistor is used to set an internal bias reference current.

Table 11: System

Pin #	Pin Name	Pin Type	Description
204	XTAL_IN	I	25 MHz system reference clock input provided from the board. The clock source can come from an external crystal or an external oscillator. This is the only clock required. Refer to "Clock Timing" on page 73 for timing requirements.
203	XTAL_OUT	O	System reference clock output provided to the board. This output can only be used to drive an external crystal. It cannot be used to drive external logic. If an external oscillator is used this pin should be left unconnected.
122	INTn	D	INTn is an active low, open drain pin that is asserted to indicate an unmasked interrupt event occurred. A single external pull-up resistor is required somewhere on this interrupt net for it to go high when it is inactive. The INTn pin will go active low if SW_MODE[1:0] (Table 14) is not 0b10 (test mode) and if the EEPROM data has executed a Halt OpCode.
121	RESETn	I	Hardware reset. Active low. The 88E6165 device is configured during reset. When RESETn is low all configuration pins become inputs and the value seen on these pins is latched on the rising edge of RESETn or some time after. Refer to Section 3.6.1 "Receiver AC Characteristics" on page 72 for Reset and Configuration Timing details.

Table 12: Register Access Interface

Pin #	Pin Name	Pin Type	Description
114	MDC_PHY	Typically O, PU	Management Data Clock, Master. MDC_PHY is the reference clock output for the serial management interface (SMI) that connects to an external SMI slave device, typically external PHYs. The Master SMI is used to access the registers in any external PHYs and it's path to the external PHYs is available to the CPU to use (via the MDC_CPU & MDIO_CPU pins). MDC_PHY is a multi-function pin used to configure the 88E6165 device during a hardware reset. When reset is asserted, MDC_PHY becomes an input and configuration information is latched into the device. At the rising edge of RESETn MDC_PHY is internally pulled high via a resistor so it can be left floating when unused. **NOTE:** On previous devices, this pin functioned as a PPU_EN configuration pin. While this pin still performs this function, it is now recommended that the PPU always remain enabled and then access the PHY registers using the SMI PHY Command and Data registers (Global 2, offsets 0x18 and 0x19). The PPUState bits (Global 1, offset 0x00) and the PPUEn bit (Global 1, offset 0x04) exist in this device but are marked as Reserved, or they are modified, as these bits are not expected to be used as they were in the previous devices. The PPUEn and PPUState bits will physically be changed in future devices to match this documentation.
116	MDIO_PHY	I/O, PU	Management Data I/O, Master. MDIO_PHY is used to transfer management data in and out of the device synchronously to MDC_PHY. This pin requires an external pull-up resistor in the range of 4.7 kohm to 10 kohm. The 88E6165 device uses Device Addresses 0x03 to 0x07 to access the external PHYs for ports 3 to 7 respectively. The CPU can read or write any register on any device connected to this MDC_PHY/ MDIO_PHY interface - see the SMI PHY Command and Data registers (Global 2, offsets 0x18 and 0x19) MDIO_PHY is internally pulled high via a resistor so it can be left floating when unused.

Table 12: Register Access Interface (Continued)

Pin #	Pin Name	Pin Type	Description
124	MDC_CPU	I, PU	Management Data Clock, Slave. MDC_CPU is the reference clock input for the serial management interface (SMI) that connects to an external SMI master, typically a CPU. A continuous clock stream is not expected. The maximum frequency supported is 8.3 MHz. The CPU's SMI interface is used to access the registers in the Switch and it is available in all combinations of SW_MODE[1:0] (Table 14). MDC_CPU is internally pulled high via a resistor so it can be left floating when unused.
123	MDIO_CPU	I/O, PU	Management Data I/O, Slave. MDIO_CPU is used to transfer management data in and out of the device synchronously to MDC_CPU. This pin requires an external pull-up resistor in the range of 4.7 kohm to 10 kohm. The 88E6165 device uses one or all of the 32 possible SMI port addresses (two modes are supported). The address(es) that are used are selectable using the P3_OUTD[4:0]/ADDR[4:0] pins (Table 6). MDIO_CPU is internally pulled high via a resistor so it can be left floating when unused.

Table 13: Serial EEPROM Interface

Pin #	Pin Name	Pin Type	Description
59	EE_CS /EE_4WIRE	Typically O, PU	Serial EEPROM chip select. EE_CS is the serial EEPROM chip select referenced to EE_CLK. It is used to enable the external EEPROM (if present), and to delineate each data transfer. EE_CS is a multi-function pin used to configure the devices during a hardware reset. When reset is asserted, EE_CS becomes an input and the desired EEPROM type configuration is latched at the rising edge of RESETn as follows: 0 = It supports 2-Wire (for 1K bit 24C01A, 2K bit 24C02 & 4K bit 24C04) 1 = It supports 4-Wire (for 2K bit 93C56 & 4K bit 93C66) The external 4-Wire EEPROM must be configured in the x16 organization using 8-bit addresses. EE_CS is internally pulled high via a resistor so the pin can be left floating when unused or to select support for a 4-Wire device. Use a 4.7 kohm resistor to VSS for a configuration low.
58	EE_CLK /FD_FLOW_DIS	Typically O, PU	Serial EEPROM clock. EE_CLK is the serial EEPROM clock reference output by the 88E6165 device. It is used to shift the external serial EEPROM (if installed) to the next data bit so the default values of the internal registers can be overridden. EE_CLK is a multi-function pin used to configure the 88E6165 device during a hardware reset. When reset is asserted, EE_CLK becomes an input and it becomes the full-duplex Flow Control disable as follows: 0 = Enable advertisement of full-duplex flow control on all PHYs 1 = Disable full-duplex flow control on all full-duplex ports Full-duplex flow control requires support from the end station. It is supported on any full-duplex port that has Auto-Negotiation enabled, advertises that it supports Pause (i.e., FD_FLOW_DIS = Low at reset), and sees that the end station also supports Pause (from data returned during Auto-Negotiation). EE_CLK is internally pulled high via a resistor so the pin can be left unconnected for a configuration high. Use a 4.7 kohm resistor to VSS for a configuration low.

Table 13: Serial EEPROM Interface (Continued)

Pin #	Pin Name	Pin Type	Description
57	EE_DIN /HD_FLOW_DIS	Typically I, PU O During EEPROM Loading	Serial EEPROM data into the 4-Wire EEPROM devices. EE_DIN is serial EEPROM data referenced to EE_CLK used to transmit the EEPROM command and address to the external 4-Wire serial EEPROM (if present). The pin is not used for 2-Wire EEPROMs. EE_DIN is a multi-function pin used to configure the devices during a hardware reset. When reset is asserted, EE_DIN becomes an input and it becomes the half-duplex Flow Control disable as follows: 0 = Enable “forced collision” flow control on all half-duplex ports 1 = Disable flow control on all half-duplex ports Half-duplex flow control is active on all half-duplex ports when enabled. HD_FLOW_DIS is latched after reset. EE_DIN is internally pulled high via a resistor so it can be left floating to disable half-duplex flow control or when the pin is unused. Use a 4.7 kohm resistor to VSS for a configuration low.
55	EE_DOUT	I, PU	Serial EEPROM data out from 4-Wire EEPROM devices or Serial EEPROM data I/O to/from 2-Wire EEPROM devices. EE_DOUT is serial EEPROM data referenced to EE_CLK used to receive (and send if 2-Wire EEPROM) the EEPROM (address) data (to) from the external serial EEPROM (if present). EE_DOUT is internally pulled high via a resistor so it can be left floating when the pin is unused.

Table 14: Switch Configuration Interface

Pin #	Pin Name	Pin Type	Description
62 61	SW_MODE[1] SW_MODE[0]	I, PU	Switch Mode. These pins are used to configure the 88E6165 device after reset. Switch Mode pins work as follows: 1 0 Description 0 0 CPU attached mode – ports come up disabled[1] 0 1 Reserved 1 0 Test mode – ports come up enabled – EEPROM is ignored 1 1 EEPROM attached mode – EEPROM defined port states[2] The EEPROM attached mode (when both SW_MODE pins = high) can be used with a CPU. An EEPROM can also be used in CPU attached mode (when both SW_MODE pins are low). The difference between these two modes is the initial setting of the port's Port State bits. In CPU attached mode, the port comes up disabled so the CPU can fully configure the switch before packets are allowed to flow. This is critical in LAN to WAN Routers to prevent a 'leak' between the LAN and the WAN while the CPU is booting. In all but the Test mode, the INTn pin will go active low after the EEPROM is done initializing the internal registers. EEPROM data is not read in if the Test mode is selected. EEPROM data is read in if one of the three other modes (CPU attached mode, Boot mode, and EEPROM attached mode - SW_MODE[1:0] = 0b00, 0b01, and 0b11, respectively) is selected. SW_MODE[1:0] are not latched on the rising edge of RESETn and they must remain static for proper device operation. They are internally pulled high via resistors so the pins can be left unconnected to enable the EEPROM attached mode.

1. The ports come up disabled in the CPU mode so the CPU can fully boot and configure the switch before packets are allowed to flow. This is required for WAN to LAN Routers or for CPUs that must perform switch configuration before packets are allowed to flow.
2. In EEPROM attached mode the ports come up enabled unless the Port Control register (see 88E6165 Datasheet Part 2 Switch Core) is overwritten by the EEPROM data (see 88E6165 Datasheet Part 2 Switch Core, section 12 on the EEPROM programming format). This mode is for unmanaged switches without a CPU attached to the switch. It can also be used to debug a new managed switch or Router design so the switch will work without any software. If this is done for debug, ensure production units use the CPU attached mode.

Table 15: Power & Ground

Pin #	Pin Name	Pin Type	Description
71 79 91 97 113 120 128 135 142 149 155 162 167 183 189 197 200	VDDO_CORE	Power	1.0V power to the digital core.
175 185 193	VDDO_LED	Power	Power to LEDs.
115	VDDO_SMI_PHY	Power	Power to the MDC_PHY and MDIO_PHY I/Os. VDDO_SMI_PHY is connected to 1.8V to support 1.8V I/Os or connected to 2.5V to support 2.5V I/Os (2.5V I/Os are 3.3V tolerant). See SMI_PHY_VDDO_SEL.
117	SMI_PHY_VDDO_SEL	I, PD	The pads for these devices are both 1.8V and 2.5V capable. This pin acts as a select pin for selecting between 1.8V and 2.5V supplies. 0 = This pin allows the SMI_PHY_VDDO to operate at 2.5V power supply. 1 = This pin allows the SMI_PHY_VDDO to operate at 1.8V power supply. This pin is internally pulled low via a resistor so it can be left floating when the pin is unused.
69 78 88	P4_VDDO	Power	Power to the Port 4 GMII interface. P4_VDDO is connected to 1.8V to support 1.8V I/Os or connected to 2.5V to support 2.5V I/Os (2.5V I/Os are 3.3V tolerant). See P4_VDDO_SEL.
63	P4_VDDO_SEL	I, PD	Port 4 GMII Pad Voltage Select. The pads for these devices are both 1.8V and 2.5V capable. The P4_VDDO_SEL selects one of these two voltages. 0 = This pin allows the P4_VDDO to operate at 2.5V power supply. 1 = This pin allows the P4_VDDO to operate at 1.8V power supply This pin is internally driven low via a resistor so that the pin can be left floating when unused.

Table 15: Power & Ground (Continued)

Pin #	Pin Name	Pin Type	Description
111	P4_VDDOS	Power	Power to the Port 4 SDET and LED interfaces. P4_VDDOS is connected to 1.8V to support 1.8V I/Os or connected to 2.5V to support 2.5V I/Os (2.5V I/Os are 3.3V tolerant). See P4_VDDOS_SEL.
109	P4_VDDOS_SEL	I, PD	Port 4 SDET and LED Pad Voltage Select. The pads for these devices are both 1.8V and 2.5V capable. The P4_VDDOS_SEL selects one of these two voltages. 0 = This pin allows the P4_VDDOS to operate at 2.5V power supply. 1 = This pin allows the P4_VDDOS to operate at 1.8V power supply This pin is internally driven low via a resistor so that the pin can be left floating when unused.
118 132 141 151	P5_VDDO	Power	Power to the Port 5 GMII interface. P5_VDDO is connected to 1.8V to support 1.8V I/Os or connected to 2.5V to support 2.5V I/Os (2.5V I/Os are 3.3V tolerant). See P5_VDDO_SEL.
125	P5_VDDO_SEL	I, PD	Port 5 Pad Voltage Select. The pads for the device are both 1.8V and 2.5V capable. The P5_VDDO_SEL selects one of these two voltages. 0 = This pin allows the P5_VDDO to operate at 2.5V power supply. 1 = This pin allows the P5_VDDO to operate at 1.8V power supply This pin is internally driven low via a resistor so that the pin can be left floating when unused.
56	EE_VDDO	Power	Power supply to the EEPROM interface. EE_VDDO is connected to 1.8V to support 1.8V I/Os or connected to 2.5V to support 2.5V I/Os (2.5V I/Os are 3.3V tolerant). See EE_VDDO_SEL.
60	EE_VDDO_SEL	I, PD	EEPROM Pad Voltage Select. The pads for the device are both 1.8V and 2.5V capable. The EE_VDDO_SEL selects one of these two voltages. 0 = This pin allows the EE_VDDO to operate at 2.5V power supply. 1 = This pin allows the EE_VDDO to operate at 1.8V power supply This pin is internally driven low via a resistor so that the pin can be left floating when unused.

Table 15: Power & Ground (Continued)

Pin #	Pin Name	Pin Type	Description
171	LED_VDDO_SEL	I, PD	Gigabit PHY LED voltage select. The pads for the device is both 1.8V and 2.5V capable. The LED_VDDO_SEL selects one of these two voltages. 0 = This pin allows the LED_VDDO to operate at 2.5V power supply. 1 = This pin allows the LED_VDDO to operate at 1.8V power supply This pin is internally driven low via a resistor so that the pin can be left floating when unused.
202 210	AVDD	Power	Gigabit PHY 1.8V common power.
106 100	P5_AVDD P4_AVDD	Power	1.8V Power to analog power used to power each SERDES interface. If Port 5 or Port 4 are not used, tie P5_AVDD or P4_AVDD respectively, to VSS to save power.
52 47 36 41 30 25 19 14 8 3	P4_AVDD P4_AVDD P3_AVDD P3_AVDD P2_AVDD P2_AVDD P1_AVDD P1_AVDD P0_AVDD P0_AVDD	Power	1.8V Power to analog core used to power each Gig PHY interface.
163	VPP	Power	1.8V PHY power.
165	AVDD_PLL	Power	1.8V power to the on-chip PLL circuitry
11 22 33 44 103	VSS	Ground	Ground to device. These ground pins are used to isolate the neighboring high speed interfaces from one another.
205 206	VSSC	Ground	Ground reference for XTAL_IN and XTAL_OUT pins.
EPAD	VSS	Ground	Ground to device. The 88E6165 device is package in a 144-pin LQFP package with an EPAD (exposed die pad) on the bottom of the package. This EPAD must be soldered to VSS as it is the main VSS connection on the device. The location and dimensions of the EPAD can be found in Figure 37 and Table 49, respectively. See the Marvell® EPAD Layout Guidelines Application Note for EPAD layout details.

Table 16: No Connect

Pin #	Pin Name	Pin Type	Description
82 93 94 156 159 160 161 164 166 168 169 170 176 180 186 191 196 198 199 201 207 208 209 212 213 214 215 216	NC	--	No Connect. Do not connect these pins to anything. These pins must be left unconnected.

1.2 88E6165 Device Pin Assignment List

Table 17: Package Pin List—Alphabetical by Signal Name

Pin Number	Pin Name
202	AVDD
210	AVDD
165	AVDD_PLL
119	CLK125
58	EE_CLK/FD_FLOW_DIS
59	EE_CS/EE_4WIRE
57	EE_DIN/HD_FLOW_DIS
55	EE_DOUT
56	EE_VDDO
60	EE_VDDO_SEL
122	INTn
171	LED_VDDO_SEL
124	MDC_CPU
114	MDC_PHY
123	MDIO_CPU
116	MDIO_PHY
82	NC
93	NC
94	NC
156	NC
159	NC
160	NC
161	NC
164	NC
166	NC
168	NC
169	NC
170	NC
176	NC
180	NC
186	NC
191	NC
196	NC
198	NC
199	NC
201	NC
207	NC
208	NC
209	NC
212	NC
213	NC
214	NC
215	NC
216	NC
3	P0_AVDD
8	P0_AVDD
172	P0_LED0
173	P0_LED1

Pin Number	Pin Name	Pin Number	Pin Name
174	P0_LED2	182	P2_LED1
9	P0_MDIN[0]	184	P2_LED2
6	P0_MDIN[1]	31	P2_MDIN[0]
4	P0_MDIN[2]	28	P2_MDIN[1]
1	P0_MDIN[3]	26	P2_MDIN[2]
10	P0_MDIP[0]	23	P2_MDIN[3]
7	P0_MDIP[1]	32	P2_MDIP[0]
5	P0_MDIP[2]	29	P2_MDIP[1]
2	P0_MDIP[3]	27	P2_MDIP[2]
14	P1_AVDD	24	P2_MDIP[3]
19	P1_AVDD	36	P3_AVDD
177	P1_LED0	41	P3_AVDD
178	P1_LED1	187	P3_LED0
179	P1_LED2	188	P3_LED1
20	P1_MDIN[0]	190	P3_LED2
17	P1_MDIN[1]	42	P3_MDIN[0]
15	P1_MDIN[2]	39	P3_MDIN[1]
12	P1_MDIN[3]	37	P3_MDIN[2]
21	P1_MDIP[0]	34	P3_MDIN[3]
18	P1_MDIP[1]	43	P3_MDIP[0]
16	P1_MDIP[2]	40	P3_MDIP[1]
13	P1_MDIP[3]	38	P3_MDIP[2]
25	P2_AVDD	35	P3_MDIP[3]
30	P2_AVDD	47	P4_AVDD
181	P2_LED0	52	P4_AVDD

Pin Number	Pin Name
100	P4_AVDD
96	P4_COL
95	P4_CRS
64	P4_GMII_EN
76	P4_GTXCLK/JUMBO
80	P4_INCLK
83	P4_IND[0]
84	P4_IND[1]
85	P4_IND[2]
86	P4_IND[3]
87	P4_IND[4]
89	P4_IND[5]
90	P4_IND[6]
92	P4_IND[7]
81	P4_INDV
110	P4_LED
192	P4_LED0
194	P4_LED1
195	P4_LED2
53	P4_MDIN[0]
50	P4_MDIN[1]
48	P4_MDIN[2]
45	P4_MDIN[3]
54	P4_MDIP[0]
51	P4_MDIP[1]

Pin Number	Pin Name
49	P4_MDIP[2]
46	P4_MDIP[3]
77	P4_OUTCLK
74	P4_OUTD[0]/P4_MODE[0]
73	P4_OUTD[1]/P4_MODE[1]
72	P4_OUTD[2]/P4_MODE[2]
70	P4_OUTD[3]
68	P4_OUTD[4]
67	P4_OUTD[5]/LED_MODE
66	P4_OUTD[6]/RMU_MODE[0]
65	P4_OUTD[7]/RMU_MODE[1]
75	P4_OUTEN/P4_HALFDPX
102	P4_RXN
101	P4_RXP
112	P4_SDET
99	P4_TXN
98	P4_TXP
69	P4_VDDO
78	P4_VDDO
88	P4_VDDO
63	P4_VDDO_SEL
111	P4_VDDOS
109	P4_VDDOS_SEL
106	P5_AVDD
158	P5_COL/P5_SDET

Pin Number	Pin Name
157	P5_CRS/P5_LED
126	P5_GMII_EN
139	P5_GTXCLK/AM_DIS
143	P5_INCLK
145	P5_IND[0]
146	P5_IND[1]
147	P5_IND[2]
148	P5_IND[3]
150	P5_IND[4]
152	P5_IND[5]
153	P5_IND[6]
154	P5_IND[7]
144	P5_INDV
140	P5_OUTCLK
137	P5_OUTD[0]/P5_MODE[0]
136	P5_OUTD[1]/P5_MODE[1]
134	P5_OUTD[2]/P5_MODE[2]
133	P5_OUTD[3]/ADDR[0]
131	P5_OUTD[4] /ADDR[1]
130	P5_OUTD[5]/ADDR[2]
129	P5_OUTD[6]/ADDR[3]
127	P5_OUTD[7]/ADDR[4]
138	P5_OUTEN/P5_HALFDPX/
108	P5_RXN
107	P5_RXP

Pin Number	Pin Name
105	P5_TXN
104	P5_TXP
118	P5_VDDO
132	P5_VDDO
141	P5_VDDO
151	P5_VDDO
125	P5_VDDO_SEL
121	RESETn
211	RSET
117	SMI_PHY_VDDO_SEL
61	SW_MODE[0]
62	SW_MODE[1]
71	VDDO_CORE
79	VDDO_CORE
91	VDDO_CORE
97	VDDO_CORE
113	VDDO_CORE
120	VDDO_CORE
128	VDDO_CORE
135	VDDO_CORE
142	VDDO_CORE
149	VDDO_CORE
155	VDDO_CORE
162	VDDO_CORE
167	VDDO_CORE

Pin Number	Pin Name
183	VDDO_CORE
189	VDDO_CORE
197	VDDO_CORE
200	VDDO_CORE
175	VDDO_LED
185	VDDO_LED
193	VDDO_LED
115	VDDO_SMI_PHY
163	VPP
11	VSS
22	VSS
33	VSS
44	VSS
103	VSS
EPAD	VSS
205	VSSC
206	VSSC
204	XTAL_IN
203	XTAL_OUT

Section 2 Application Examples

2.1 Examples using the 88E6165 Device

Figure 3: Gigabit Firewall Router with four 10/100/1000BASE-T LAN Ports and one 10/100/1000BASE-T WAN Port

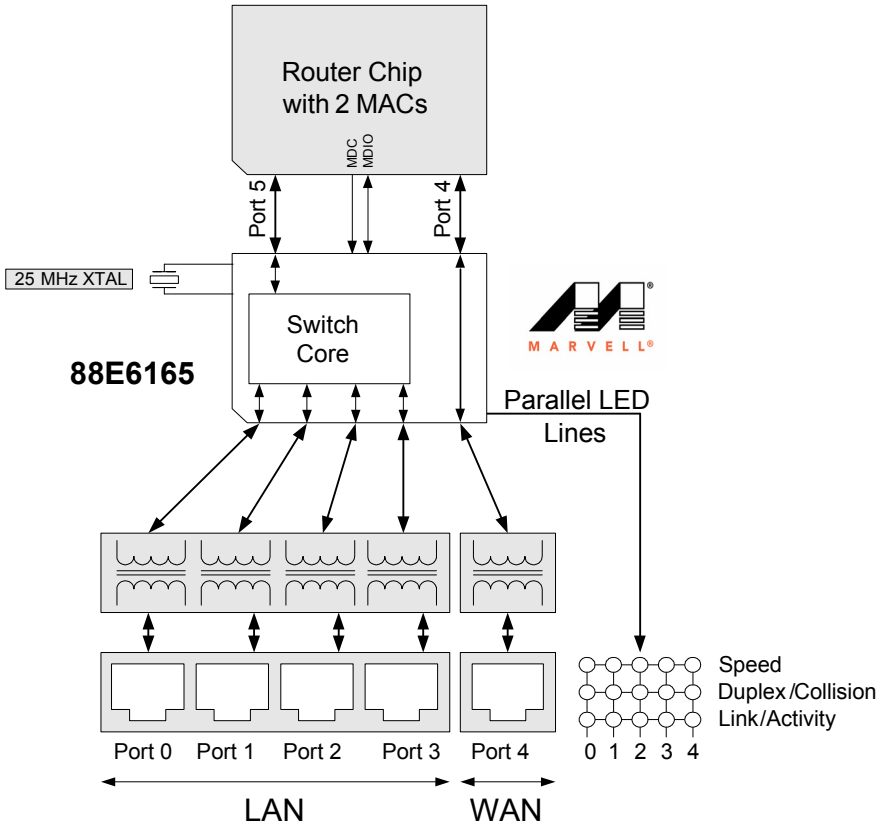


Figure 4: Gigabit Ethernet Firewall Router with 100BASE-FX or 1000BASE-X fiber WAN Port

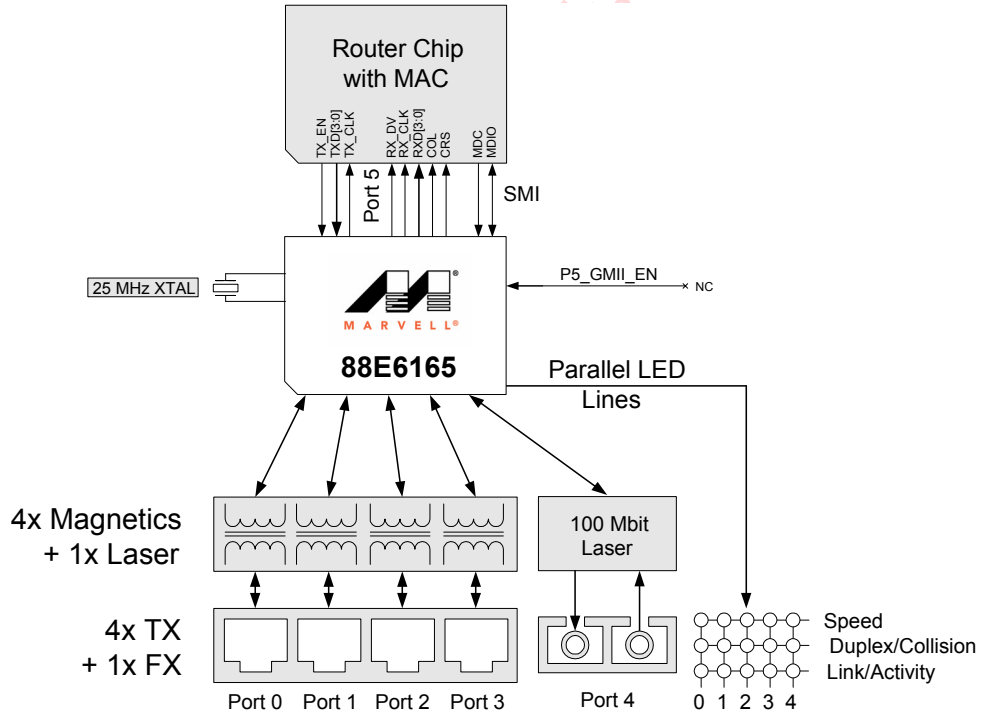


Figure 5: Wireless 5 Port Gigabit Ethernet SMB Switch

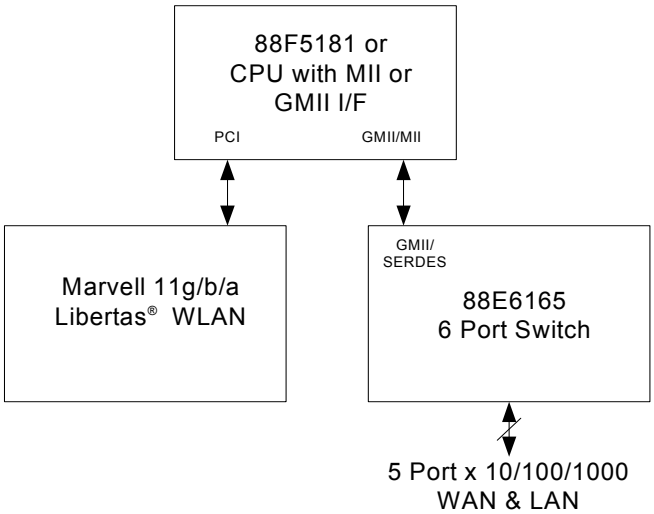


Figure 6: Multi-dwelling Unit Interface Gateway

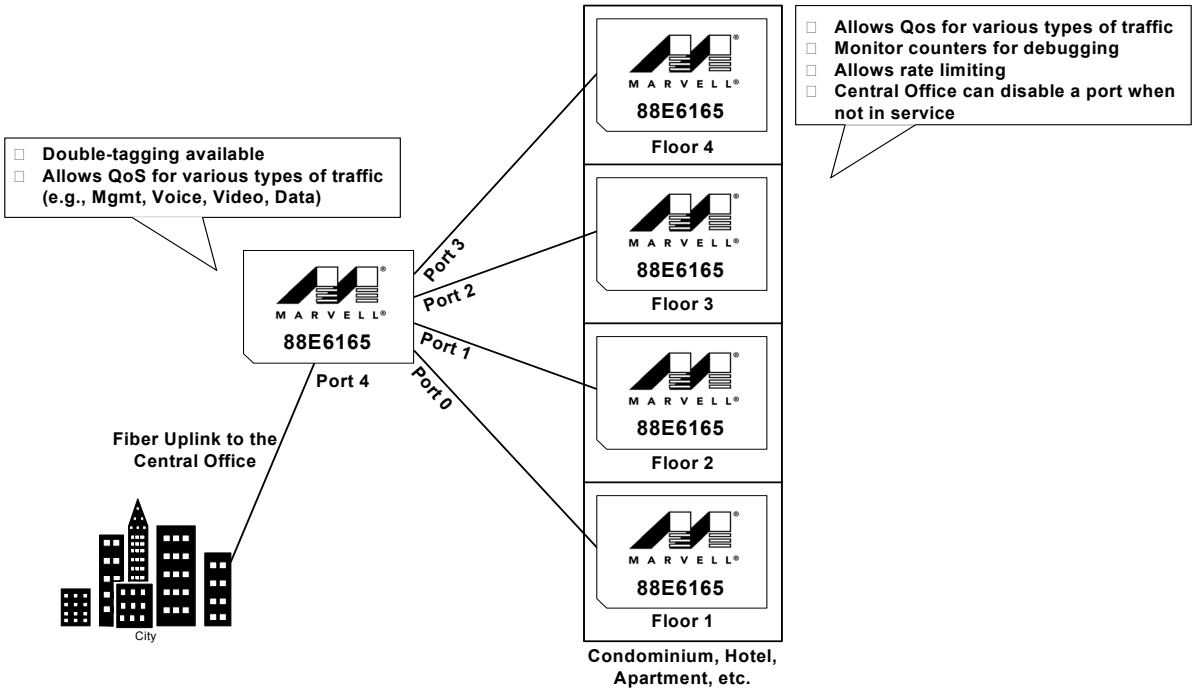
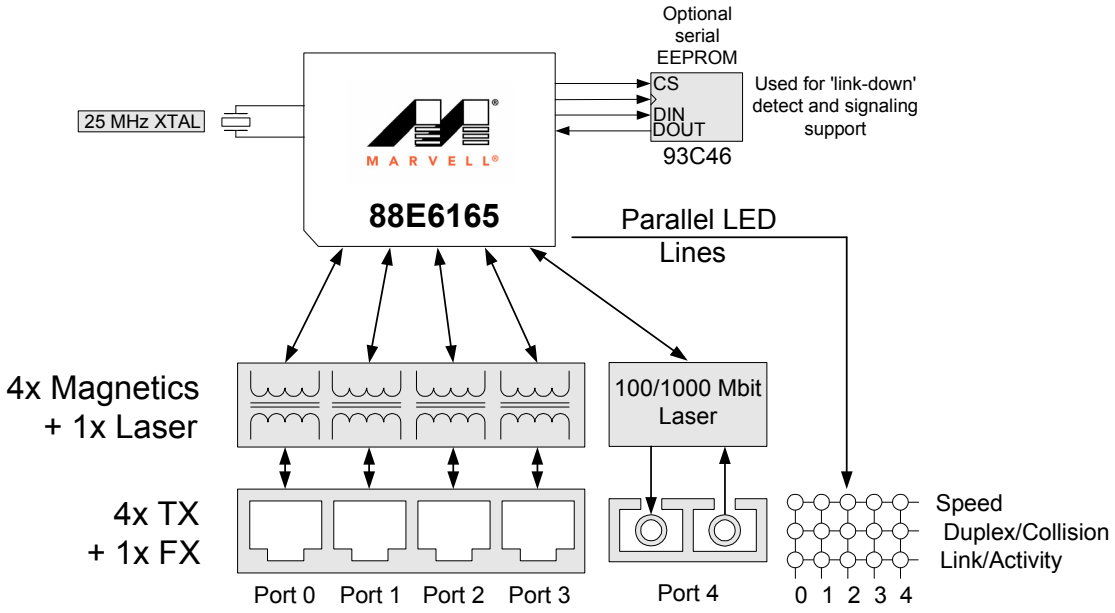


Figure 7: Media Converter for 100BASE-FX/1000BASE-X fiber to 10/100/1000BASE-T copper



2.2 Device Physical Interfaces

The device contains a number of interfaces that support both copper and fiber media. Table 18 lists the interfaces supported on each port of the 88E6165 device. Refer to the diagrams further in this section for connection details.

Table 18: 88E6165 Device Interfaces

Port	10BASE-T 100BASE-T	1000BASE-T	100BASE-FX	1000BASE-X/ SGMII/ SERDES	200 Mbps MII	RGMII[1]
0-3	x	x				
4	x	x	x	x	x	
5			x	x	x	x

1. 1000BASE-X, full-duplex only.

2.2.1 10/100/1000 PHY Interface

Ports 0 to 4 on the device support a 10/100/1000 PHY interface. In the device, this interface supports 10BASE-T, 100BASE-TX, and 1000BASE-T copper IEEE standards. Port 4 and Port 5 support a 100BASE-FX fiber option as well. The MAC inside the switch works the same way regardless of the external interface being used. Each PHY's Link, Speed, Duplex and Flow Control information is directly communicated to the MAC it is attached to so the MAC tracks, or follows, the mode the PHY links up in. A detailed description of the PHY functional and register description is covered in "88E6165 Datasheet Part 3 of 3: Gigabit PHYs".

2.2.2 MII 200 Mbps Mode

Port 4 and Port 5 of the device's GMII/MII interfaces can run at a data rate of 200 Mbps, full-duplex. Do not select this mode unless the MAC on the other end of the MII interface can also run at double speed rate. Both PHY (reverse MII) and MAC (forward MII) 200 Mbps modes are supported. When the 200 Mbps PHY mode is selected, the output MII clocks run at 50 MHz rate. These is no change in the format of the data, it just runs faster. When the 200 Mbps MAC mode is selected, the input MII clocks must be 50 MHz ±50 ppm. Again, the format of the data is not changed.

2.2.3 SERDES or (G)MII Interface

Port 4 and Port 5 are SERDES interfaces. The SERDES interfaces can be used for these options

- Connection to Marvell® triple speed 10/100/1000 copper PHYs
- Connection to 1000BASE-X fiber modules
- SGMII interface
- Cross-chip connection to other Marvell switch devices - i.e., cross-chip connection

2.2.3.1 Triple Speed PHY SERDES Interface Option

Port 4 and Port 5's SERDES can be configured to use a triple speed PHY interface to an external PHY. In this mode, the SERDES use the SGMII protocol. The in-band Link, Speed and Duplex signals in the SGMII protocol are ignored. The external PHY's Link, Speed, Duplex and Flow Control information must be transferred to the

port's MAC so the MAC is in the correct mode. This can be done in software (if the port's PHYDetect bit is zero - Port offset 0x00) or it is done automatically by the PHY Polling Unit (PPU - Section 2.2.6)

The triple speed PHY interface can support Marvell PHYs with Auto-Media Detect™ for auto switching between copper and fiber. This can be supported in software or automatically in hardware by the PHY Polling Unit (PPU) and by setting the port's MGMII bit to a one (in the port's Port Status Register - offset 0x00). If the port's MGMII bit is not set to a one, the PPU will support copper only and will not support Auto-Media Detect.

Port 4 is set to Triple Speed PHY mode if its Px_LED/Px_MODE pin is low at the rising edge of RESETn and if the port's PHYDetect bit is a 1 (in the port's Port Status Register - offset 0x00). PHYDetect will be set to a 1 on Port 4if the PPU finds a PHY at SMI address 0x08.

Ports 4 and Port 5 are set to Triple Speed PHY mode if their Px_OUTD[2:0]/Px_MODE[2:0] pins are set to 0x6 at the rising edge of RESETn. The automatic transfer of PHY status to its MAC requires that the port's PHYDetect bit be a 1 (in the port's Port Status Register - offset 0x00). PHYDetect will be set to a 1 on port 9 if the PPU finds a PHY at SMI address 0x09. It will be set to a 1 on port 10 if the PPU finds a PHY at SMI address 0x0A.

2.2.3.2 IEEE 1000BASE-X SERDES Interface Option

Port 4 and Port 5's SERDES can be configured in 1000BASE-X.

Port 4 is set to 1000BASE-X mode if its Px_LED/Px_MODE pin is high at the rising edge of RESETn. Connecting an LED to VDDO through a resistor to this pin will enable 1000BASE-X on the port. After RESETn the Px_LED/Px_MODE pin will become the Link/Activity LED for the port (off = no link, on = link, blink = activity).

Ports 4 and Port 5 are set to 1000BASE-X mode if their Px_OUTD[2:0]/Px_MODE[2:0] pins are set to 0x5 at the rising edge of RESETn. In this mode, the Px_CRS/Px_LED pin become the Link/Activity LED for the port (off = no link, on = link, blink = activity) after RESETn.

The port enters 1000BASE-X mode, if configured, even if an external PHY is detected at the port's SMI address.

1000BASE-X mode uses a PCS to auto-negotiate with a link partner to determine if Flow Control should be supported or not (auto-negotiation can be disabled). Link will be automatically established if the port's Px_SDET is detected high and the port's PCS determines Sync is OK (sets the port's SyncOK to a 1). Link will automatically go down if either Px_SDET or SyncOK go to zero. Speed is always 1000 Mbps and Duplex is always full-duplex on 1000BASE-X ports. An interrupt can be generated on the ports when link changes state (see Global 2, offset 0x00 and 0x01).

2.2.3.3 Cross-chip Interface Option

Port 4 and Port 5's SERDES can be configured in cross-chip mode. This mode is used to connect two or more Marvell® switch devices together to create a larger switch. 1000BASE-X protocol is used on the line and the port's Speed is locked to 1000 Mbps and its Duplex is fixed at full-duplex.

Port 4 is set to cross-chip mode if its Px_LED/Px_MODE pin is low at the rising edge of RESETn and if the port's PHYDetect bit is a 0 (in the port's Port Status Register - offset 0x00). PHYDetect will be set to a 0 on port 4 if the PPU cannot find a PHY at SMI address 0x08.

Port 4 and Port 5 are set to cross-chip mode if their PxOUTD[2:0]/Px_MODE[2:0] pins are set to 0x4 at the rising edge of reset.

Note

Ports that are configured in cross-chip mode are initialized with their Link down. This gives software time to initialize the switch's configuration before software allows packets to flow by forcing the port's link up (using the port's ForcedLink bit in the port's PCS Control register - offset 0x01).

2.2.3.4 Port Status Registers

Each switch port of the devices has a status register that reports information about that port's MAC, SERDES or (G)MII interface. These registers can be used to check the current port configuration. See 88E6165 Datasheet, Part 2: Switch Core, Port Status Register, for more information.

2.2.4 Port 4 Bypass Control

Port 4 can be connected to an external PHY, SERDES/1000BASE-X/SGMII, or GMII/MII interface. In order to support configurations where a CPU is connected to the switch and the CPU will receive all traffic from Port 4, the switch core can be bypassed. In the bypass configuration, the switch core will only be supporting five ports (Port 0 to Port 3 and Port 5).

The P4_MODE[2:0] pins are used to configure the bypass modes. Refer to Table 19 for details. Three different types of bypass mode are supported:

- Port 4 connected to GMII/MII Interface
- Port 4 connected to SERDES/1000BASE-X/SGMII interface
- Port 4 connected to network 10/100/1000 PHY Interface (MDI)

Table 19 describes the P4_MODE[2:0] configuration options for each bypass mode option.

Table 19: 88E6165 Bypass Modes

P4_MODE[2:0]	Connection	Bypass
000	GMII	SERDES and GPHY
001	Reserved	
010	MII 100	
011	MII 10	
100	PHY	SERDES and GMII/MII
101	1000BASE-X	GPHY and GMII/MII
110	SGMII	
111	100BASE-FX	

2.2.5 Digital Interface Options

The (G)MII digital interface supports many different modes defined in the following sections. The mode to use is configured once at reset by external pull-up resistors connected to the P4_MODE[2:0] and P5_MODE[2:0] pins. If Port 4 or Port 5 is not connected to any device, the port should be disabled. If Port 4 or Port 5's(G)MII digital pins are unused but the port's SERDES interface is used, the P4_MODE[2:0] or P5_MODE[2:0] pins must be set accordingly. See Table 6 and Table 9 for more information.

Port 4 supports MII MAC mode, MII PHY mode and (G)MII mode options, while Port 5 supports MII MAC mode, MII PHY mode, RGMII and (G)MII mode options.

Note

(G)MII PHY mode and (G)MII MAC mode are discussed in the following sections. Electrically, there is no difference since the GMII Interface uses source synchronous clocks. Each concept is discussed separately since the port supports being connected to an external PHY (GMII MAC mode - where the port looks like a MAC supporting 10/100/1000 Mbps) or to an external MAC (GMII PHY mode where the port looks like a PHY supporting 1000 Mbps only).

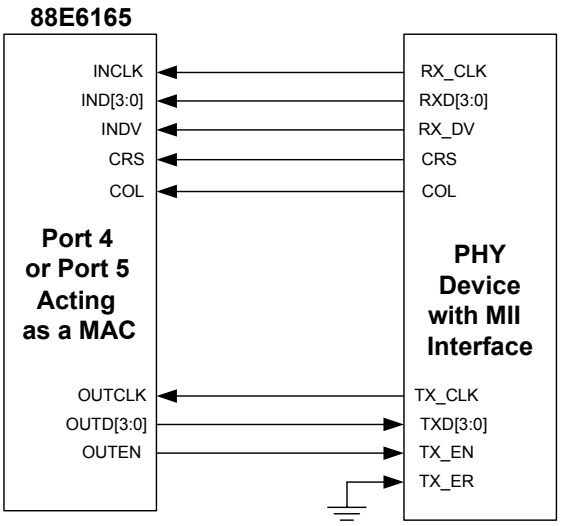
Warning

A port's SERDES must be powered up to generate the GTX_CLK output for MII PHY modes of operation.

2.2.5.1 MII MAC Mode

The MII MAC Mode, sometimes called 'Forward MII', configures Port 4 or Port 5's GMAC inside the devices to act as a MAC so it can be directly connected to an external MII-based PHY. In this mode, the devices receive the interface clocks (Px_OUTCLK and Px_INCLK) from the PHY and will work at any frequency from DC to 50 MHz (50 MHz supports 200 Mbps in each direction). The two clocks can be asynchronous with each other. Both full- and half-duplex modes are supported and need to be selected to match the mode of the link partner's MAC. The MII MAC mode is compliant with IEEE 802.3 clause 22. (**Note:** The MII requires only four data bits in each direction so only the lower four data bits are used). P4_MODE or P5_MODE should be set correctly at reset (see Table 6 and Table 9) to select this configuration and the PHY's SMI address must be set to 0x04 for Port 4 or 0x05 for Port 5 for auto-negotiation to operate correctly.

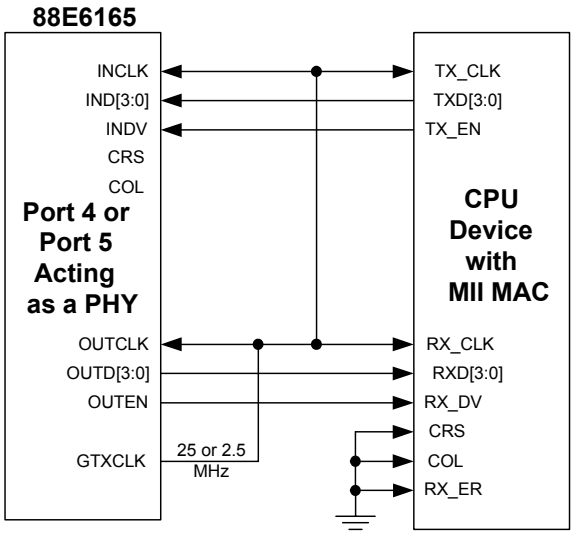
Figure 8: MII MAC Interface Pins



2.2.5.2 MII PHY Mode

The MII PHY Mode, sometimes called ‘Reverse MII’, configures Port 4 or Port 5’s GMAC inside the device to act as a PHY so that it can be directly connected to an external MAC. In this mode, the devices drive the interface clocks (INCLK and OUTCLK for both MACs) from its GTXCLK pin so the appropriate GTXCLK frequency must be selected. GTX_CLK is used as a generic asynchronous clock source, but it is recommended that there are not more than four loads on GTX_CLK. For connection to more than four loads (that is, connection for use with Port 4), buffer Port 5’s GTX_CLK, or use a generic oscillator. Only full-duplex modes are supported (since CRS and COL are not driven by the devices outputs) and must match the mode of the link partner’s MAC. The MII PHY mode is compliant with IEEE 802.3 clause 22 in full-duplex mode (**Note**: The MII requires only four data bits in each direction so only the lower four data bits on the devices are used). At reset, P4_MODE and P5_MODE should be set for the appropriate speed —see Table 6 and Table 9. In this mode, there is no external PHY for Port 4 or Port 5, and so Port 4 or Port 5 is skipped by the PPU. In Reverse MII mode initially, the link status is down requiring the system software to force the port’s link up to enable the port.

Figure 9: MII PHY Interface Pins

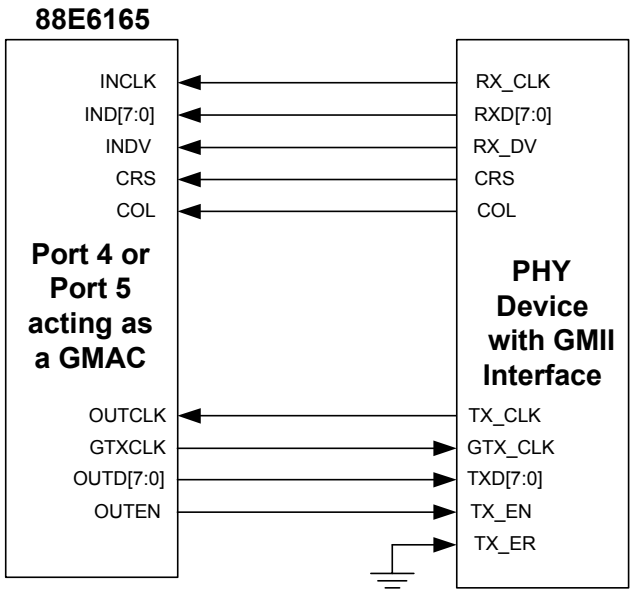


2.2.5.3 GMII MAC Mode

The GMII MAC Mode, sometimes called 'Forward GMII', configures Port 4's or Port 5's GMAC inside the device to act as a gigabit MAC (GMAC) so that it can be directly connected to an external GMII-based Gigabit PHY. In this mode, the devices receive the interface clocks (OUTCLK and INCLK) from the PHY but generates GTXCLK for the PHY. 10 Mbps, 100 Mbps or 1000 Mbps is supported in this configuration. Full- and half-duplex modes are supported at 10 Mbps or 100 Mbps. Full-duplex is supported at 1000 Mbps. The speed and mode in the external PHY's auto-negotiation must be restricted from advertising the 1000BASE, half-duplex case as the GMAC inside the devices do not support that mode. This is done automatically by the PHY Polling Unit (PPU) inside the devices. GMII MAC mode is compliant with IEEE 802.3 clause 28. P4_MODE and P5_MODE should be set to GMII mode at reset (see Table 6 and Table 9) for this configuration and the PHY's SMI address must be set to 0x04 for Port 4 or 0x05 for Port 5 for auto-negotiation to operate correctly.

A triple speed interface is supported in GMII MAC mode (i.e., 10, 100 and 1000). When the PHY completes auto-negotiation and brings the link up the auto-negotiated speed, duplex and flow control information must be moved from the PHY to the MAC so the MAC matches the PHY's settings. This is done automatically by the PPU if the port's PHYDetect bit is set to a one (Port offset 0x00). The interface pins will track the speed that the MAC is set to.

Figure 10: GMII MAC Interface Pins

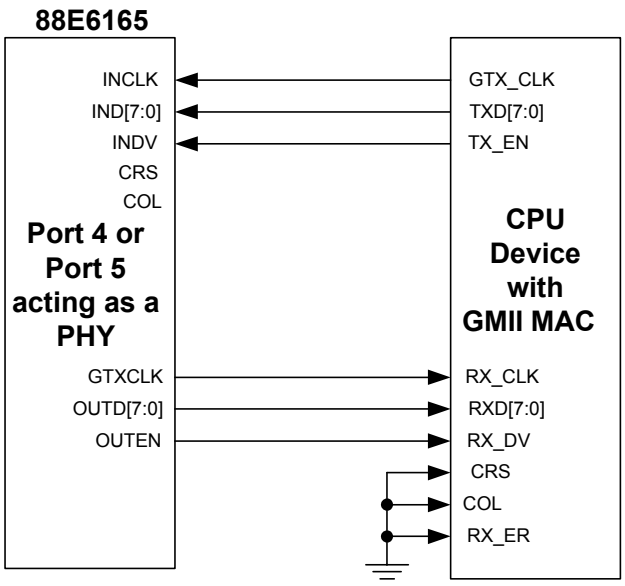


2.2.5.4 GMII PHY Mode

The GMII PHY Mode, sometimes called ‘Reverse GMII’, configures Port 4’s or Port 5’s GMAC inside the device to act as a gigabit PHY so that it can be directly connected to an external GMAC. In this mode, the devices drive the transmit interface clock (GTXCLK) and accept the receive interface clock (INCLK). Only gigabit full-duplex mode is supported and must match the mode of the link partner’s GMAC. GMII PHY mode is compliant with IEEE 802.3 clause 28 in gigabit full-duplex. P4_MODE and P5_MODE should be set to GMII mode at reset (see Table 6 and Table 9). In this mode, there is no external PHY for Port 4 or Port 5, so Port 4 or Port 5 are skipped by the PHY Polling Unit (PPU). Initially, the link status is configured down requiring the system software to force the port’s link up to enable the port (in the PCS Control Register).

This configuration is identical to the GMII MAC Mode described above except that a CPU is connected instead of a PHY. The lack of an external PHY device restricts the interface to a gigabit speed only with the link initially being down. This allows the CPU time to initialize itself before it enables the switch port connected to it by forcing link up in the switch port’s MAC (in the port’s PCS Control Register - offset 0x01).

Figure 11: GMII PHY Interface Pins

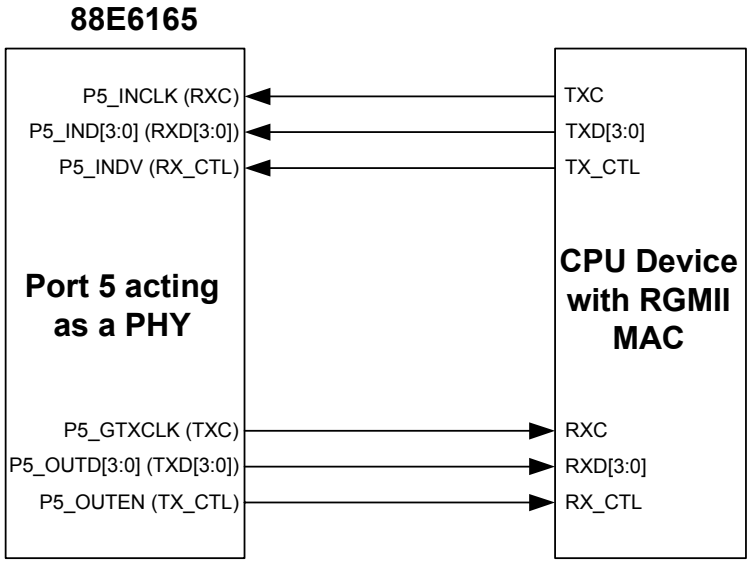


2.2.5.5 RGMII Mode

The RGMII Mode configures Port 5's GMAC to act as a Reduced Gigabit Media Independent Interface (RGMII) so that it can be directly connected to an external RGMII-based Gigabit MAC inside a CPU. When the RGMII mode is selected, transmit control (P5_OUTEN) is presented on both clock edges of P5_GTXCLK. Receive control (P5_INDV) is presented on both clock edges of P5_INCLK.

The lack of an external PHY device restricts the interface to a gigabit speed only with the link initially being down. This allows the CPU time to initialize itself before it enables the switch port connected to it by forcing link up in the switch port's MAC (in the port's PCS Control register - offset 0x01)

Figure 12: RGMII Interface Pins



2.2.6 PHY Polling Unit (PPU)

The devices contain a PHY Polling Unit (PPU) to transfer Link, Speed, Duplex and Pause information from an external PHY to its associated MAC (the internal PHYs use a direct approach such that this information is transferred even if the Port's PHYDetect bit is zero - Port offset 0x00). The PPU can perform this job only if the SMI address of the external PHY matches the physical port number it is connected to in the switch (i.e., the PHY connected to Port 4 uses SMI address 0x04, the PHY connected to Port 5 uses SMI address 0x05, etc.).

If the PPU is disabled on a port (i.e., the port's PHYDetect bit is zero), software must perform the job of setting the switch MAC's mode to the mode of the PHY (for the external PHYs) by forcing the MAC's link, speed, duplex and pause settings (in the port's PCS Control Register - offset 0x01) based upon what it sees in the PHY's registers. Link up must be the last mode register set and link down must be the first mode register cleared (i.e., the port's speed, duplex and pause modes must only be changed while the port's link is down).

Even though the PPU has full access to the external and internal PHY's registers software can access all of the PHY registers at any time by using the SMI Command and Data registers (Global 2, offsets 0x18 and 0x19).

Note

On previous devices, the PPU could be disabled by a PPUEn bit (Global 1, offset 0x04) and the PPU's state could be read in the PPUState bits (Global 1, offset 0x00). These bits exist and function the same in this device, but they are documented differently or as Reserved bits as this is no longer the recommended way to access the PHY registers (use the SMI Command and Data registers instead - Global 2, offsets 0x18 and 0x19). The PPUEn and PPUState bits will physically be changed in future devices to match this documentation.

Section 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 20: Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
$V_{DD(2.5)}$	Power Supply Voltage on any 2.5V signal with respect to VSS	-0.5	2.5	+3.6	V
$V_{DD(1.8)}$	Power Supply Voltage on any 1.8V supply with respect to VSS	-0.5	1.8	+3.6 or $V_{DD(2.5)}$ +0.5[1] whichever is less	V
$V_{DD(1.0)}$	Power Supply Voltage on any 1.0V supply with respect to VSS	-0.5	1.0	+3.6 or $V_{DD(1.8)}$ +0.5[2] whichever is less	V
V_{PIN}	Voltage applied to any input pin with respect to VSS	-0.5		+3.6 or V_{DDO_PIN}[3] +0.5[4] whichever is less	V
$T_{STORAGE}$	Storage temperature	-55		+125[5]	°C

1. VDD(1.8) must never be more than 0.5V greater than VDD(2.5) or damage will result. Power must be applied to VDD(2.5) before or at the same time as VDD(1.8).
2. VDD(1.0) must never be more than 0.5V greater than VDD(1.8) or damage will result. Power must be applied to VDD(1.8) before or at the same time as VDD(1.0).
3. The VDDO pad ring has separate I/O power supply options. Therefore, the voltage applied to a group of I/O pins must follow what is defined in Section 1
4. VPIN must never be more than 0.5V greater than VDDO or damage will result.
5. 125°C is the re-bake temperature. For extended storage time greater than 24 hours, +85°C should be the maximum.

3.2 Recommended Operating Conditions

Table 21: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD(2.5)}$	2.5V power supply	For any 2.5V supply pin[1]	2.375	2.5	2.625	V
$V_{DD(1.8)}$	1.8V power supply	For any 1.8V supply pin	1.710	1.8	1.890	V
$V_{DD(1.0)}$	1.0V power supply	For any 1.0V supply pin	.950	1.0	1.050	V
T_A	Ambient operating temperature[2]	Commercial parts	0		70	°C
T_J	Maximum junction temperature				125[2]	°C
IREF	Internal bias reference	External resistor value required to be placed between IREF and VSS pins	1980	2000	2020	Ω

1. Some VDDO pins can be set to either 1.8V or 2.5V. To guarantee proper operation they must be set within the appropriate ranges in this table. VDDO voltages between 1.890V and 2.625V are not supported.
2. The important parameter is maximum junction temperature. As long as the maximum junction temperature is not exceeded, the device can be operated at any ambient temperature. Refer to White Paper on "TJ Thermal Calculations" for more information.

3.3 Thermal Conditions for 88E6165 device 216-pin LQFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance[1] - junction to ambient of the 88E6165 device 216-Pin LQFP package $\theta_{JA} = (T_J - T_A)/ P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		19.60		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/ sec air flow		16.00		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/ sec air flow		15.10		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/ sec air flow		14.50		°C/W
ψ_{JT}	Thermal characteristic parameter[1] - junction to top center of the 88E6165 device 216-Pin LQFP package $\psi_{JT} = (T_J - T_{TOP})/P.$ T_{TOP} = Temperature on the top center of the package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.33		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/ sec air flow		0.51		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/ sec air flow		0.62		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/ sec air flow		0.70		°C/W
θ_{JC}	Thermal resistance[1] - junction to case of the 88E6165 device 216-Pin LQFP package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = Power Dissipation from the top of the package	JEDEC with no air flow		7.60		°C/W
θ_{JB}	Thermal resistance[1] - junction to board of the 88E6165 device 216-Pin LQFP package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		10.00		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

3.4 Current Consumption

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 22: Current Consumption

Pins	Parameter	Condition	Min	Typ	Max	Units
P4_AVDD (Pin 100) P5_AVDD (Pin 106)	1.8V power to analog core used to power SERDES interface	All ports active (Port 4 - Port 5 at 1000 Mbps)		48		mA
		All ports active (Port 4 - Port 5 at 100 Mbps)		48		mA
		All ports active (Port 4 - Port 5 at 10 Mbps)		48		mA
		All ports idle (Port 4 - Port 5 linked at 1000 Mbps but idle)		48		mA
		All ports idle (Port 4 - Port 5 linked at 100 Mbps but idle)		48		mA
		All ports idle (Port 0 - Port 2 linked at 10 Mbps but idle)		48		mA
		Reset		0		mA
		No link on any port		48		mA
Px_AVDD	1.8V power to analog core for each Gig PHY interface	All ports active (Port 0 - Port 4 at 1000 Mbps)		532		mA
		All ports active (Port 0 - Port 4 at 100 Mbps)		173		mA
		All ports active (Port 0 - Port 4 at 10 Mbps)		127		mA
		All ports idle (Port 0 - Port 4 linked at 1000 Mbps but idle)		532		mA
		All ports idle (Port 0 - Port 4 linked at 100 Mbps but idle)		173		mA
		All ports idle (Port 0 - Port 4 linked at 10 Mbps but idle)		115		mA
		Reset		8		mA
		No link on any port		33		mA

Table 22: Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
VDDO	2.5V to SMI PHY bus, SMI CPU bus, EEPROM, LED, and Port 4's and Port 5's GMII/MII I/O pins.	All ports active (Port 0 - Port 4 at 1000 Mbps)		65		mA
		All ports active (Port 0 - Port 4 at 100 Mbps)		16		mA
		All ports active (Port 0 - Port 4 at 10 Mbps)		7		mA
		All ports idle (Port 0 - Port 4 linked at 1000 Mbps but idle)		22		mA
		All ports idle (Port 0 - Port 4 linked at 100 Mbps but idle)		11		mA
		All ports idle (Port 0 - Port 4 linked at 10 Mbps but idle)		6		mA
		Reset		0		mA
		No link on any port		5		mA
VDDO	1.8V to SMI PHY bus, SMI CPU bus, EEPROM, LED, and Port 4's and Port 5's GMII/MII I/O pins.	All ports active (Port 0 - Port 4 at 1000 Mbps)		46		mA
		All ports active (Port 0 - Port 4 at 100 Mbps)		9		mA
		All ports active (Port 0 - Port 4 at 10 Mbps)		4		mA
		All ports idle (Port 0 - Port 4 linked at 1000 Mbps but idle)		18		mA
		All ports idle (Port 0 - Port 4 linked at 100 Mbps but idle)		7		mA
		All ports idle (Port 0 - Port 4 linked at 10 Mbps but idle)		3		mA
		Reset		0		mA
		No link on any port		2		mA

Table 22: Current Consumption (Continued)

Pins	Parameter	Condition	Min	Typ	Max	Units
VDD_CORE	1.0V power to digital core	All ports active (Port 0 - Port 4 at 1000 Mbps)		645		mA
		All ports active (Port 0 - Port 4 at 100 Mbps)		189		mA
		All ports active (Port 0 - Port 4 at 10 Mbps)		127		mA
		All ports idle (Port 0 - Port 4 linked at 1000 Mbps but idle)		569		mA
		All ports idle (Port 0 - Port 4 linked at 100 Mbps but idle)		185		mA
		All ports idle (Port 0 - Port 4 linked at 10 Mbps but idle)		125		mA
		Reset		10		mA
		No link on any port		127		mA
AVDD AVDD_PLL V_{CT}	1.8V power common block, PLL block, and to External Magnetics Center Tap Pin	All GE ports 1000 Mbps and active		562		mA
		All GE ports 100 Mbps and active		150		mA
		All GE ports 10 Mbps and active		356		mA
		All GE ports 1000 Mbps and idle		562		mA
		All GE ports 100 Mbps and idle		150		mA
		All GE ports 10 Mbps and idle		152		mA
		Reset		6		mA
		No link on any port		6		mA

3.5 DC Electrical Characteristics

3.5.1 Digital Operating Conditions

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 23: Digital Operating Conditions

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{IH}	High level input voltage	All pins	VDDO = 2.375V	1.7			V
			VDDO = 1.710V	1.4			V
V_{IL}	Low level input voltage	All pins	VDDO = 2.375V	-0.3		0.7	V
			VDDO = 1.710V	-0.3		0.54	V
V_{OH}	High level output voltage	LED pins	I_{OH} = -8 mA	VDDO - 0.4			V
		All others (except INTn [1])	I_{OH} = -4 mA	VDDO - 0.4			V
V_{OL}	Low level output voltage	INTn and LED pins	I_{OL}= 8 mA			0.4	V
		All others	I_{OL}= 4 mA			0.4	V
I_{ILK}	Input leakage current	With pull-up resistor	$0<V_{IN}<V_{DD}$			+ 10 - 50	µA
		With pull-down resistor	$0<V_{IN}<V_{DD}$			+ 50 - 10	µA
		All others	$0<V_{IN}<V_{DD}$			±10	µA
C_{IN}	Input capacitance	All pins				5	pF

1. The INTn is an active low, open drain pin. See INTn description in the Signal Description.

3.5.2 SERDES Electrical Specifications

3.5.2.1 Transmitter DC Characteristics

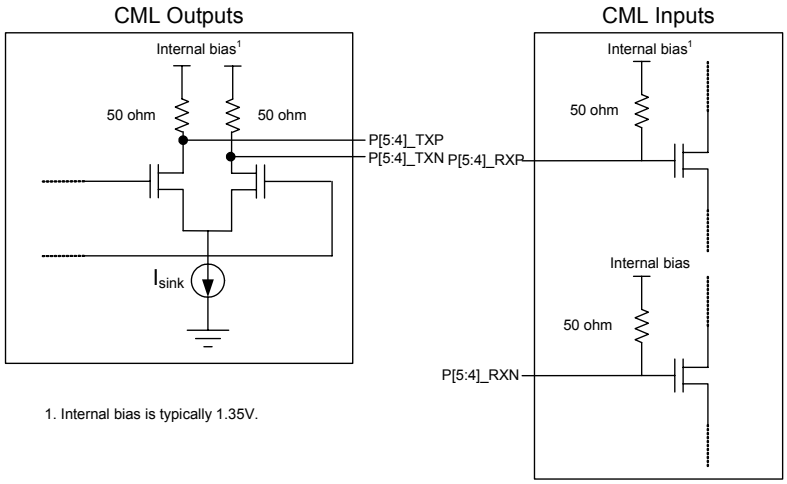
Symbol	Parameter	Min	Typ	Max	Units
V_{OH}	Output Voltage High			1625	mV
V_{OL}	Output Voltage Low	875			mV
V_{RING}	Output Ringing			10	mV
$\|V_{OD}\|$[1]	Output Voltage Swing (differential, peak)	Programmable - see Table 24.			mV peak
V_{OS}	Output Offset Voltage (also called Common mode voltage)	Variable - see 3.5.2.2 for details.			mV
R_O	Output Impedance (single-ended) (50 ohm termination)	40		60	Ω
Delta R_O	Mismatch in a pair			10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1			25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1			25	mV
I_{S+}, I_{S-}	Output current on short to VSS			40	mA
I_{S+-}	Output current when P[5:4]_TXP and P[5:4]_TXN are shorted			12	mA
I_{X+}, I_{X-}	Power off leakage current			10	mA

1. Output amplitude is programmable by writing to SERDES Register 26.2:0.

Table 24: Programming SGMII Output Amplitude

SERDES Register 26 Bits	Field	Description
2:0	SERDES Interface Output Amplitude (100 ohm differential load)	Differential voltage peak-to-peak measured with 100 ohm differential load. 000 = 14 mV 001 = 112 mV 010 = 210 mV 011 = 308 mV 100 = 406 mV 101 = 504 mV 110 = 602 mV 111 = 700 mV

Figure 13: CML I/Os



1. Internal bias is typically 1.35V.

3.5.2.2 Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII/Fiber interface connections. These are:

- DC connection to an LVDS receiver
- AC connection to an LVDS receiver
- DC connection to an CML receiver
- AC connection to an CML receiver

If AC coupling or DC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- Internal bias. See Figure 13 for details.
- The output voltage swing is programmed by SERDES Register 26.2:0 (see Table 24).

Voffset(i.e., common mode voltage) = internal bias - single-ended peak-peak voltage swing. See Figure 14 for details.

If DC coupling is used with a CML receiver, then the DC levels will be determined by a combination of the MACs output structure and the 88E6165 device input structure shown in the CML Inputs diagram in Figure 15. Assuming the same MAC CML voltage levels and structure, the common mode output levels will be determined by:

Voffset(i.e., common mode voltage) = internal bias - single-ended peak-peak voltage swing/2. See Figure 15 for details.

If DC coupling is used, the output voltage DC levels are determined by the AC coupling considerations above, plus the I/O buffer structure of the MAC.

Figure 14: AC connections (CML or LVDS receiver) or DC connection LVDS receiver

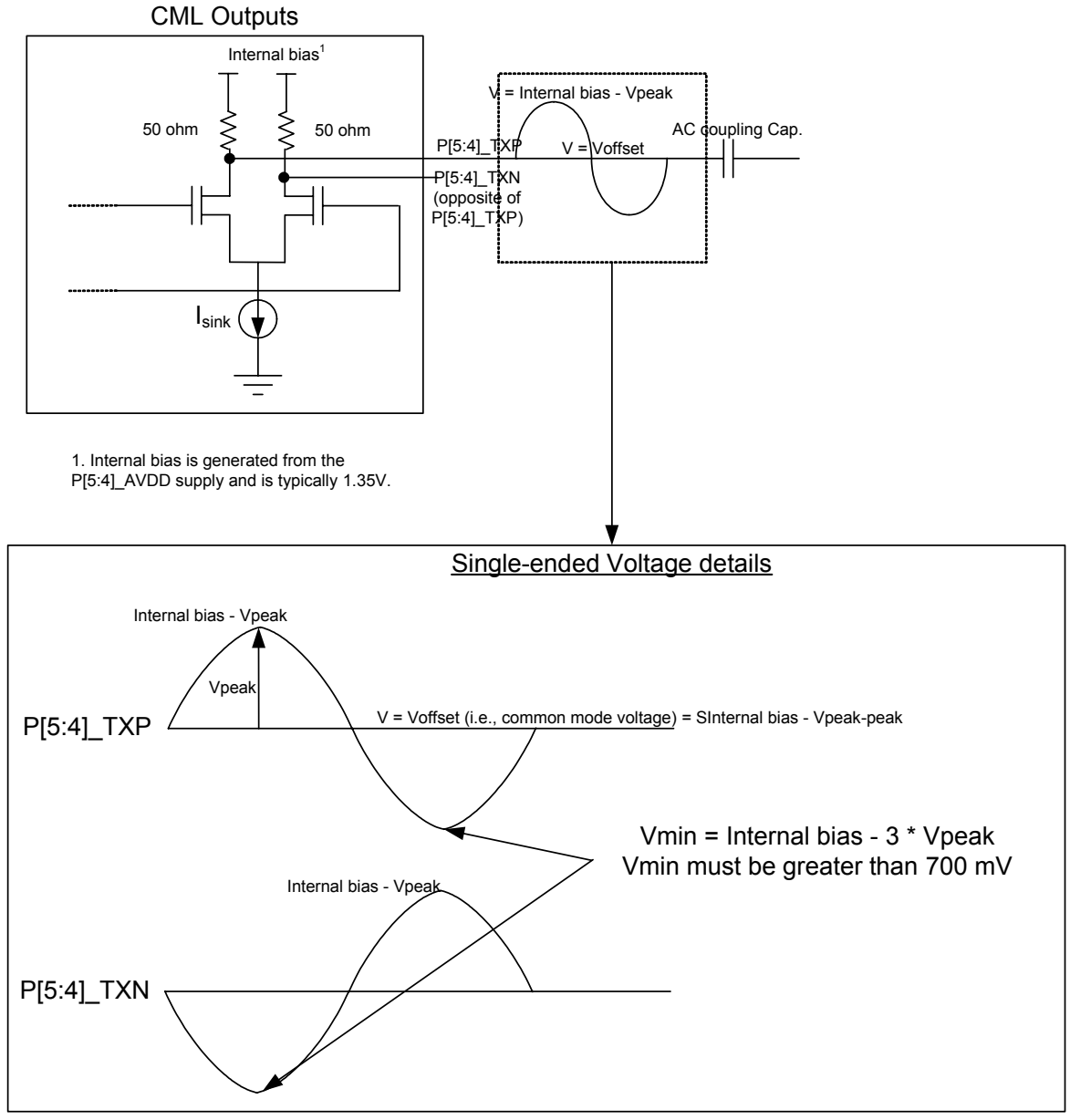
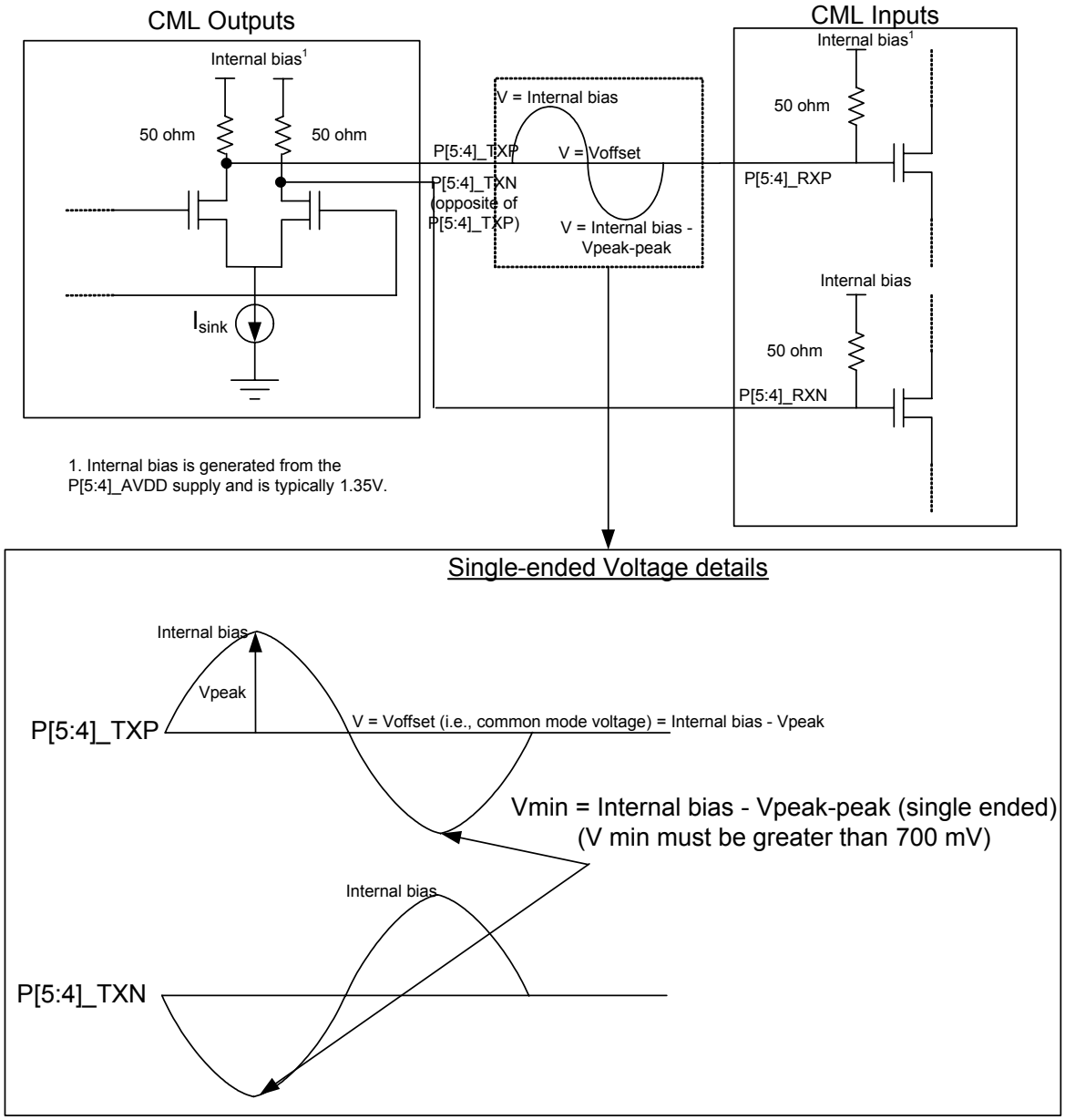


Figure 15: DC connection to a CML receiver

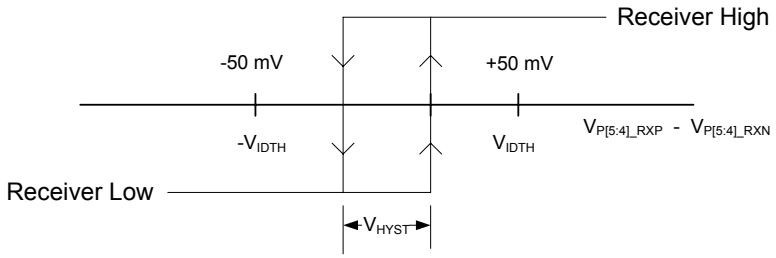


3.5.2.3 Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_I	Input DC Voltage range P[5:4]_RXP or P[5:4]_RXN	675		1725	mV
V_{IDTH}[1]	Input Differential Threshold |P[5:4]_RXP - P[5:4]_RXN|	200		2100	mV (peak-peak differential)
V_{HYST}[1]	Input Differential Hysteresis	25			mV
R_{IN}	Receiver 100 ohm Differential Input Impedance	80		120	ohm

1. Receiver is at high level when VP[5:4]_RXP - VP[5:4]_RXN is greater than VIDTH (min) and is at low level when VP[5:4]_RXP - VP[5:4]_RXN is less than -VIDTH (min). A minimum hysteresis of VHYST is present between -VIDTH and +VIDTH as shown in the figure. When the fiber link is down, an offset is applied to prevent false signal detect due to noise. When the fiber link is up, the offset circuit is disabled.

Figure 16: Input Differential Hysteresis



3.5.3 IEEE DC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications:

-10BASE-T IEEE 802.3 Clause 14

-100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 25: IEEE DC Transceiver Parameters

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V_{ODIFF}	Absolute peak differential output voltage	TXP/N [5:4]	10BASE-T no cable	2.2	2.5	2.8	V
		TXP/N [5:4]	10BASE-T cable model	585[1]			mV
		TXP/N [5:4]	100BASE-FX mode	0.4	0.8	1.2	V
		TXP/N [5:4]	100BASE-TX mode	0.950	1.0	1.05	V
	Overshoot[2]	TXP/N [5:4]	100BASE-TX mode	0		5%	V
	Amplitude Symmetry (positive/ negative)	TXP/N [5:4]	100BASE-TX mode	0.98x		1.02x	V+/V-
V_{IDIFF}	Peak Differential Input Voltage accept level	RXP/N [5:4]	10BASE-T mode	585[3]			mV
		RXP/N[4] P[4]_SDET	100BASE-FX mode	200			mV
	Signal Detect Assertion	RXP/N[4]	100BASE-TX mode	1000	460[4]		mV peak-peak
	Signal Detect De-assertion	RXP/N[4]	100BASE-TX mode	200	360[5]		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. ANSI X3.263-1995 Figure 9-1.
3. The input test is actually a template test. IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The devices will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should be de-assert signal detect (internal signal in 100BASE-TX mode). The devices will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

3.6 AC Electrical Specifications

3.6.1 Receiver AC Characteristics

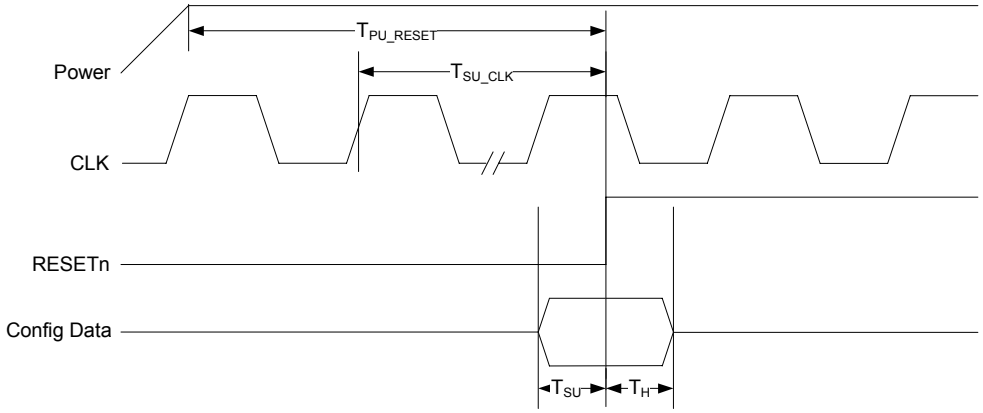
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Table 26: Reset and Configuration Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted or RESETn assertion time	At power up or sub-sequent resets after power up	10			ms
T_{SU_CLK}	Number of valid REFCLK cycles prior to RESETn de-asserted		10			Clks
T_{SU}	Configuration data valid prior to RESETn de-asserted[1]		200			ns
T_{HD}	Config data valid after RESETn de-asserted		0			ns

1. When RESETn is low all configuration pins become inputs, and the value seen on these pins is latched on the rising edge of RESETn. All configuration pins that become outputs during normal operation will remain tri-stated for 40 ns after the rising edge of RESETn.

Figure 17: Reset and Configuration Timing



3.6.2 Clock Timing

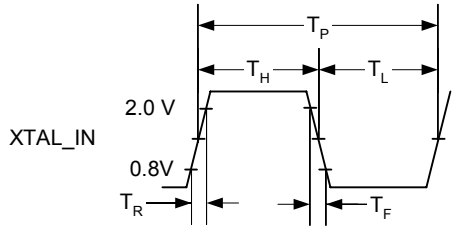
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Table 27: Clock Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P[1]	XTAL_IN period		40 -50 ppm	40	40 +50 ppm	ns
T_H	XTAL_IN high time		16			ns
T_L	XTAL_IN low time		16			ns
T_R	XTAL_IN rise				3	ns
T_F	XTAL_IN fall				3	ns

1. 25.000 MHz

Figure 18: Oscillator Clock Timing



3.7 GMII Timing

3.7.1 GMII Transmit Timing

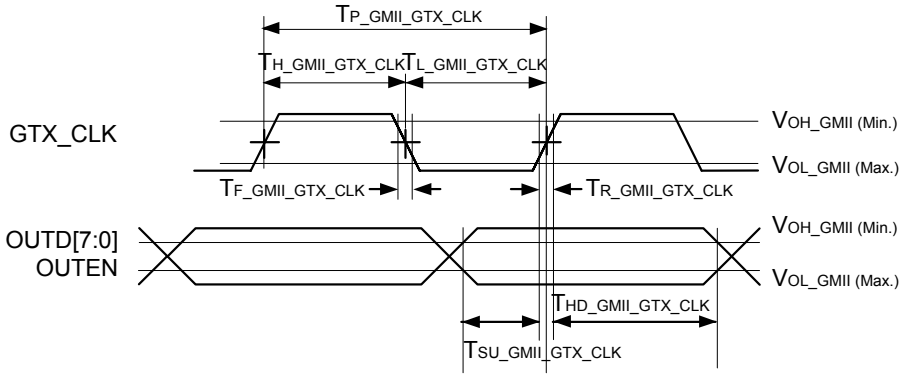
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 28: GMII Transmit Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_GMII\_GTX\_CLK}$	GMII output to clock		2.5			ns
$T_{HD\_GMII\_GTX\_CLK}$	GMII clock to output		0.5			ns
$T_{H\_GMII\_GTX\_CLK}$	GTX_CLK High		2.5[1]		5.5	ns
$T_{L\_GMII\_GTX\_CLK}$	GTX_CLK Low		2.5[1]		5.5	ns
$T_{P\_GMII\_GTX\_CLK}$	GTX_CLK Period		7.5[1]	8.0		ns
$T_{R\_GMII\_GTX\_CLK}$	GTX_CLK Rise Time				1.0	ns
$T_{F\_GMII\_GTX\_CLK}$	GTX_CLK Fall Time				1.0	ns
$T_{RSLEW\_GMII\_GTX\_CLK}$	GTX_CLK Rising Slew Rate		0.6[2]			V/ns
$T_{FSLEW\_GMII\_GTX\_CLK}$	GTX_CLK Falling Slew Rate		0.6[2]			V/ns

1. GTX_CLK numbers not guaranteed during transition between 10/100/1000BASE-T operation.
2. Instantaneous change during internal VIH_GMII (Min.) and VIL_GMII (Max.).

Figure 19: GMII Transmit Timing



3.7.2 GMII Receive Timing

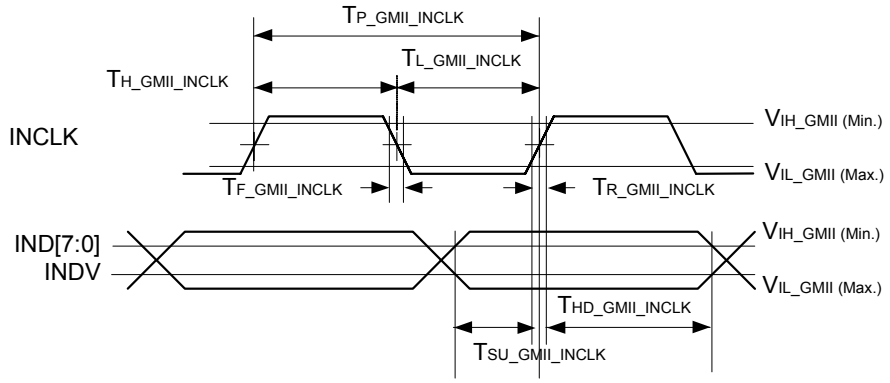
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 29: GMII Receive Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{SU\_GMII\_INCLK}$	GMII Setup Time		2.0			ns
$T_{HD\_GMII\_INCLK}$	GMII Hold Time		0			ns
$T_{H\_GMII\_INCLK}$	INCLK High		2.5[1]			ns
$T_{L\_GMII\_INCLK}$	INCLK Low		2.5[1]			ns
$T_{P\_GMII\_INCLK}$	INCLK Period		7.5[1]	8.0	8.5	ns
F_{GMII_INCLK}	INCLK Frequency		125[1] -100 ppm		125 +100 ppm	MHz
$T_{R\_GMII\_INCLK}$	INCLK Rise Time				1.0	ns
$T_{F\_GMII\_INCLK}$	INCLK Fall Time				1.0	ns

1. RX_CLK toggle rate is “don’t care” if link is down, or if not in 1000BASE-T mode.

Figure 20: GMII Receive Timing



3.8 RGMII Timing

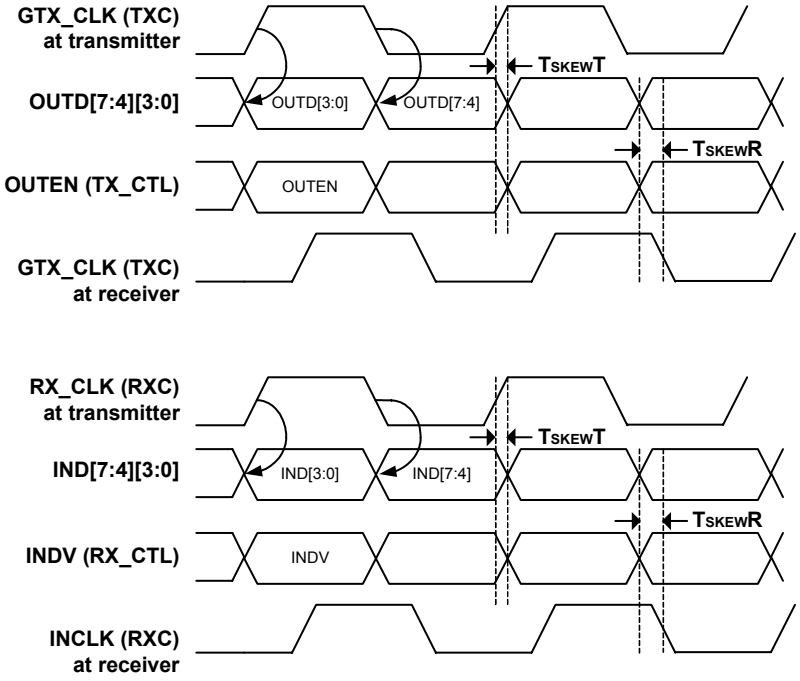
Table 30: RGMII Interface Timing

(For other timing modes see Section 3.8.1 "RGMII Timing for Different RGMII Modes" on page 77.)

Symbol	Parameter	Min	Typ	Max	Units
TskewT	Data to Clock output Skew (at transmitter)	-500	0	500	ps
TskewR	Data to Clock input Skew (at receiver)	1.0	-	2.6	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH1000}$	High Time for 1000BASE-T [1]	3.6	4.0	4.4	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20-80%)			0.75	ns

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three TCYCLE of the lowest speed transitioned between.

Figure 21: RGMII Multiplexing and Timing



3.8.1 RGMII Timing for Different RGMII Modes

The RGMII Timing Control register is an indirect access register. See 88E6165 Datasheet, Part 2 - Switch Core, "Indirect Access Registers" for details.

3.8.1.1 RGMII Transmit Timing

Table 31: Transmit - GTXCLK (TXC) Timing when RGMII Transmit Delay Control (bit 3) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{sskew}	RGMII Transmit Delay Control (bit 3) = 0	-0.5		0.5	ns

Figure 22: Transmit - GTXCLK (TXC) Timing when RGMII Transmit Delay Control (bit 3) = 0

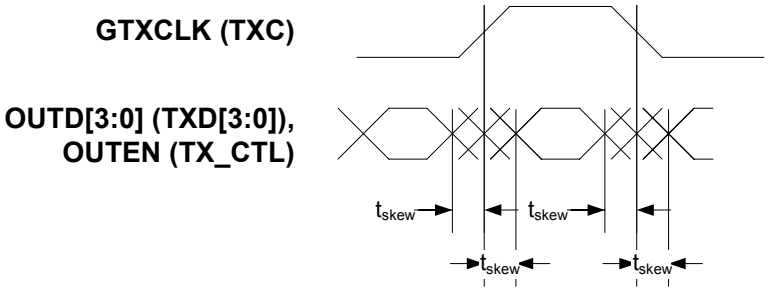
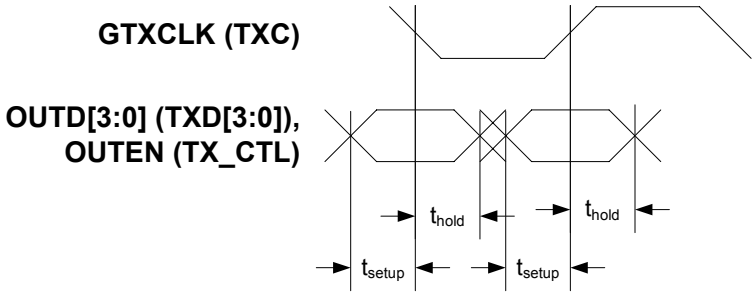


Table 32: Transmit - GTXCLK (TXC) Timing when RGMII Transmit Delay Control (bit 3) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Transmit Delay Control (bit 3) = 1	1.2			ns
t_{hold}		1.0			ns

Figure 23: Transmit - GTXCLK (TXC) Timing when RGMII Transmit Delay Control (bit 3) = 1



3.8.1.2 RGMII Receive Timing

Table 33: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (bit 4) = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 0	1.0			ns
t_{hold}		0.8			ns

Figure 24: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (bit 4) = 0

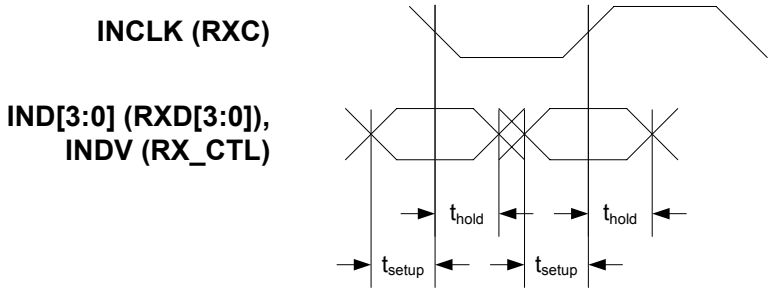
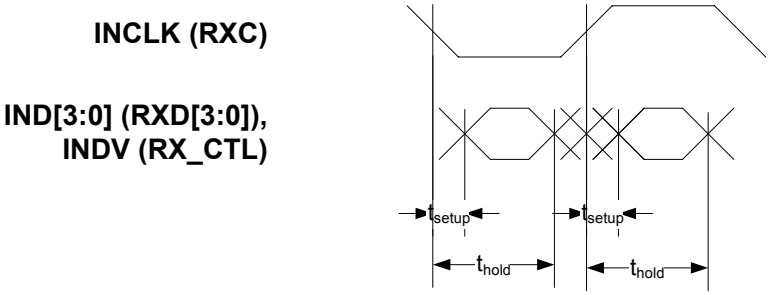


Table 34: Receive - INCLK (RXC) Timing when RGMII Receive Delay Control (bit 4) = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units
t_{setup}	RGMII Receive Delay Control (bit 4) = 1	-0.9			ns
t_{hold}		2.7			ns

Figure 25: Receive - RXC Timing when RGMII Receive Delay Control (bit 4) = 1



3.9 MII Timing

3.9.1 MII MAC Mode Clock Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

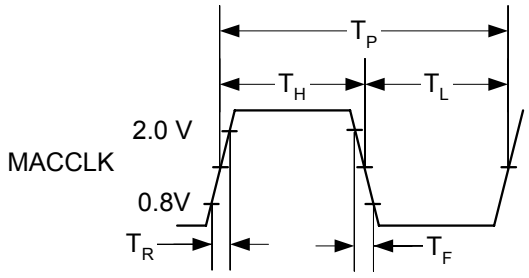
In MII MAC mode, the Px_INCLK and Px_OUTCLK pins are inputs.

Table 35: MII MAC Mode Clock Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	MACCLK_IN period		20[1]	40 or 400		ns
T_H	MACCLK_IN high time		8			ns
T_L	MACCLK_IN low time		8			ns
T_R	MACCLK_IN rise				3	ns
T_F	MACCLK_IN fall				3	ns

1. This value applies for 200 Mbps mode

Figure 26: MAC Clock Timing



3.9.2 MII Receive Timing - MAC Mode

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

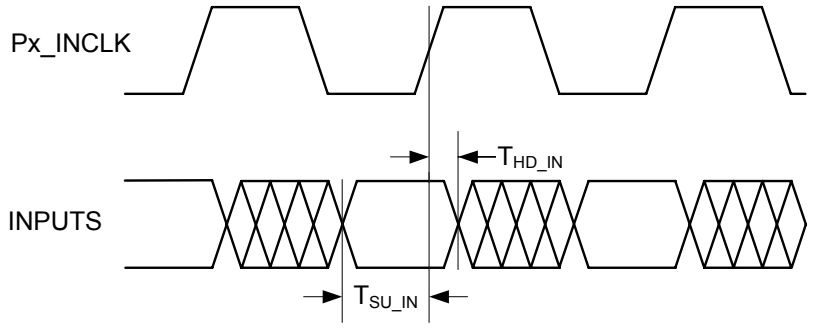
Table 36: MII Receive Timing—MAC Mode 100 Mbps Operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_IN}	MII inputs (Px_IND[3:0] and Px_INDV) valid prior to Px_INCLK going high	With 10 pF load	10			ns
T_{HD_IN}	MII inputs (Px_IND[3:0] and Px_INDV) valid after Px_INCLK going high	With 10pF load	10			ns

Table 37: MII Receive Timing—MAC Mode 200 Mbps Operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{SU_IN}	MII inputs (Px_IND[3:0] and Px_INDV) valid prior to Px_INCLK going high	With 10 pF load	5			ns
T_{HD_IN}	MII inputs (Px_IND[3:0] and Px_INDV) valid after Px_INCLK going high	With 10pF load	2			ns

Figure 27: MAC Mode MII Receive Timing



3.9.3 MII Transmit Timing - MAC Mode

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 38: MII Transmit Timing—MAC Mode 100 Mbps Operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{OUTCLK}	Px_OUTCLK period	10BASE mode[1]		400		ns
		100BASE mode		40		ns
T_{H_OUTCLK}	Px_OUTCLK high	10BASE mode		200		ns
		100BASE mode		20		ns
T_{L_OUTCLK}	Px_OUTCLK low	10BASE mode		200		ns
		100BASE mode		20		ns
T_{CQ_MAX}	Px_OUTCLK to outputs (Px_OUTD[3:0], Px_OUTEN) valid	With 10 pF load			25	ns
T_{CQ_MIN}	Px_OUTCLK to outputs Px_OUTD[3:0], Px_OUTEN) invalid	With 10 pF load	0			ns

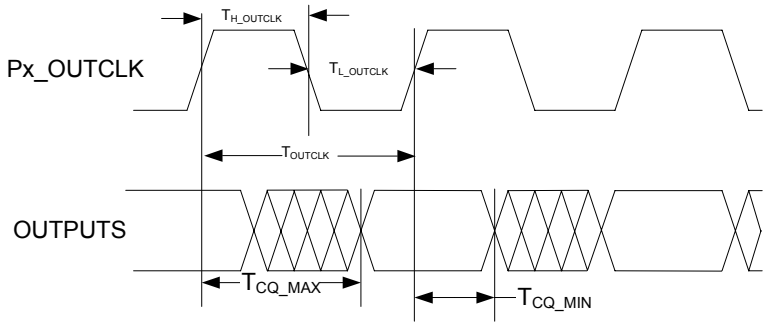
1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps

Table 39: MII Transmit Timing—MAC Mode 200 Mbps Operation

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{OUTCLK}	Px_OUTCLK period	200 Mbps Operation mode[1]		20		ns
T_{H_OUTCLK}	Px_OUTCLK high	200 Mbps Operation		10		ns
T_{L_OUTCLK}	Px_OUTCLK low	200 Mbps Operation		10		ns
T_{CQ_MAX}	Px_OUTCLK to outputs (Px_OUTD[3:0], Px_OUTEN) valid	With 10 pF load			15	ns
T_{CQ_MIN}	Px_OUTCLK to outputs Px_OUTD[3:0], Px_OUTEN) invalid	With 10 pF load	3			ns

1. 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps

Figure 28: MAC Mode MII Transmit Timing



3.10 Serial Management Interface (SMI) Timing

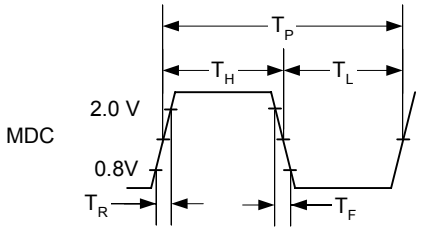
3.10.1 SMI Clock Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 40: SMI Clock Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		120			ns	8.33 MHz
T_H	MDC high time		48			ns	
T_L	MDC low time		48			ns	
T_R	MDC rise				6	ns	
T_F	MDC fall				6	ns	

Figure 29: SMI Clock Timing (CPU Set)



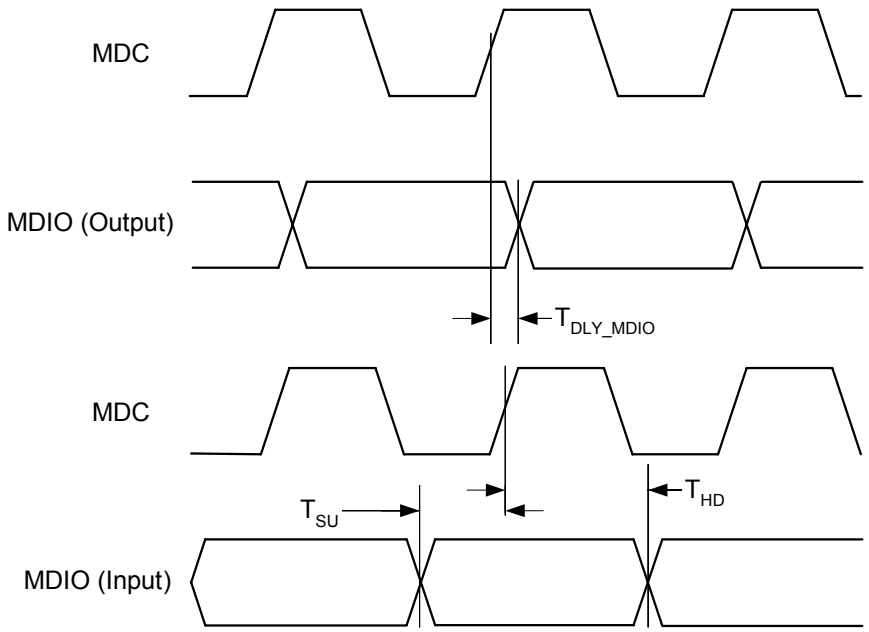
3.10.2 SMI Data Timing (CPU Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 41: SMI Data Timing (CPU Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		30	ns	
T_{SU}	MDIO (Input) to MDC setup time		10			ns	
T_{HD}	MDIO (Input) to MDC hold time		10			ns	

Figure 30: SMI Data Timing



3.10.3 SMI Timing (PHY Set)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 42: SMI Timing (PHY Set)

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	MDC period		120[1]			ns	8.33 MHz
T_H	MDC high time		48			ns	
T_L	MDC low time		48			ns	
T_R	MDC rise				6	ns	
T_F	MDC fall				6	ns	
T_{SU}	MDIO setup time		- 12.5			ns	2
T_{HD}	MDIO hold time		0		12.5	ns	2
T_{DLY_MDIO}	MDC to MDIO (Output) delay time		0		5	ns	3

1. MDC_PHY will track MDC_CPU when the PPU is disabled. When the PPU is enabled the MDC_PHY period will be 240 ns.
2. MDIO input setup and hold time is intentionally sampled with respect to the MDC falling edge.
3. MDIO data is intentionally clocked out on the falling edge of MDC.

Figure 31: SMI Timing Output (PHY Mode)

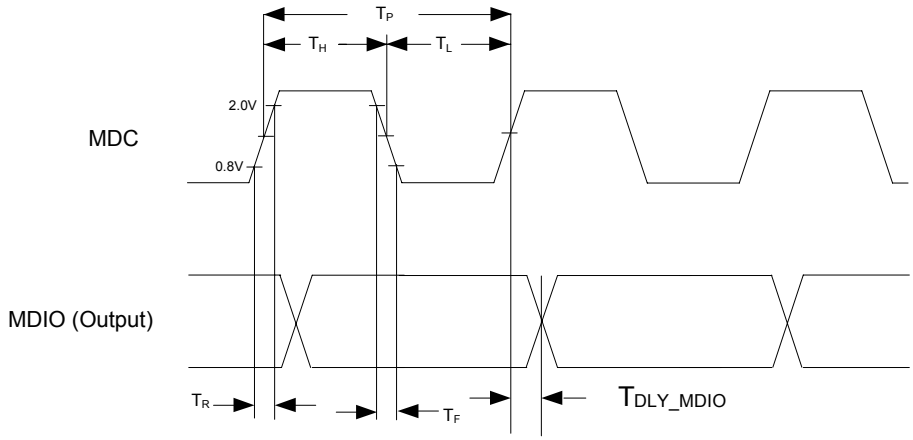
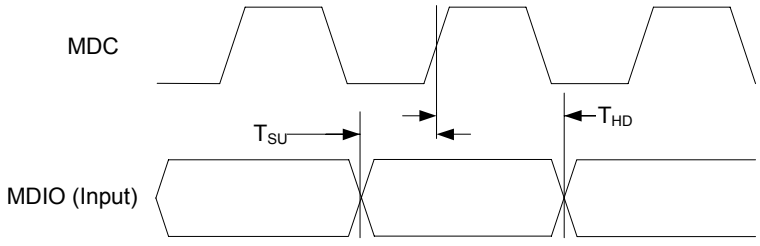


Figure 32: SMI Timing Input (PHY Mode)



3.11 EEPROM Timing

3.11.1 2-Wire EEPROM Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 43: 2-Wire EEPROM Input Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	EE_CLK period			19200		ns
T_H	EE_CLK high time			9600		ns
T_L	EE_CLK low time			9600		ns
T_{IN}	EE_CLK input time		50		4500	ns

Figure 33: 2-Wire Input Timing

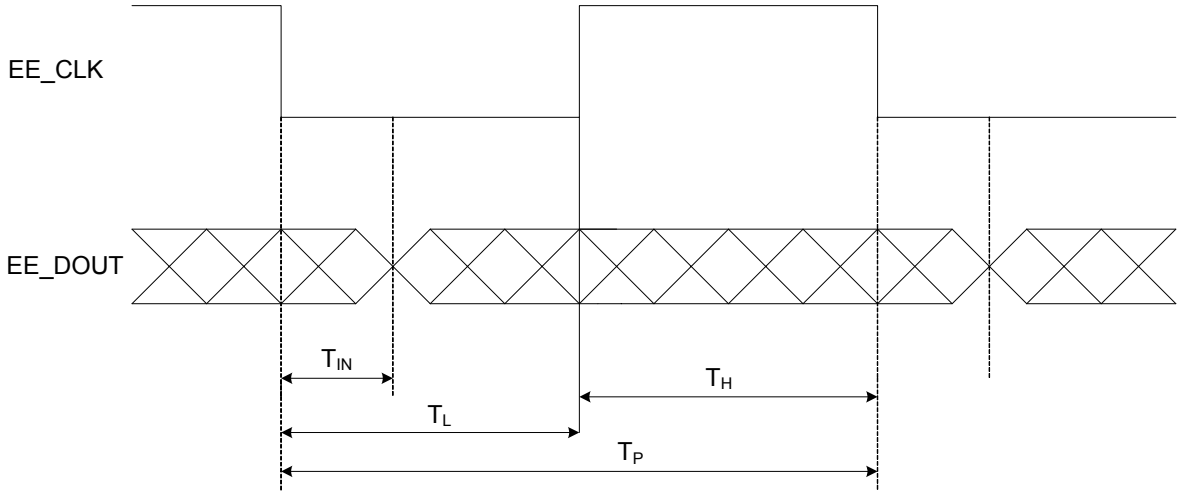
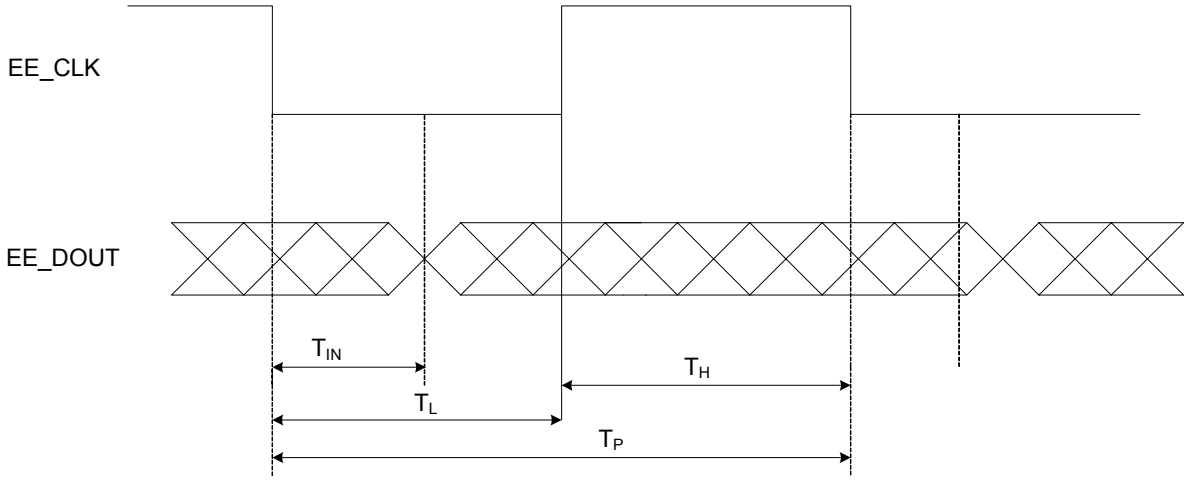


Table 44: 2-Wire EEPROM Output Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_P	EE_CLK period			19200		ns
T_H	EE_CLK high time			9600		ns
T_L	EE_CLK low time			9600		ns
T_{IN}	EE_CLK output time		0		9800	ns

Figure 34: 2-Wire Output Timing



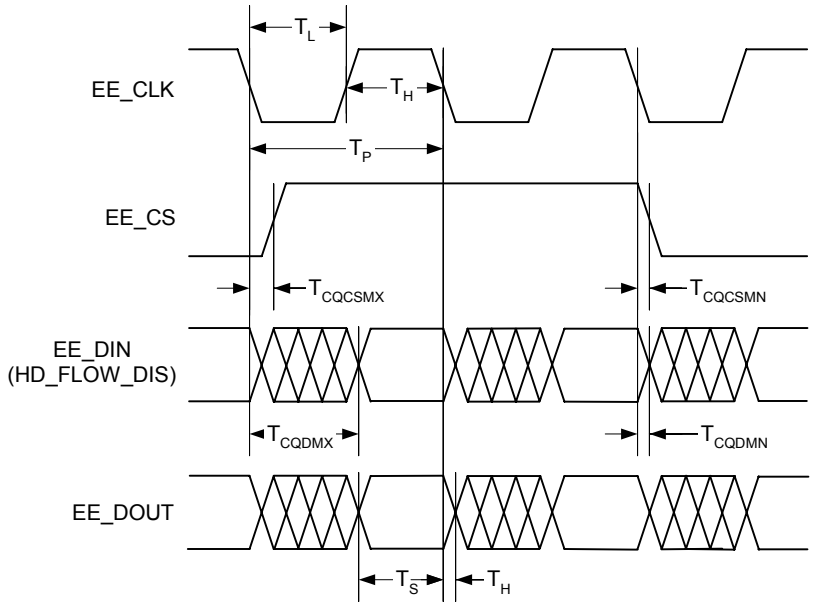
3.11.2 4-Wire EEPROM Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 45: 4-Wire EEPROM Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T_P	EE_CLK period			9600		ns	
T_H	EE_CLK high time			4800		ns	
T_L	EE_CLK low time			4800		ns	
T_{CQCSMX}	Serial EEPROM chip select valid	Referenced to EE_CLK			5	ns	
T_{CQCSMN}	Serial EEPROM chip select invalid				5	ns	
T_{CQDMX}	Serial EEPROM data transmitted to EEPROM valid				10	ns	
T_{CQDMN}	Serial EEPROM data transmitted to EEPROM invalid		3			ns	
T_S	Setup time for data received from EEPROM		10			ns	
T_H	Hold time for data received from EEPROM		10			ns	

Figure 35: 4-Wire EEPROM Timing



3.12 SERDES (Serial Interface) Timing

Table 46: SERDES (Serial Interface) Transmitter AC Characteristics

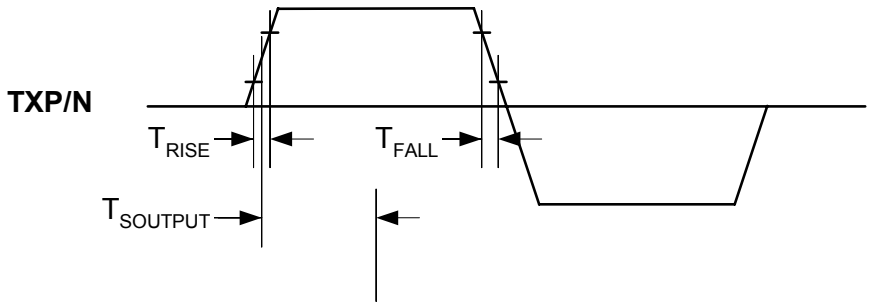
Symbol	Parameter	Min	Typ	Max	Units
CLOCK	Clock signal duty cycle @ 125 MHz	45		55	%
T_{FALL}	V_{OD} Fall time (20% - 80%)	80		200	ps
T_{RISE}	V_{OD} Rise time (20% - 80%)	80		200	ps

Table 47: SERDES (Serial Interface) Receiver AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
$T_{SOUTPUT}$[1]	SERDES output	360	400	440	ps

1. Measured at 50% of the transition.

Figure 36: SERDES Rise and Fall Times



3.13 IEEE AC Parameters (Port 4 and Port 5)

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:

-10BASE-T IEEE 802.3 Clause 14-2000

-100BASE-TX ANSI X3.263-1995

-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Table 48: IEEE AC Parameters

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	TXP/N[5:4]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall time	TXP/N[5:4]	100BASE-TX	3.0	4.0	5.0	ns
T_{RISE}/ T_{FALL} Symmetry		TXP/N[5:4]	100BASE-TX	0		0.5	ns
DCD	Duty cycle distortion	TXP/N[5:4]	100BASE-TX	0		0.5[1]	ns, peak-peak
Transmit Jitter		TXP/N[5:4]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Table 3.

Section 4 Package Mechanical Dimensions

Figure 37: 216-pin LQFP EPAD Package Mechanical Drawings

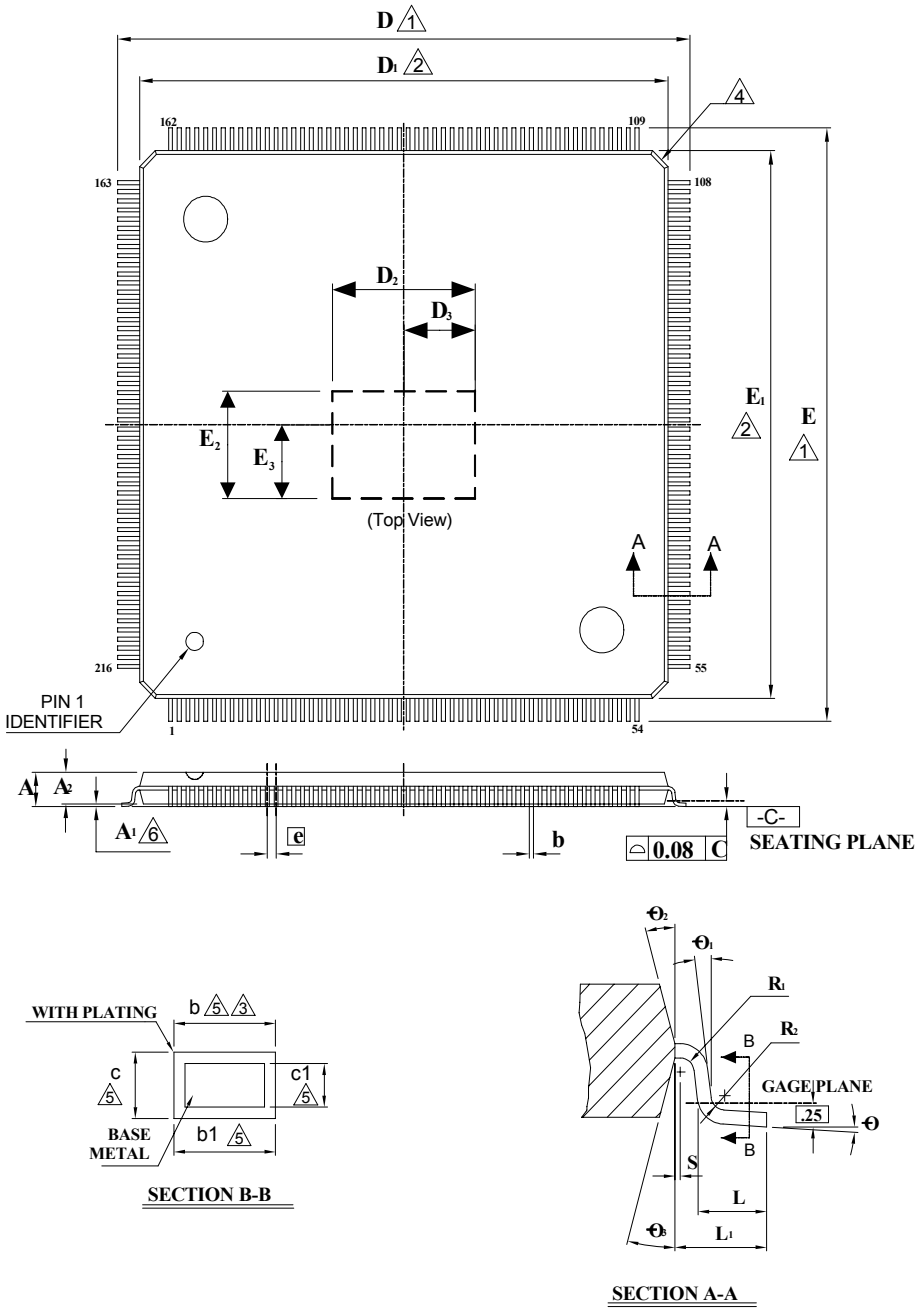


Table 49: 216-pin LQFP EPAD Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	--	--	1.60
A_1	0.05	--	0.15
A_2	1.35	1.40	1.45
b	0.13	0.18	0.23
b_1	0.13	0.16	0.19
c	0.09	0.14	0.20
c_1	0.09	0.12	0.16
D	25.85	26.00	26.15
D_1	23.90	24.00	24.10
E	25.85	26.00	26.15
E_1	23.90	24.00	24.10
e	0.40 BSC		
L	0.45	0.60	0.75
L_1	1.00 REF		
R_1	0.08	--	--
R_2	0.08	--	--
S	0.20	--	--
θ	0°	3.5°	7°
θ_1	0°	--	--
θ_2	11°	12°	13°
θ_3	11°	12°	13°

Exposed Pad Size (mm)			
D_2	D_3	E_2	E_3
8.26	4.13	6.10	4.45

Notes:

1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION: MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026

Section 5 Ordering Information

5.1 Ordering Part Numbers and Package Markings

Figure 38 shows the ordering part numbering scheme for the devices. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 38: Sample Part Number

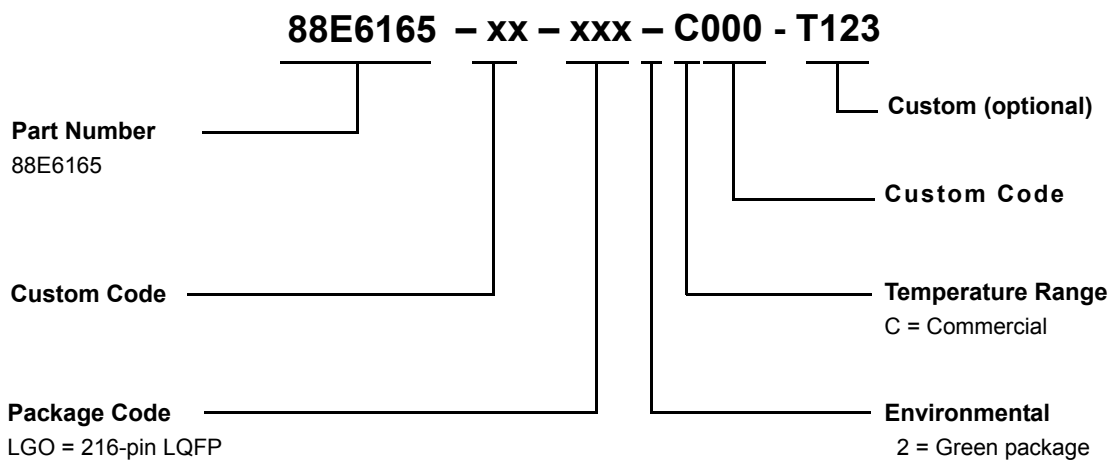
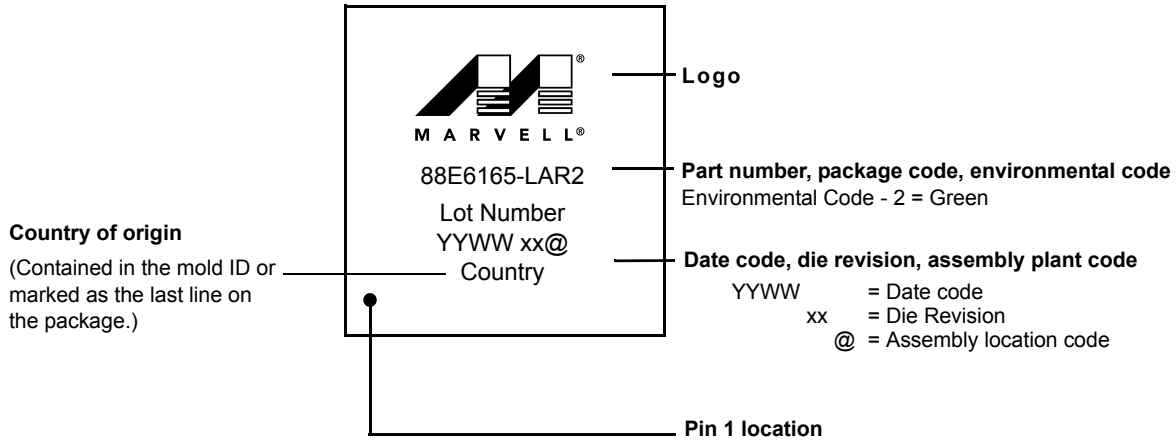


Table 50: Part Order Options - Commercial

Package Type	Part Order Number
88E6165 216-pin LQFP - Commercial - Green	88E6165-xx-LGO2C000

Figure 39 is an example of the package marking and pin 1 location for the 88E6165 216-pin LQFP Commercial green package.

Figure 39: 88E6165 216-pin LQFP Commercial Green Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

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