Ultralow Noise, 150 mA CMOS Linear Regulator

Data Sheet **ADP150**

FEATURES

- Ultra low noise: 9 µV rms, independent of V_{OUT}
- No additional noise bypass capacitor required
- Stable with 1 µF ceramic input and output capacitors
- Maximum output current: 150 mA
- Input voltage range: 2.2 V to 5.5 V
- Low quiescent current
  - I_{GND} = 10 µA with zero load
- Low shutdown current: <1 µA
- Low dropout voltage: 105 mV @ 150 mA load
- Initial output voltage accuracy: ±1%
- Up to 14 fixed output voltage options: 1.8 V to 3.3 V
- PSRR performance of 70 dB at 10 kHz
- Current limit and thermal overload protection
- Logic-controlled enable
- 5-lead TSOT package
- 4-ball, 0.8 mm × 0.8 mm, 0.4 mm pitch WLCSP

TYPICAL APPLICATION CIRCUITS

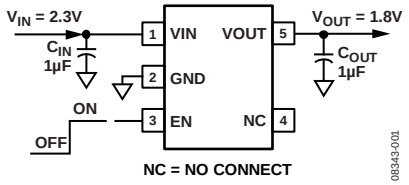

Figure 1. 5-Lead TSOT with Fixed Output Voltage, 1.8 V

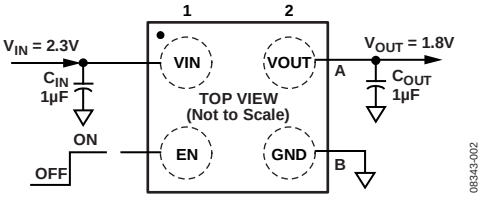

Figure 2. 4-Ball WLCSP with Fixed Output Voltage, 1.8 V

APPLICATIONS

- Mobile phones
- Digital camera and audio devices
- Portable and battery-powered equipment
- Post dc-to-dc regulation
- Portable medical devices
- RF, PLL, VCO, and clock power supplies

GENERAL DESCRIPTION

The ADP150 is an ultralow noise (9 µV), low dropout, linear regulator that operates from 2.2 V to 5.5 V and provides up to 150 mA of output current. The low 105 mV dropout voltage at 150 mA load improves efficiency and allows operation over a wide input voltage range.

Using an innovative circuit topology, the ADP150 achieves ultralow noise performance without the necessity of an additional noise bypass capacitor, making it ideal for noise sensitive analog and RF applications. The ADP150 also achieves ultralow noise performance without compromising PSRR or line and load transient performance. The ADP150 offers the best combination of ultralow noise and quiescent current consumption to maximize battery life in portable applications.

The ADP150 is specifically designed for stable operation with tiny 1 µF ± 30% ceramic input and output capacitors to meet the requirements of high performance, space-constrained applications.

The ADP150 is available in 14 fixed output voltage options, ranging from 1.8 V to 3.3 V.

Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADP150 is available in tiny 5-lead TSOT and 4-ball, 0.4 mm pitch WLCSP packages for the smallest footprint solution to meet a variety of portable power applications.

Rev. B

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10/09—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.4 V) or 2.2 V, whichever is greater; EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.2		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		10		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			22	µA
		I_{OUT} = 100 µA		20		µA
		I_{OUT} = 100 µA, T_J = −40°C to +125°C			40	µA
		I_{OUT} = 10 mA		60		µA
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			100	µA
		I_{OUT} = 150 mA		220		µA
		I_{OUT} = 150 mA, T_J = −40°C to +125°C			320	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		0.2		µA
		EN = GND, T_J = −40°C to +125°C			1.0	µA
OUTPUT VOLTAGE ACCURACY						
5-Lead TSOT	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		100 µA < I_{OUT} < 150 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V, T_J = −40°C to +125°C	−2.5		+1.5	%
4-Ball WLCSP	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		100 µA < I_{OUT} < 150 mA, V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V, T_J = −40°C to +125°C	−2.0		+1.5	%
REGULATION						
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4 V) to 5.5 V, T_J = −40°C to +125°C	−0.05		+0.05	%/V
Load Regulation[1]						
5-Lead TSOT	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100 µA to 150 mA		0.003		%/mA
		I_{OUT} = 100 µA to 150 mA, T_J = −40°C to +125°C			0.0075	%/mA
4-Ball WLCSP	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100 µA to 150 mA		0.002		%/mA
		I_{OUT} = 100 µA to 150 mA, T_J = −40°C to +125°C			0.006	%/mA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	I_{OUT} = 10 mA		10		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			35	mV
		I_{OUT} = 150 mA		105		mV
		I_{OUT} = 150 mA, T_J = −40°C to +125°C			160	mV
START-UP TIME[3]	$T_{START-UP}$	V_{OUT} = 3.3 V		150		µs
CURRENT LIMIT THRESHOLD[4]	I_{LIMIT}		190	260	400	mA
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage Rising	$UVLO_{RISE}$	T_J = −40°C to +125°C			1.96	V
Input Voltage Falling	$UVLO_{FALL}$	T_J = −40°C to +125°C	1.28			V
Hysteresis	$UVLO_{HYS}$	T_J = −40°C to +125°C		115		mV
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
EN INPUT						
EN Input Logic High	V_{IH}	2.2 V ≤ V_{IN} ≤ 5.5 V	1.2			V
EN Input Logic Low	V_{IL}	2.2 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN Input Leakage Current	$V_{I-LEAKAGE}$	EN = IN or GND		0.001		µA
		EN = IN or GND, T_J = −40°C to +125°C			1	µA
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 3.3 V		9		µV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 2.5 V		9		µV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 1.8 V		9		µV rms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO (V_{IN} = V_{OUT} + 0.5 V)	PSRR	10 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		70		dB
		10 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA		70		dB
		100 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		55		dB
		100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA		55		dB
POWER SUPPLY REJECTION RATIO (V_{IN} = V_{OUT} + 1 V)		10 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		70		dB
		100 kHz, V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 10 mA		55		dB

[1] Based on an end-point calculation using 1 mA and 150 mA loads. See Figure 6 for typical load regulation performance for loads less than 1 mA.
[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.2 V.
[3] Start-up time is defined as the time between the rising edges of EN to V_{OUT} being at 90% of its nominal value.
[4] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V or 2.7 V.

RECOMMENDED SPECIFICATIONS: INPUT AND OUTPUT CAPACITOR

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT AND OUTPUT CAPACITOR						
Minimum Input and Output Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C	0.7			µF
Capacitor ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.2	Ω

[1] The minimum input and output capacitance should be greater than 0.7 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R-type and X5R-type capacitors are recommended, and Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +6.5 V
VOUT to GND	−0.3 V to VIN
EN to GND	−0.3 V to +6.5 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Operating Ambient Temperature Range	−40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP150 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) by

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and a calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} can vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inch × 3 inch circuit board. Refer to JESD 51-7 and JESD 51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and a calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) by

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
5-Lead TSOT	170	43	°C/W
4-Ball, 0.4 mm Pitch WLCSP	260	58	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

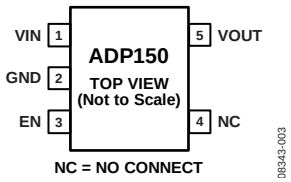

Figure 3. 5-Lead TSOT Pin Configuration

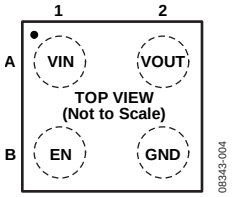

Figure 4. 4-Ball WLCSP Pin Configuration

Table 5. 5-Lead TSOT Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
2	GND	Ground.
3	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
4	NC	No Connect. Not connected internally.
5	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.

Table 6. 4-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
A2	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor.
B1	EN	Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
B2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.7 V, V_{OUT} = 3.3 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

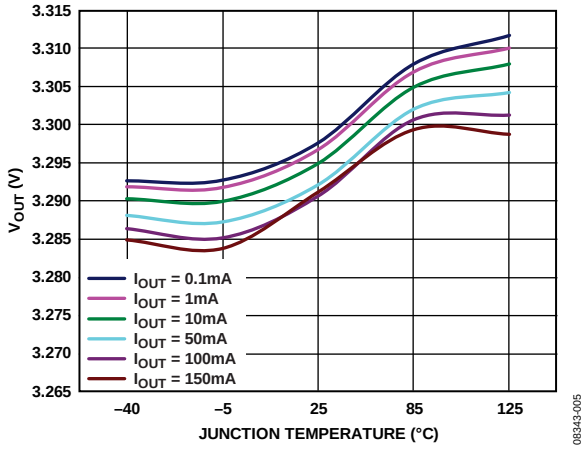

Figure 5. Output Voltage (V_{OUT}) vs. Junction Temperature

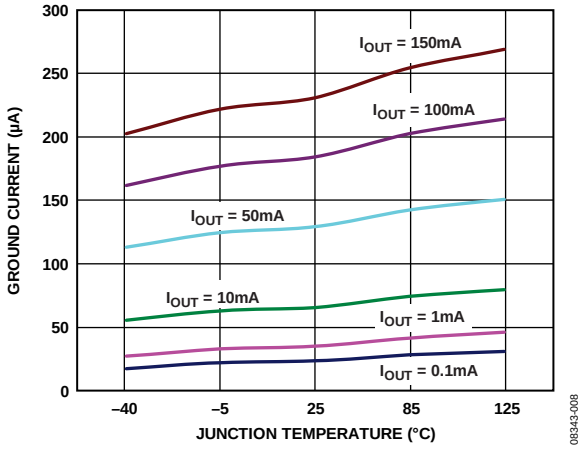

Figure 8. Ground Current vs. Junction Temperature

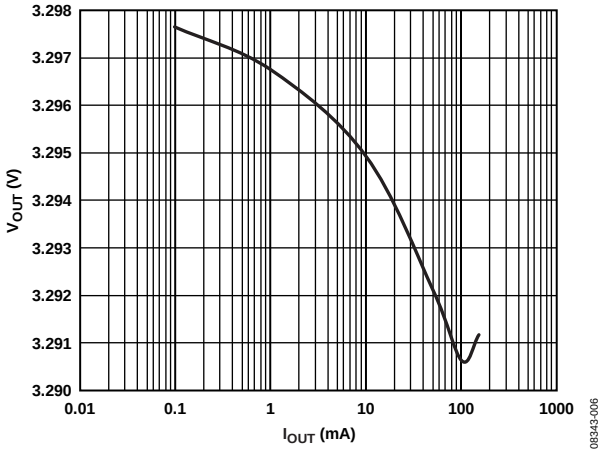

Figure 6. Output Voltage (V_{OUT}) vs. Load Current (I_{OUT})

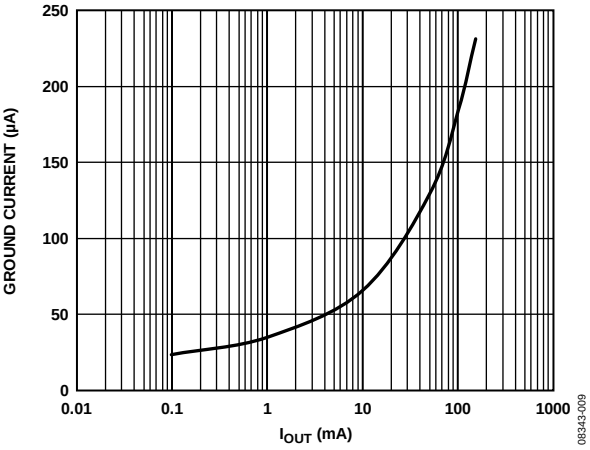

Figure 9. Ground Current vs. Load Current (I_{OUT})

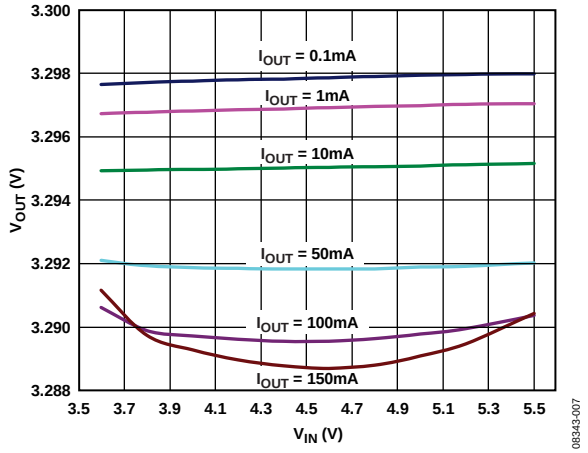

Figure 7. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN})

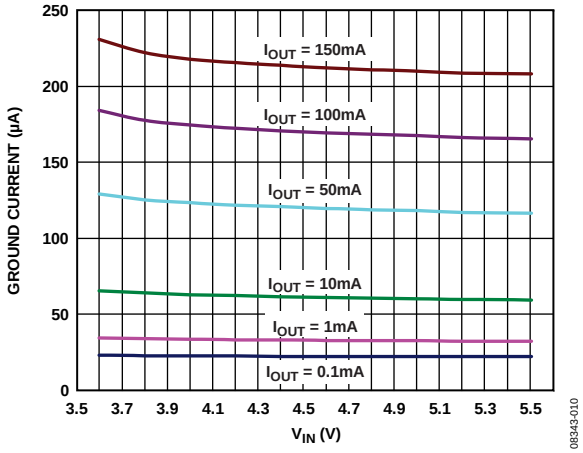

Figure 10. Ground Current vs. Input Voltage (V_{IN})

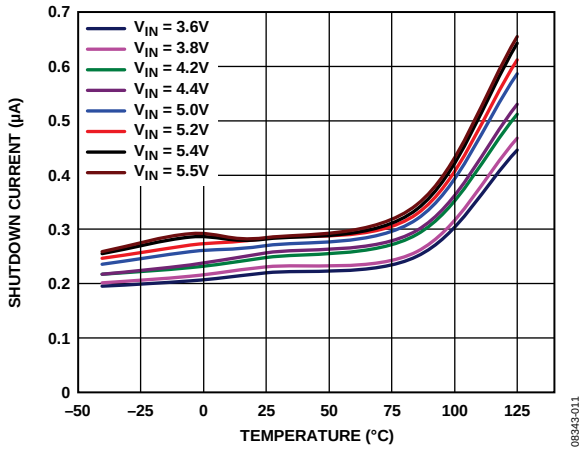

Figure 11. Shutdown Current vs. Temperature at Various Input Voltages

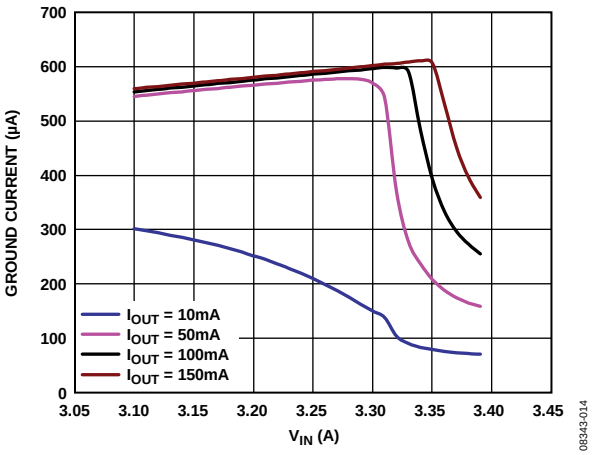

Figure 14. Ground Current vs. Input Voltage (V_{IN}) in Dropout

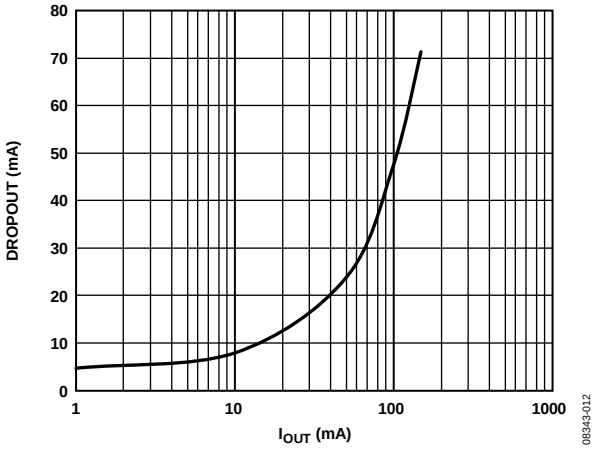

Figure 12. Dropout Voltage vs. Load Current (I_{LOAD})

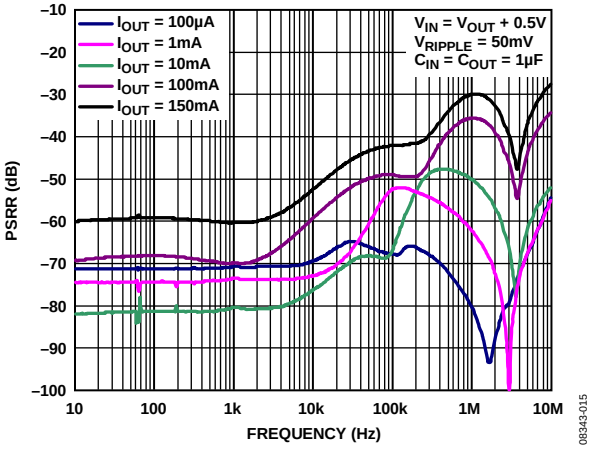

Figure 15. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 1.8 V, V_{IN} = 2.3 V

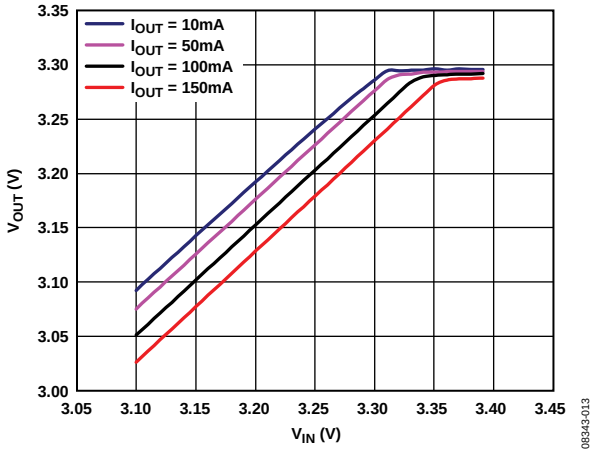

Figure 13. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout

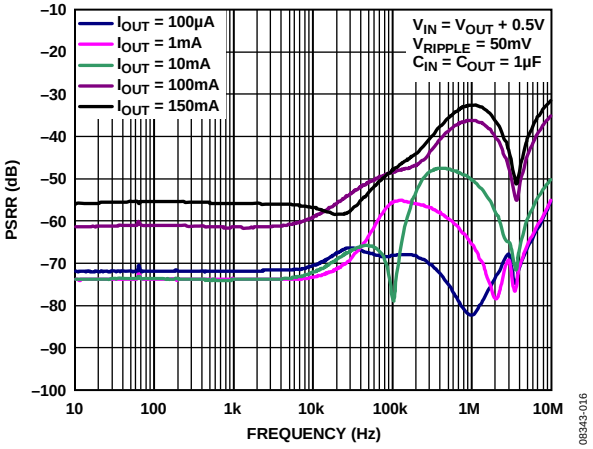

Figure 16. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 2.8 V, V_{IN}=3.3 V

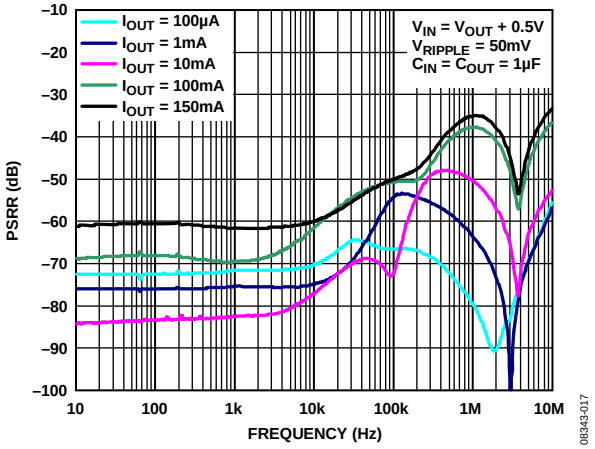

Figure 17. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 3.3 V, V_{IN} = 3.8 V

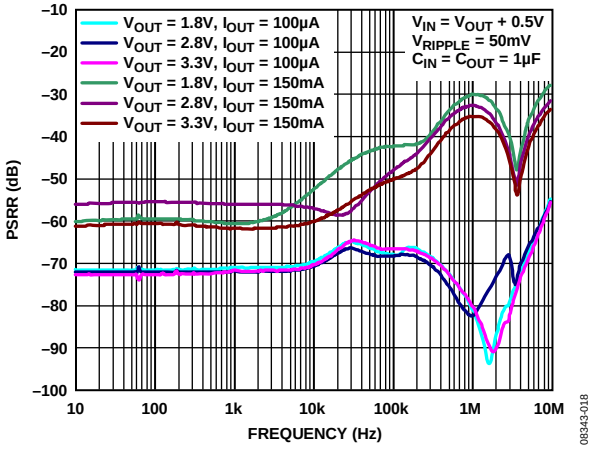

Figure 18. Power Supply Rejection Ratio (PSRR) vs. Frequency Various Output Voltages and Load Currents

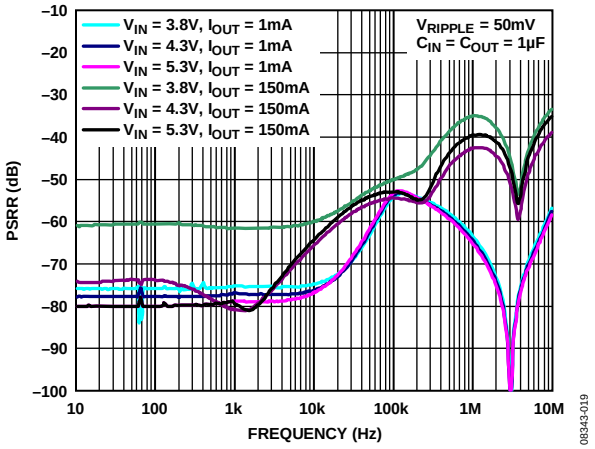

Figure 19. Power Supply Rejection Ratio (PSRR) vs. Frequency with Various Headroom Voltages (V_{IN} – V_{OUT}), V_{OUT} = 3.3 V

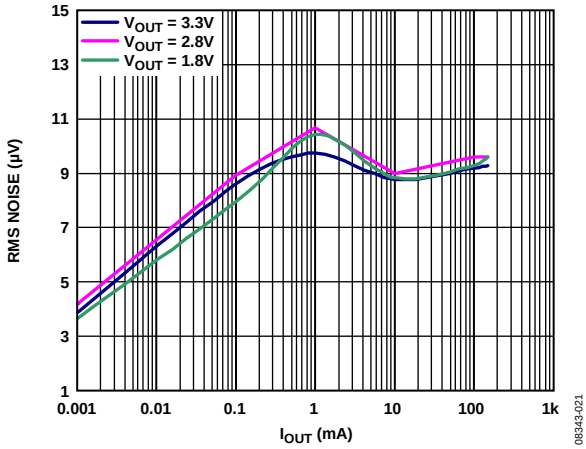

Figure 20. Output RMS Noise vs. Load Current (I_{OUT}) and Output Voltage (V_{OUT}), V_{IN} = 5 V, C_{OUT} = 1 µF

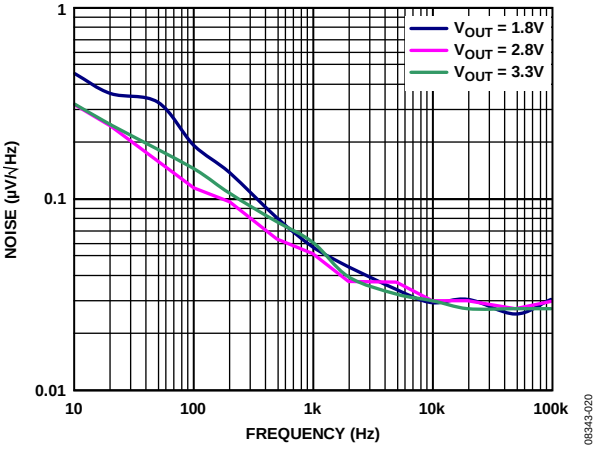

Figure 21. Output Noise Spectrum, V_{IN} = 5 V, I_{LOAD} = 10 mA, C_{OUT} = 1 µF

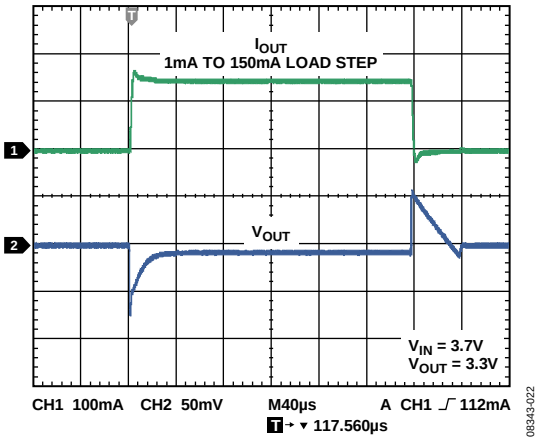

Figure 22. Load Transient Response, C_{OUT} = 1 µF

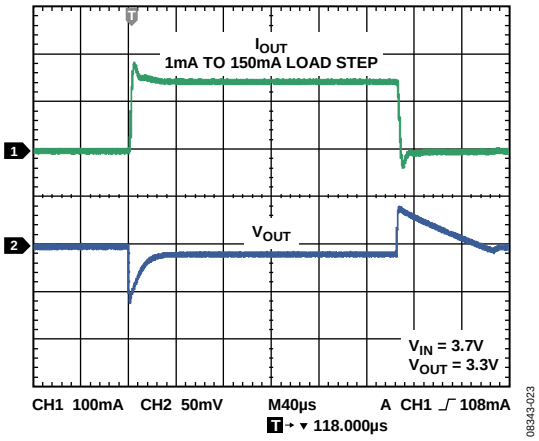

Figure 23. Load Transient Response, C_{OUT} = 4.7 µF

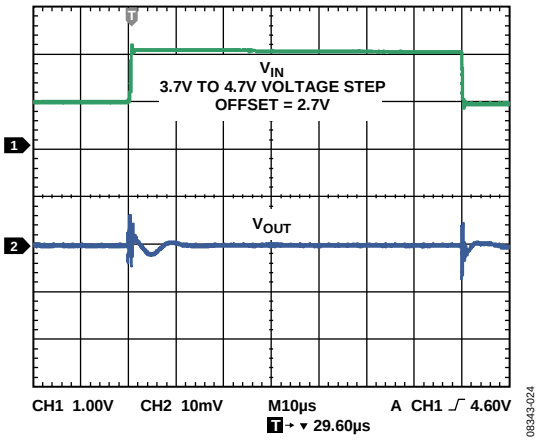

Figure 24. Line Transient Response, C_{IN}, C_{OUT} = 1 µF, I_{LOAD} = 1mA

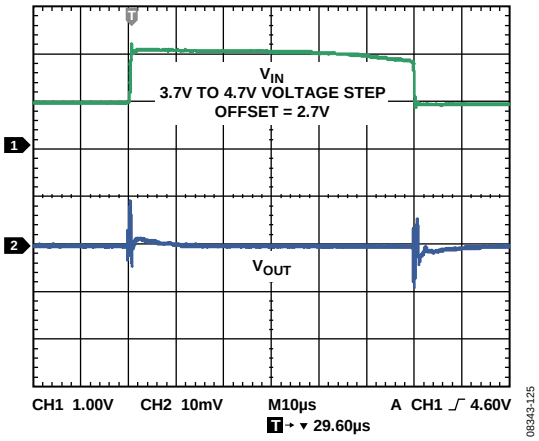

Figure 25. Line Transient Response, C_{IN}, C_{OUT} =1 µF, I_{LOAD} = 150 mA

THEORY OF OPERATION

The ADP150 is an ultralow noise, low quiescent current, low dropout linear regulator that operates from 2.2 V to 5.5 V and can provide up to 150 mA of output current. Drawing a low 220 µA of quiescent current (typical) at full load makes the ADP150 ideal for battery-operated portable equipment. Shutdown current consumption is typically 200 nA.

Using new innovative design techniques, the ADP150 provides superior noise performance for noise sensitive analog and RF applications without the need for a noise bypass capacitor. The ADP150 is also optimized for use with small 1 µF ceramic capacitors.

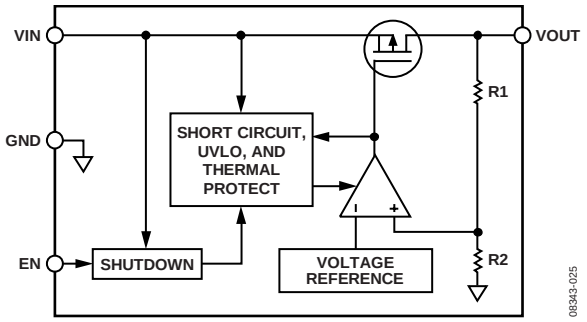

Figure 26. Internal Block Diagram

Internally, the ADP150 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device that is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP150 is available in 14 output voltage options, ranging from 1.8 V to 3.3 V. The ADP150 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on, and when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP150 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1 µF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADP150. The transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP150 to large changes in the load current. Figure 27 and Figure 28 show the transient responses for output capacitance values of 1 µF and 4.7 µF, respectively.

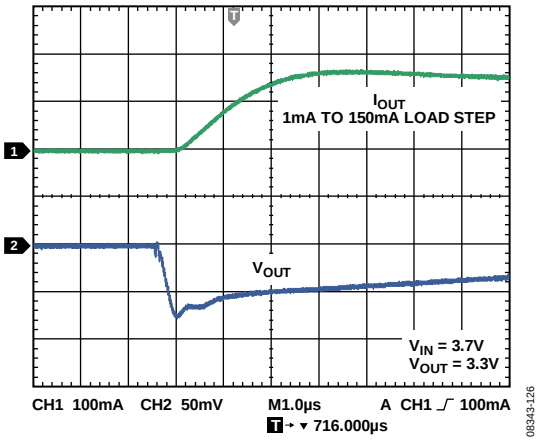

Figure 27. Output Transient Response, C_{OUT} = 1 µF

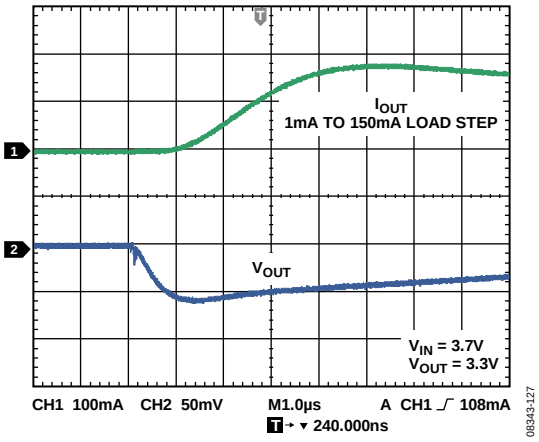

Figure 28. Output Transient Response, C_{OUT} = 4.7 µF

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance is encountered. If greater than 1 µF of output capacitance is required, increase the input capacitor to match the output capacitor.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP150, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 29 depicts the capacitance vs. the voltage bias characteristic of a 0402, 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

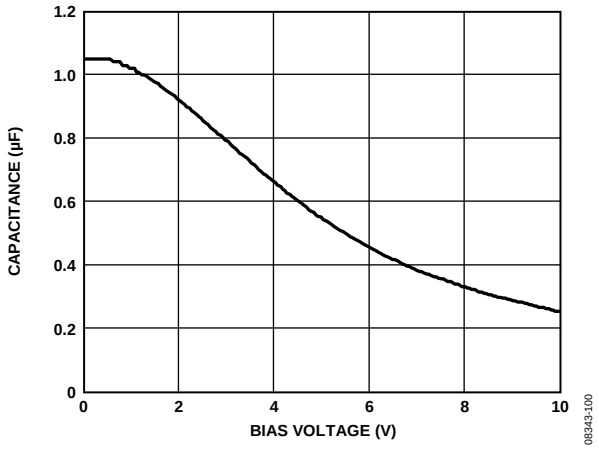

Figure 29. Capacitance vs. Voltage Bias Characteristic

Use Equation 1 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:

C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and the C_{BIAS} is 0.94 µF at 1.8 V, as shown in Figure 29.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP150, it is imperative that the effects of the dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each.

UNDERVOLTAGE LOCKOUT

The ADP150 has an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 2.0 V. This ensures that the ADP150 inputs and output behave in a predictable manner during power-up.

ENABLE FEATURE

The ADP150 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 30, when a rising voltage on EN crosses the active threshold, V_{OUT} turns on. When a falling voltage on EN crosses the inactive threshold, V_{OUT} turns off.

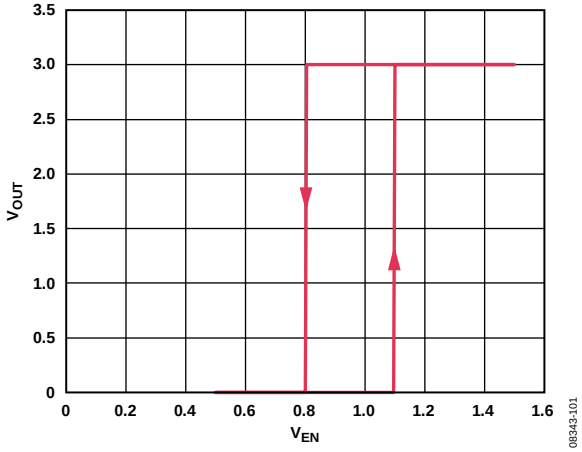

Figure 30. Typical EN Pin Operation

As shown in Figure 30, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the VIN voltage; therefore, these thresholds vary with changing input voltage. Figure 31 shows the typical EN active/inactive thresholds when the input voltage varies from 2.2 V to 5.5 V.

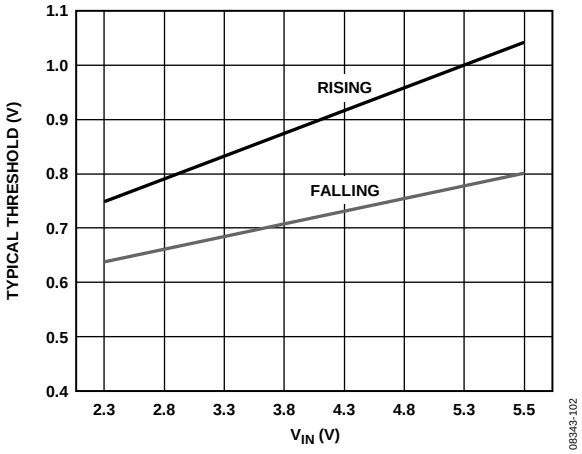

Figure 31. Typical EN Pin Thresholds vs. Input Voltage (V_{IN})

The ADP150 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 3.3 V option is approximately 150 µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in Figure 32, the start-up time is dependent on the output voltage setting.

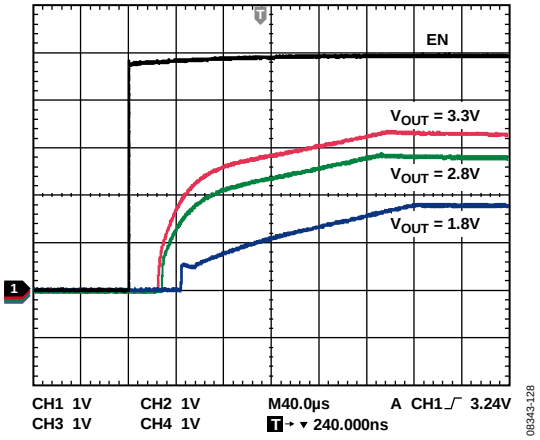

Figure 32. Typical Start-Up Time

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP150 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP150 is designed to limit current when the output load reaches 260 mA (typical). When the output load exceeds 260 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again and the output current is restored to its nominal value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADP150 limits current so that only 260 mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 260 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 260 mA and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

In most applications, the ADP150 does not dissipate much heat due to its high efficiency. However, in applications with high ambient temperature and high supply voltage to output voltage differential, the heat dissipated in the package is large enough that it can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature decreases below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP150 must not exceed 125°C. To ensure that the junction temperature stays below 125°C, be aware of the parameters that contribute to the junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB. Table 7 shows typical θ_{JA} values of the 5-lead TSOT and 4-ball WLCSP packages for various PCB copper sizes. Table 8 shows the typical Ψ_{JB} value of the 5-lead TSOT and 4-ball WLCSP.

Table 7. Typical θJA Values

	θ_{JA} (°C/W)	
Copper Size (mm²)	**TSOT**	**WLCSP**
0[1]	170	260
50	152	159
100	146	157
300	134	153
500	131	151

[1] Device soldered to minimum size pin traces.

Table 8. Typical Ψ_{JB} Values

Ψ_{JB} (°C/W)	
TSOT	**WLCSP**
42.8	58.4

Use Equation 2 to calculate the junction temperature.

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND})$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (3)$$

As shown in the previous equation, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 33 to Figure 46 show the junction temperature calculations for the different ambient temperatures, load currents, V_{IN}-to-V_{OUT} differentials, and areas of PCB copper.

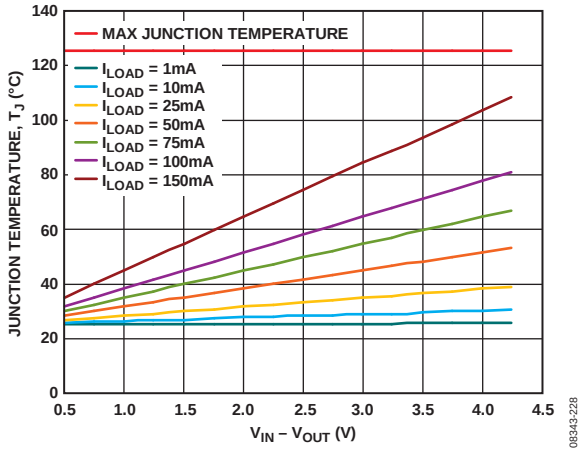

Figure 33. TSOT, 500 mm² of PCB Copper, T_A = 25°C

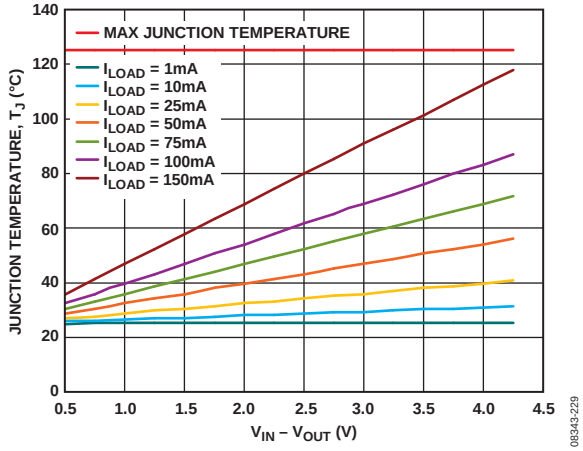

Figure 34. TSOT, 100 mm² of PCB Copper, T_A = 25°C

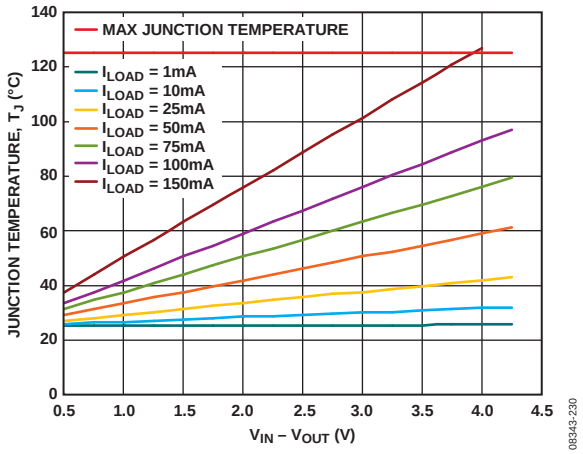

Figure 35. TSOT, 0 mm² of PCB Copper, T_A = 25°C

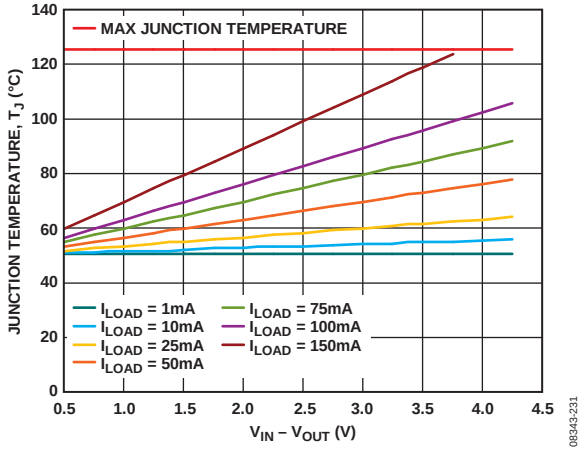

Figure 36. TSOT, 500 mm² of PCB Copper, T_A = 50°C

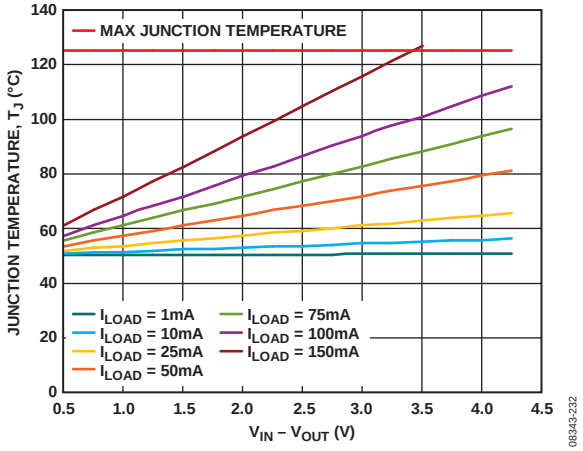

Figure 37. TSOT, 100 mm² of PCB Copper, T_A = 50°C

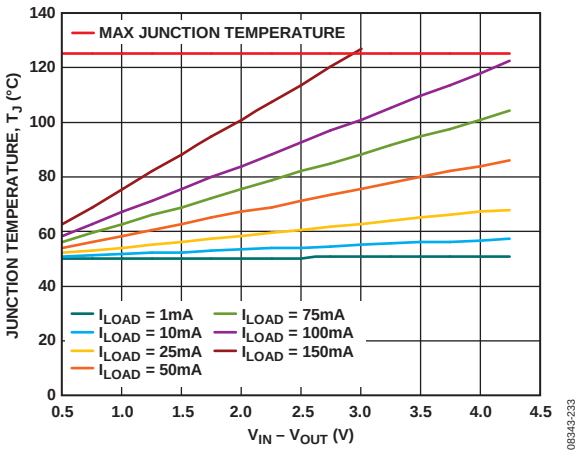

Figure 38. TSOT, 0 mm² of PCB Copper, T_A = 50°C

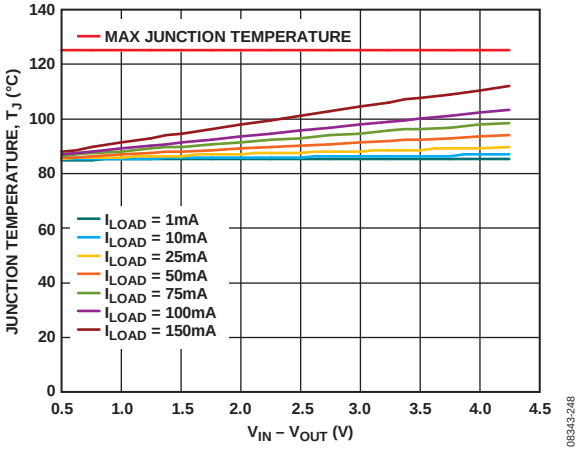

Figure 39. TSOT, 100 mm² of PCB Copper, Board Temperature = 85°C

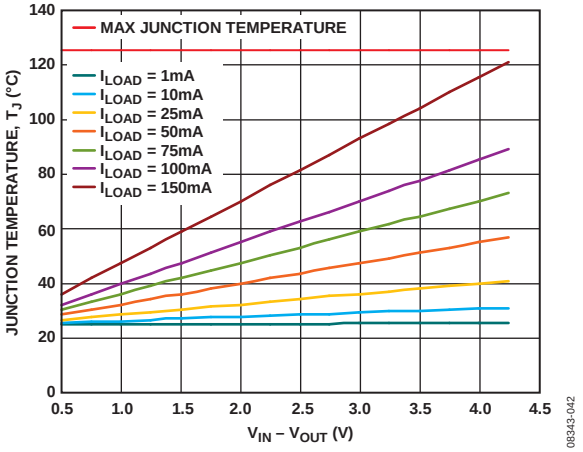

Figure 40. WLCSP, 500 mm² of PCB Copper, T_A = 25°C

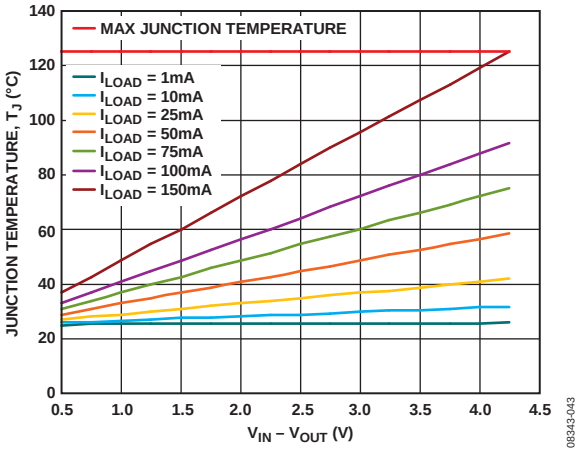

Figure 41. WLCSP, 100 mm² of PCB Copper, T_A = 25°C

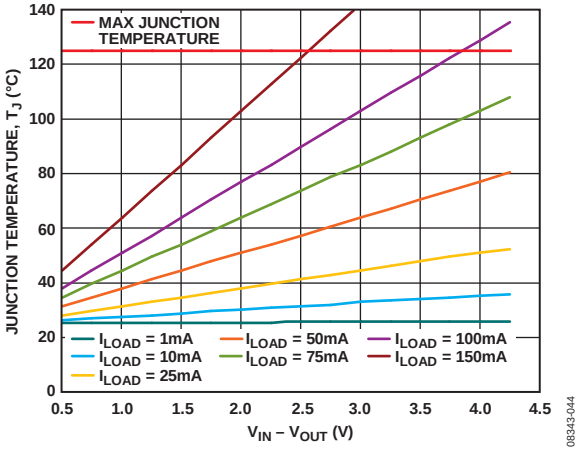

Figure 42. WLCSP, 0 mm² of PCB Copper, T_A = 25°C

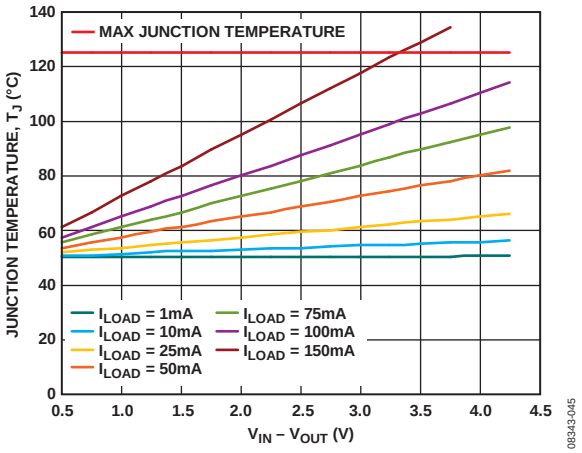

Figure 43. WLCSP, 500 mm² of PCB Copper, T_A = 50°C

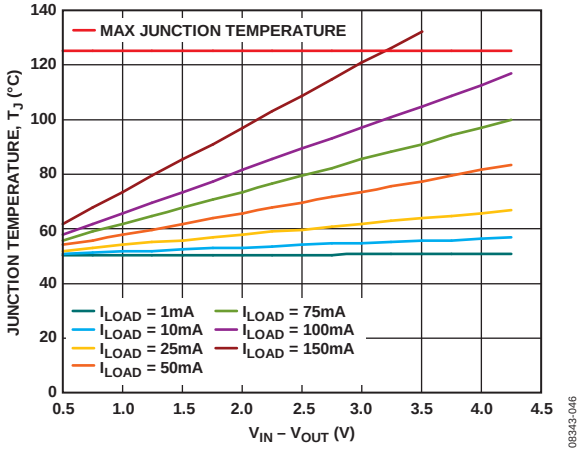

Figure 44. WLCSP, 100 mm² of PCB Copper, T_A = 50°C

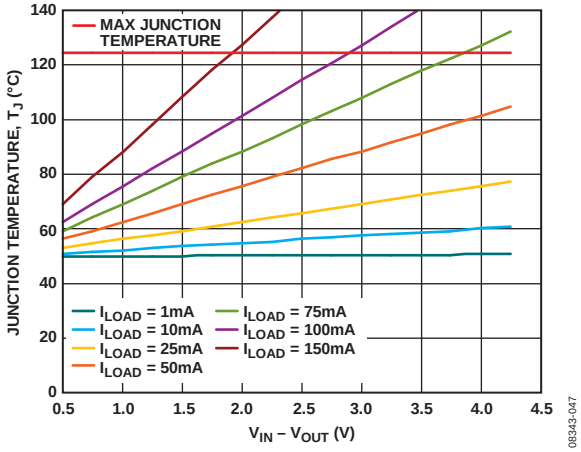

Figure 45. WLCSP, 0 mm² of PCB Copper, T_A = 50°C

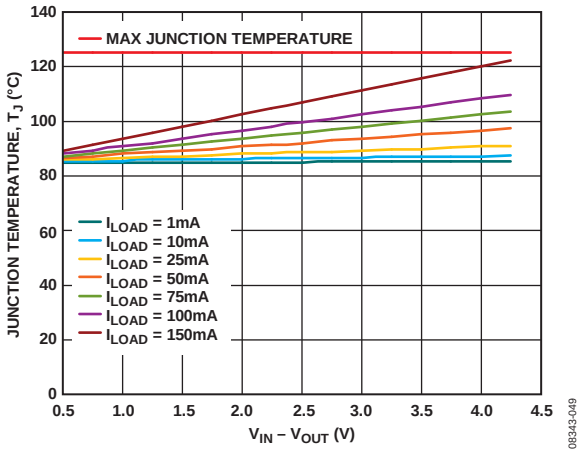

Figure 46. WLCSP, 100 mm² of PCB Copper, Board Temperature = 85°C

PCB LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP150. However, as listed in Table 7, a point of diminishing returns is reached eventually, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0402 size or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

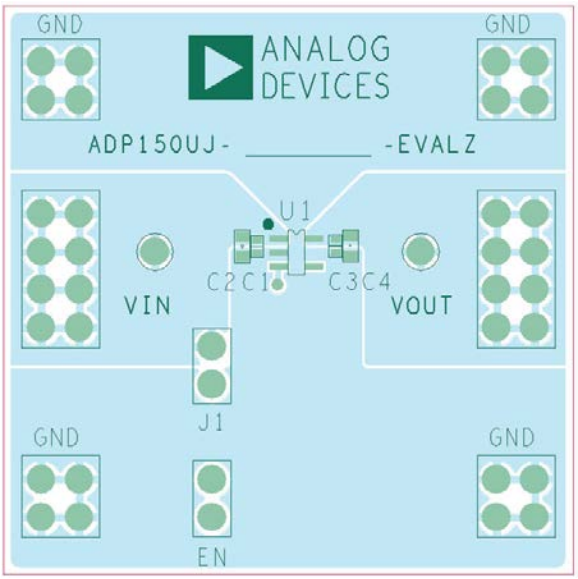

Figure 47. Example TSOT PCB Layout

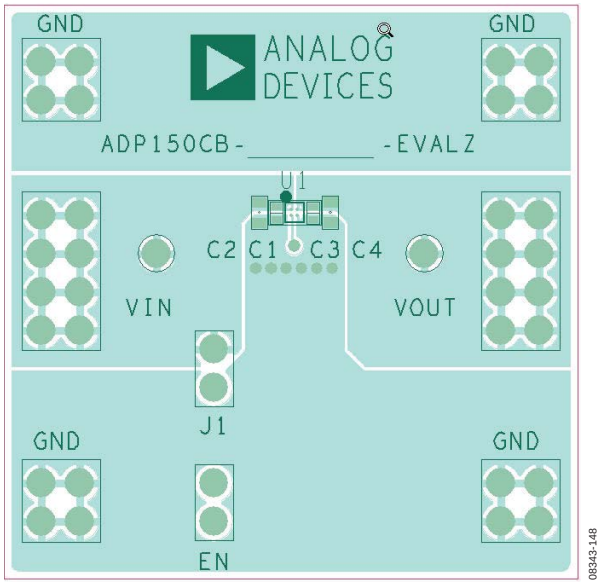

Figure 48. Example WLCSP PCB Layout

OUTLINE DIMENSIONS

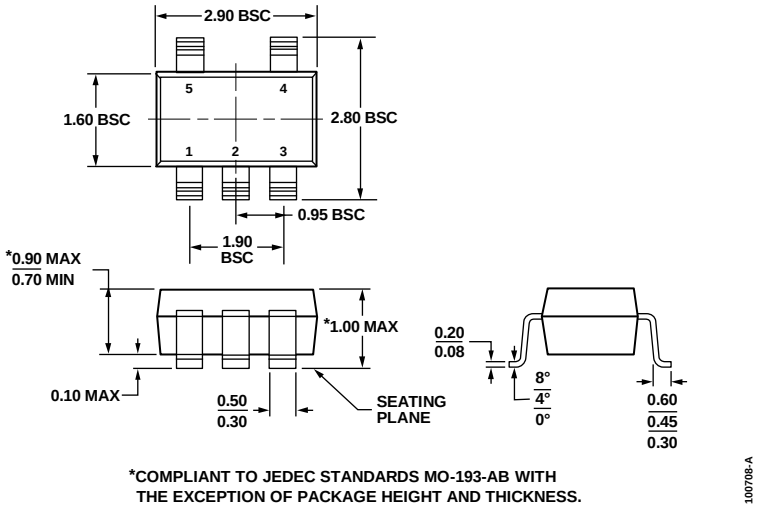

Figure 49. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions show in millimeters

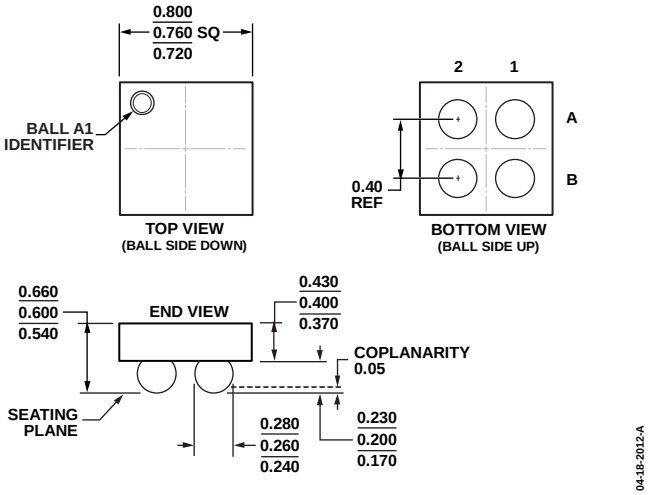

Figure 50.4-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-4-3)
Dimensions show in millimeters

ORDERING GUIDE

Model[1]	Temperature Range (T_J)	Output Voltage (V)[2]	Package Description	Package Option	Branding
ADP150ACBZ-1.8-R7	−40°C to +125°C	1.8	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-3	36
ADP150ACBZ-2.5-R7	−40°C to +125°C	2.5	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-3	3V
ADP150ACBZ-2.6-R7	−40°C to +125°C	2.6	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-3	63
ADP150ACBZ-2.75R7	−40°C to +125°C	2.75	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-3	3X
ADP150ACBZ-2.8-R7	−40°C to +125°C	2.8	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-3	46
ADP150ACBZ-2.85R7	−40°C to +125°C	2.85	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-3	3Y
ADP150ACBZ-3.0-R7	−40°C to +125°C	3.0	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-3	47
ADP150ACBZ-3.3-R7	−40°C to +125°C	3.3	4-Ball Wafer Level Chip Scale Package [WLCSP]	CB-4-3	48
ADP150AUJZ-1.8-R7	−40°C to +125°C	1.8	5-Lead Thin Small Outline Transistor Package [TSOT]	UJ-5	LDS
ADP150AUJZ-2.5-R7	−40°C to +125°C	2.5	5-Lead Thin Small Outline Transistor Package [TSOT]	UJ-5	LDZ
ADP150AUJZ-2.65-R7	−40°C to +125°C	2.65	5-Lead Thin Small Outline Transistor Package [TSOT]	UJ-5	LPE
ADP150AUJZ-2.8-R7	−40°C to +125°C	2.8	5-Lead Thin Small Outline Transistor Package [TSOT]	UJ-5	LE3
ADP150AUJZ-3.0-R7	−40°C to +125°C	3.0	5-Lead Thin Small Outline Transistor Package [TSOT]	UJ-5	LE2
ADP150AUJZ-3.3-R7	−40°C to +125°C	3.3	5-Lead Thin Small Outline Transistor Package [TSOT]	UJ-5	LEJ
ADP150CB-3.3-EVALZ		3.3	Evaluation Board with WLCSP package		
ADP150UJZ-REDYKIT			Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] Up to 14 fixed output voltage options from 1.8 V to 3.3 V are available. For additional voltage options, contact your local Analog Devices, Inc, sales or distribution representative.

NOTES

D08343-0-8/13(B)