

1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS design technology combines higher speeds and smaller size with the low power and high noise immunity.

On chip memory system includes 0.5 K words of ROM, and 32 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software :

- ◆ Fully CMOS static design
- ◆ 8-bit data bus
- ◆ On chip ROM size : 512 words
- ◆ Internal RAM size : 32 bytes (25 general purpose registers, 7 special registers)
- ◆ 36 single word instructions
- ◆ 14-bit instructions
- ◆ 2-level stacks
- ◆ Operating voltage : 2.3V ~ 6.0 V
- ◆ Operating frequency : 0 ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instructions
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset (POR), only available while PED is Disable
- ◆ Power edge-detector Reset (PED)
- ◆ Sleep Mode for power saving
- ◆ 8-bit real time clock/counter(RTCC)

with 8-bit programmable prescaler

- ◆ 4 types of oscillator can be selected by programming option (Internal Capacitor about 10p):
 - RC – Low cost RC oscillator
 - LFXT – Low frequency crystal oscillator
 - XTAL – Standard crystal oscillator
 - HFXT – High frequency crystal oscillator
- ◆ 4 oscillator start-up time can be selected by programming option:
 - 150 μ s, 20 ms, 40 ms, 80 ms
- ◆ On-chip RC oscillator based Watchdog Timer(WDT) can be operated freely
- ◆ 12 I/O pins with their own independent direction control

3. Applications

The application areas of this MDT10P05 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral ... etc.

4. Pin Assignment

DIP / SOP				SSOP			
PA2	1	18	PA1	PA2	1	20	PA1
PA3	2	17	PA0	PA3	2	19	PA0
RTCC	3	16	OSC1	RTCC	3	18	OSC1
/MCLR	4	15	OSC2	/MCLR	4	17	OSC2
V _{ss}	5	14	V _{dd}	VSS	5	16	VDD
PB0	6	13	PB7	VSS	6	15	VDD
PB1	7	12	PB6	PB0	7	14	PB7
PB2	8	11	PB5	PB1	8	13	PB6
PB3	9	10	PB4	PB2	9	12	PB5
				PB3	10	11	PB4

5. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3	I/O	Port A, TTL input level
PB0~PB7	I/O	Port B, TTL input level
RTCC	I	Real Time Clock/Counter, Schmitt Trigger input levels
/MCLR	I	Master Clear, Schmitt Trigger input levels
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
V _{dd}		Power supply
V _{ss}		Ground

6. Memory Map

(A) Register Map

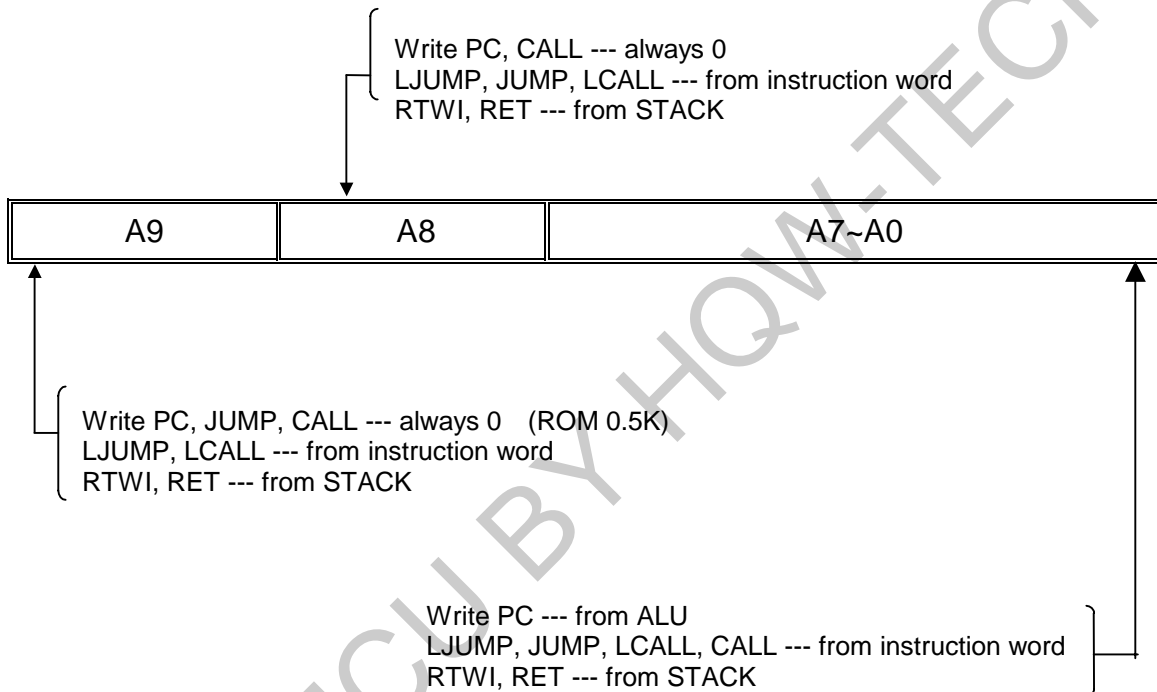
Address	Description
00	Indirect Addressing Register
01	RTCC
02	PC
03	STATUS

Address	Description
04	MSR
05	Port A
06	Port B
07~1F	Internal RAM, General Purpose Register

40 IAR (Indirect Address Register) : R0

(2) RTCC (Real Time Counter/Counter Register) : R1

(3) PC (Program Counter) : R2



(4) STATUS (Status register) : R3

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit
4	TF	Time overflow Flag bit
5-7	---	General purpose bit

(5) MSR (Memory Select Register) : R4

(6) PORT A : R5

PA3~PA0, I/O Register

(7) PORT B : R6

PB7~PB0, I/O Register

(8) TMR (Time Mode Register)

Bit	Symbol	Function		
2—0	PS2—0	Prescaler Value	RTCC rate	WDT rate
		0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
1 1 1	1 : 256	1 : 128		
3	PSC	Prescaler assignment bit : 0 — RTCC 1 — Watchdog Timer		
4	TCE	RTCC signal Edge : 0 — Increment on low-to-high transition on RTCC pin 1 — Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 — Internal instruction cycle clock 1 — Transition on RTCC pin		

(9) CPIO A, CPIO B (Control Port I/O Mode Register)

The CPIO register is "write-only"

= "0", I/O pin in output mode;

= "1", I/O pin in input mode.

(10) EPROM Option by writer programming :

Oscillator Type	Oscillator Start-up Time
RC Oscillator	150 μs, 20ms, 40ms, 80ms
HFXT Oscillator	20 ms, 40ms, 80ms
XTAL Oscillator	20ms, 40 ms, 80ms
LFXT Oscillator	40 ms, 80 ms

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power Edge Detect
PED Disable
PED Enable

Security bit
Security Disable
Security Enable

The default EPROM security is disable. Once the IC was set to enable, it can not set to disable again.

(B) Program Memory

Address	Description
000-1FF	Program memory for MDT10P05
1FF	The starting address of the power on, external reset or WDT time-out reset for MDT10P05

7. Reset Condition for all Registers

Register	Address	Power-On Reset	/MCLR or WDT Reset
CPIO A	--	1111 1111	1111 1111
CPIO B	--	1111 1111	1111 1111
TMR	--	-- 11 1111	-- 11 1111
IAR	00h	xxxx xxxx	uuuu uuuu
RTCC	01h	xxxx xxxx	uuuu uuuu
PC	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
MSR	04h	111x xxxx	111u uuuu
PORT A	05h	---- xxxx	---- uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu

Note : u = unchanged, x = unknown, - = unimplemented, read as "0"
 # = value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3
/MCLR reset (not during SLEEP)	u	u
/MCLR reset during SLEEP	1	0
WDT reset (not during SLEEP)	0	1
WDT reset during SLEEP	0	0

8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔ R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R - W→t (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R - 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R - 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C →R(7), R(0)→C	C

Instruction Code	Mnemonic Operands	Function	Operating	Status
010101 trrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
1000nn nnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
1010nn nnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110000 nnnnnnn	CALL n	Call subroutine	n→PC, PC+1→Stack	None
110001 iiiiiii	RTWI i	Return, place immediate to W	Stack→PC, i→W	None
11001n nnnnnnn	JUMP n	JUMP to address	n→PC	None

Note :

- | | | | |
|--------|-----------------------------|----|-----------------------------|
| W | : Working register | b | : Bit position |
| WT | : Watchdog timer | t | : Target |
| TMODE | : TMODE mode register | 0 | : Working register |
| CPIO | : Control I/O port register | 1 | : General register |
| TF | : Timer overflow flag | R | : General register address |
| PF | : Power loss flag | C | : Carry flag |
| PC | : Program Counter | HC | : Half carry |
| OSC | : Oscillator | Z | : Zero flag |
| Inclu. | : Inclusive 'U' | / | : Complement |
| Exclu. | : Exclusive ' ' | x | : Don't care |
| AND | : Logic AND '∩' | i | : Immediate data (8 bits) |
| | | n | : Immediate address |

9. Electrical Characteristics

(A) Operating Voltage & Frequency

V_{dd} : 2.3V ~ 6.0 V

Frequency: 0 Hz ~ 20 MHz

(B) Input Voltage

@ $V_{dd}=5.0\text{ V}$, Temperature = 25 °C

	Port	Min.	Max.
V_{il}	PA, PB	V_{ss}	1.0 V
	RTCC, /MCLR	V_{ss}	1.0V
V_{ih}	PA, PB	2.0 V	V_{dd}
	RTCC, /MCLR	3.1 V	V_{dd}

***Threshold Voltage :**

Port A, Port B $V_{th}=1.5\text{V}$

RTCC/MCLR $V_{il}=1.2\text{V}$, $V_{ih}=3.0\text{V}$ (Schmitt Trigger)

(C) Output Voltage :

@ $V_{dd}=5.0\text{ V}$, Temperature = 25 °C, the typical value as followings :

PA, PB Port	
$I_{oh} = -20.0\text{ mA}$	$V_{oh} = 3.6\text{ V}$
$I_{ol} = 20.0\text{ mA}$	$V_{ol} = 0.6\text{ V}$
$I_{oh} = -5.0\text{ mA}$	$V_{oh} = 4.6\text{ V}$
$I_{ol} = 5.0\text{ mA}$	$V_{ol} = 0.3\text{ V}$

(D) Leakage Current

@ $V_{dd}=5.0\text{ V}$, Temperature = 25 °C, the typical value as followings :

I_{il}	- 0.1 μA (Max.)
I_{ih}	+ 0.1 μA (Max.)

(E) Sleep Current

@WDT – Disable, PED-Disable Temperature = 25 °C, the typical value as followings :

$V_{dd}=2.3\text{ V}$	$I_{dd} < 0.1\ \mu\text{A}$
$V_{dd}=3.0\text{ V}$	$I_{dd} < 0.1\ \mu\text{A}$
$V_{dd}=4.0\text{ V}$	$I_{dd} < 0.1\ \mu\text{A}$
$V_{dd}=5.0\text{ V}$	$I_{dd} < 0.1\ \mu\text{A}$
$V_{dd}=6.0\text{V}$	$I_{dd} < 0.1\ \mu\text{A}$

@WDT – Enable, PED-Disable Temperature = 25 °C, the typical value as followings :

$V_{dd} = 2.3\text{ V}$	$I_{dd} < 1.0\ \mu\text{A}$
$V_{dd} = 3.0\text{ V}$	$I_{dd} = 3.0\ \mu\text{A}$
$V_{dd} = 4.0\text{ V}$	$I_{dd} = 7.5\ \mu\text{A}$
$V_{dd} = 5.0\text{ V}$	$I_{dd} = 16.0\ \mu\text{A}$
$V_{dd} = 6.0\text{ V}$	$I_{dd} = 26.0\ \mu\text{A}$

(F) Typical Operating Current : (Temperature = 25 °C)

(i) OSC Type = RC (OSC1&OSC2 Internal Cap about 10P); WDT – Enable;

The IC may not oscillate properly if the resistance of R_{ext} less than 4.7K.

The minimum resistance of R_{ext} must be more than 4.7K.

@ $V_{dd} = 5.0\text{ V}$

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
0P	4.7 K	11.5 M	1.2 mA
	10.0 K	5.3 M	700 μA
	47.0 K	1.3 M	250 μA
	100.0 K	628 K	200 μA
	300.0 K	215 K	140 μA
	470.0 K	135 K	135 μA
3P	4.7 K	9.3 M	1.1 mA
	10.0 K	4.4 M	540 μA
	47.0 K	1.05 M	225 μA
	100.0 K	540 K	160 μA
	300.0 K	170 K	130 μA
	470.0 K	110 K	120 μA
20P	4.7 K	5.4 M	630 μA
	10.0 K	2.4 M	340 μA
	47.0 K	600 K	170 μA
	100.0 K	285 K	140 μA
	300.0 K	110 K	120 μA
	470.0 K	55 K	110 μA

Cext. (F)	Rext. (Ohm)	Frequency (Hz)	Current (A)
100P	4.7 K	2.0 M	310 μ A
	10.0 K	1.0 M	220 μ A
	47.0 K	230 K	140 μ A
	100.0 K	110 K	130 μ A
	300.0 K	35 K	110 μ A
	470.0 K	20 K	100 μ A
300P	4.7 K	900 K	200 μ A
	10.0 K	400 K	180 μ A
	47.0 K	90 K	115 μ A
	100.0 K	40 K	110 μ A
	300.0 K	14 K	105 μ A
	470.0 K	9.2 K	100 μ A

(ii) OSC Type=LF (OSC1 & OSC2 Internal Cap); WDT – Disable
; PED=Enable

Voltage/Frequency	32 K (Ext C=50P)	455 K (Ext C=50P)	1 M	Sleep
2.3 V	11 μ A	22 μ A	@2.4V 35 μ A	< 0.1 μ A
3.0 V	19 μ A	40 μ A	50 μ A	< 0.1 μ A
4.0 V	40 μ A	75 μ A	85 μ A	< 0.1 μ A
5.0 V	70 μ A	120 μ A	140 μ A	< 0.1 μ A
6.0 V	125 μ A	200 μ A	220 μ A	< 0.1 μ A

(iii) OSC Type=XT(OSC1&OSC2 Internal Cap about 10P); WDT – Enable

Voltage/Frequency	1 M	4 M	10 M	Sleep
2.3 V	32 μ A	100 μ A	230 μ A	< 1.0 μ A
3.0 V	75 μ A	180 μ A	385 μ A	3.0 μ A
4.0 V	155 μ A	300 μ A	610 μ A	7.5 μ A
5.0 V	250 μ A	440 μ A	950 μ A	16 μ A
6.0 V	400 μ A	650 μ A	1.2 mA	27 μ A

(iv) OSC Type=HF (OSC1& OSC2 Internal Cap about 10P); WDT – Enable

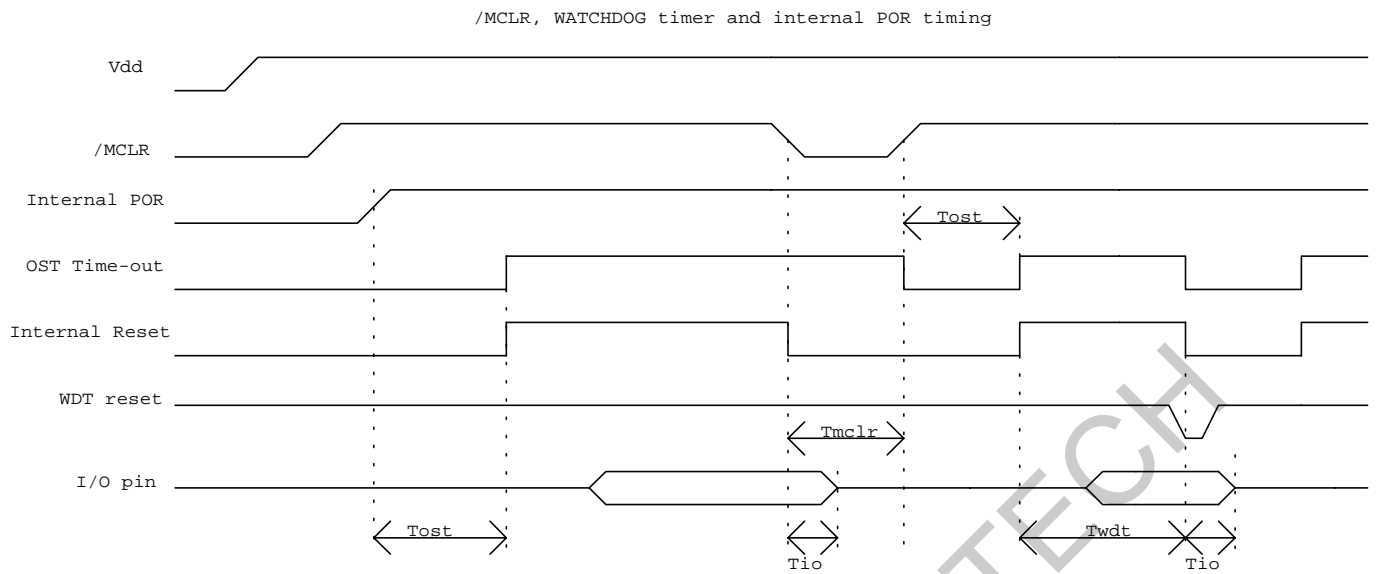
Voltage/Frequency	4 M	10 M	20 M	Sleep
2.3 V	100 μ A	230 μ A	@2.5V 590 μ A	< 1.0 μ A
3.0 V	200 μ A	420 μ A	750 μ A	3.0 μ A
4.0 V	340 μ A	650 μ A	1.1 mA	7.5 μ A
5.0 V	540 μ A	900 μ A	1.7 mA	16 μ A
6.0 V	900 μ A	1.25 mA	2.35 mA	27 μ A

(G)The basic WDT time-out cycle time

@ $V_{dd}=5.0v$,Temperature = 25 $^{\circ}C$, the typical value as followings :

Voltage (V)	Basic WDT time-out cycle time (ms)
2.3	23.5
3.0	21.5
4.0	20.3
5.0	18.3
6.0	17.5

(H) Reset & Watchdog Timer Timing

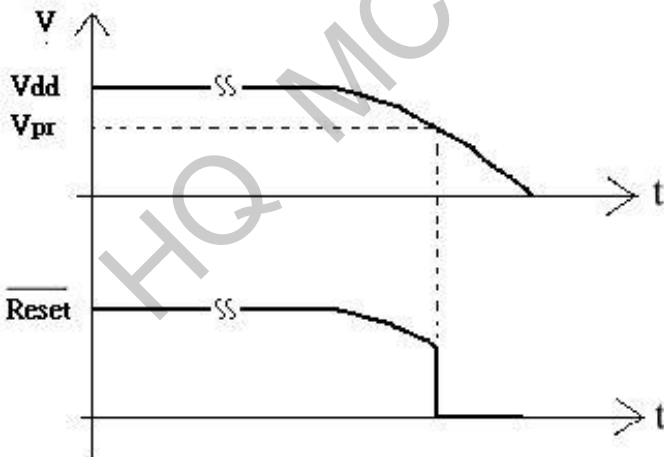


Symbol	Description	Min	Typ	Max	Unit
Tost	Oscillator start up time	15	20	24	ms
Tio	I/O floating from /MCLR low			100	ns
Tmclr	/MCLR pulse width	500			ns
Twdt	Watchdog timer time-out period (No postscaler)	15	20	24	ms

(I) Power Edge-detector Reset Voltage (Not in Sleep Mode), @ V_{dd}=5.0 V(PED : Enable)

$V_{pr} \leq 1.6 \sim 1.9 \text{ V}$

$V_{pr} : V_{dd}$ (Power Supply)

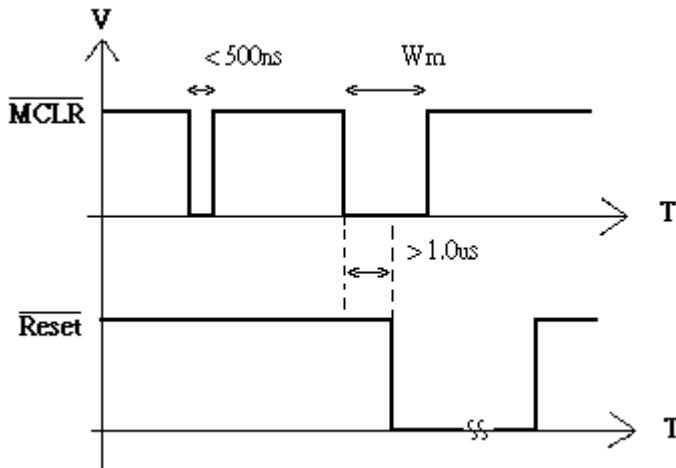


PS.IF PED_Enable then Internal Power_on_reset will be off

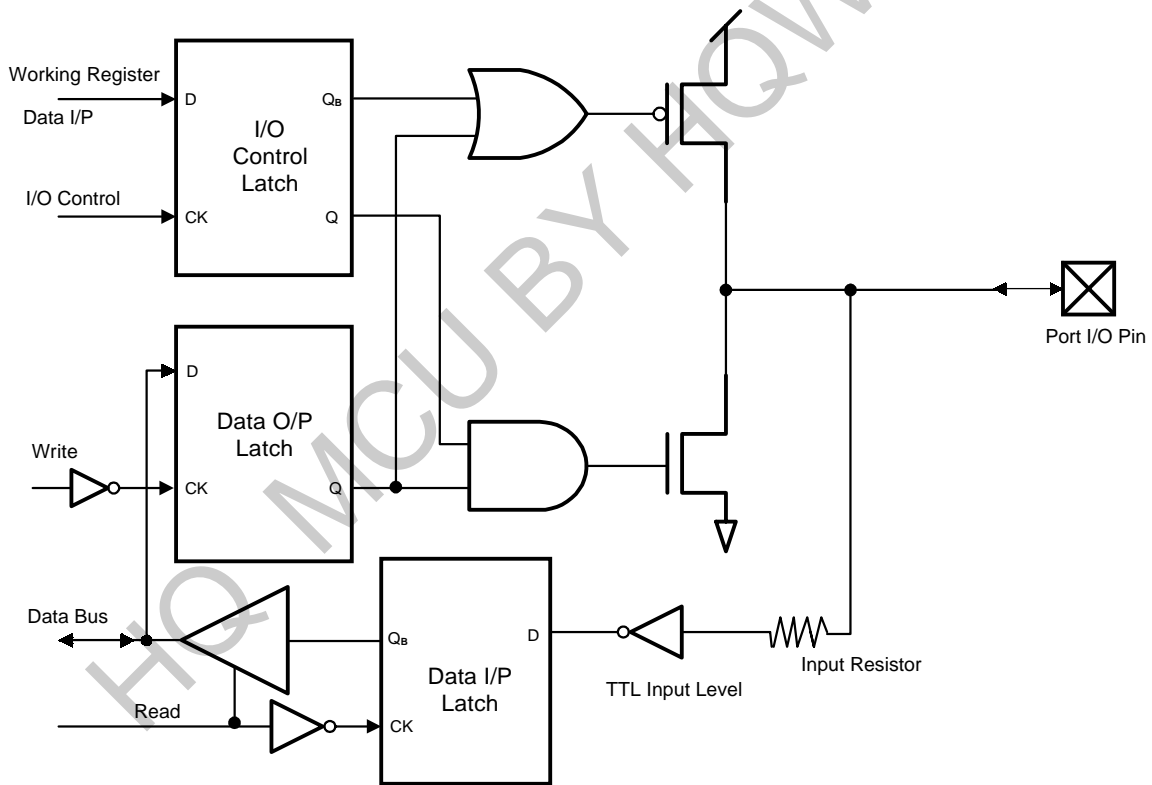
(J) MCLR Filter : @ $V_{dd}=5.0v$

$W_m \geq 1.2\mu s$

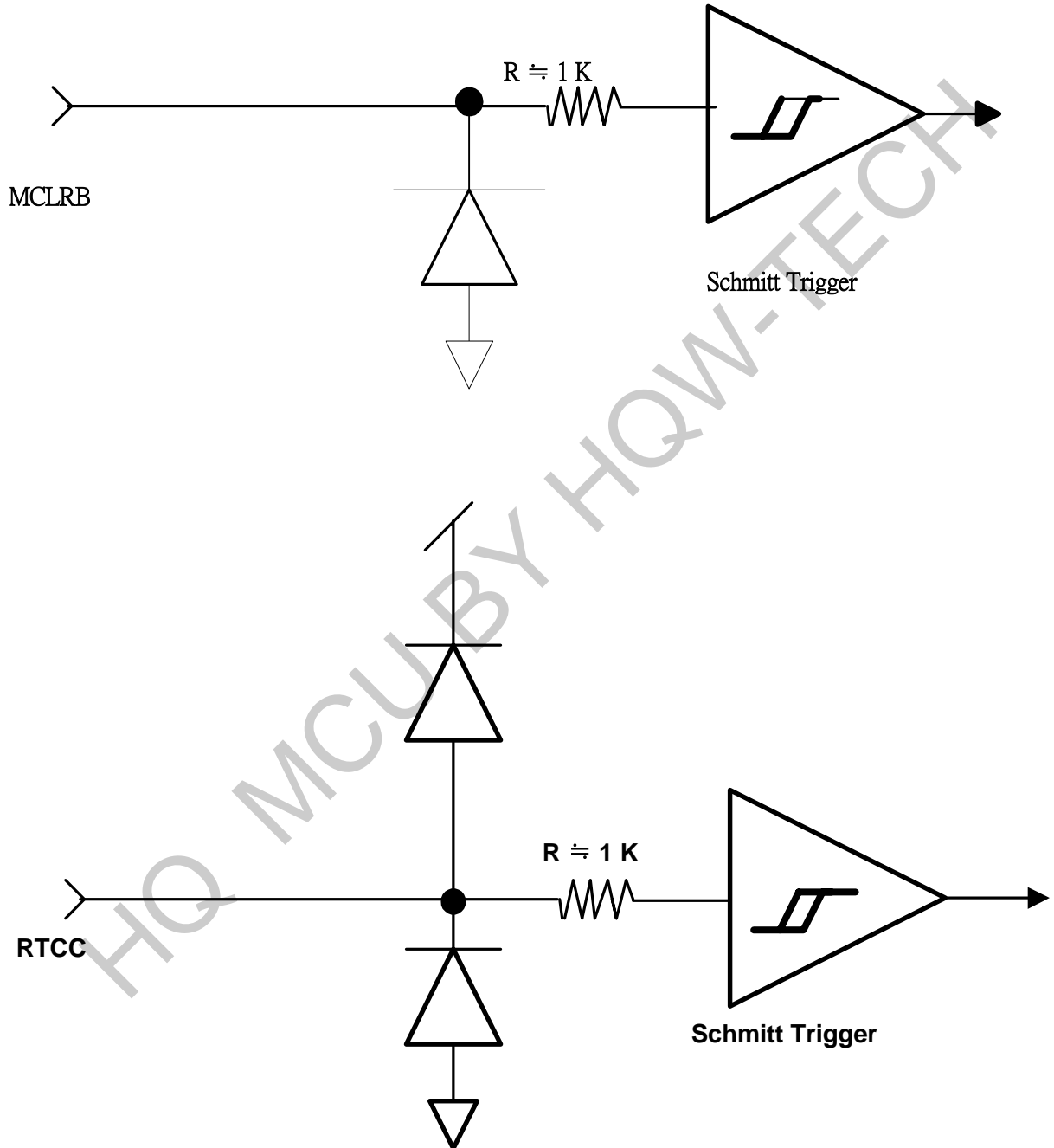
W_m : Filter pulse width (low) in /MCLR pin.



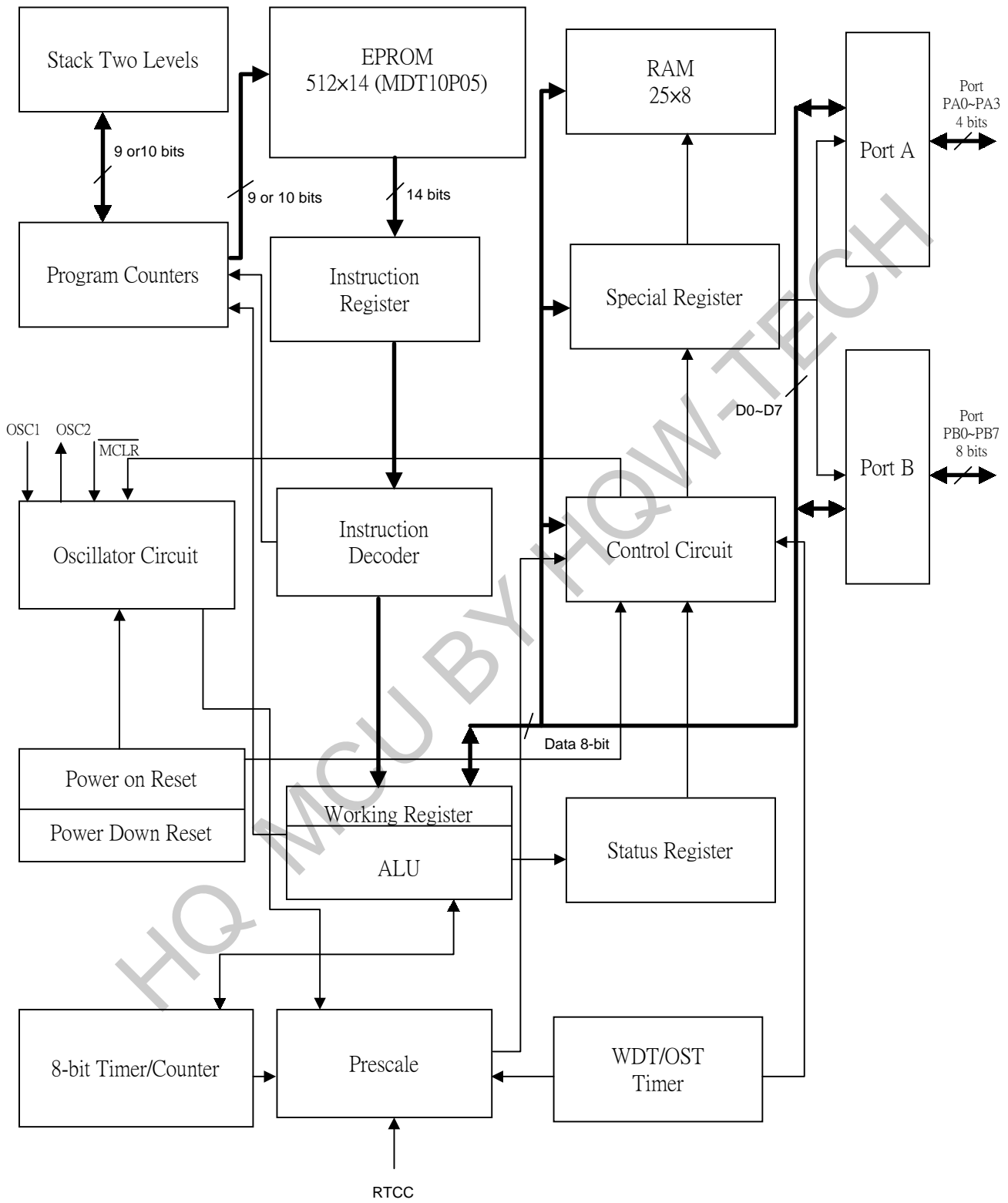
10. Port A and Port B Equivalent Circuit



11. MCLR_B and RTCC Input Equivalent Circuit



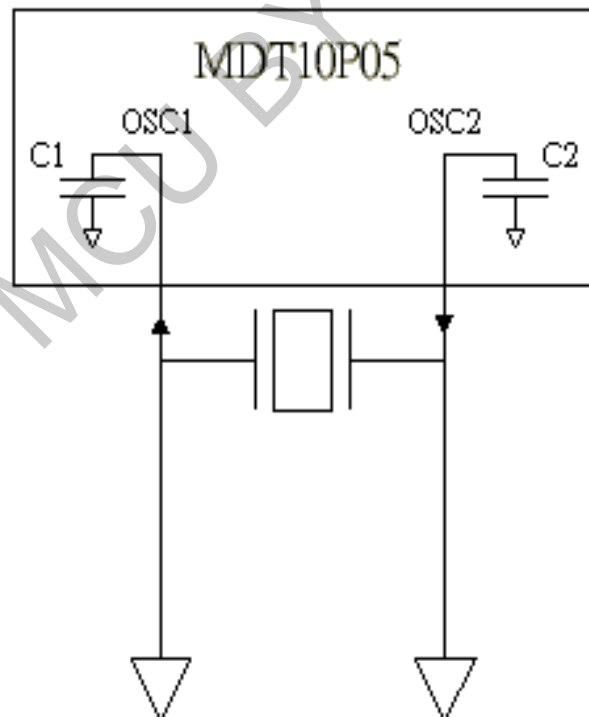
12. Block Diagram



13. Internal Capacitor Selection For Crystal Oscillator

@ $V_{dd} = 3.0V \sim 5.0V$

Osc. Type	Resonator Freq.	C1	C2
HF	20 MHz	0 pF ~10 pF	0 pF ~20 pF
	10 MHz	0 pF ~50 pF	0 pF ~100 pF
	4 MHz	0 pF ~30 pF	0 pF ~100 pF
XT	10 MHz	0 pF ~30 pF	0 pF ~50 pF
	4 MHz	0 pF ~50 pF	0 pF ~100 pF
	1 MHz	0 pF ~30 pF	0 pF ~50 pF
LF	1 MHz	5 pF ~10 pF	5 pF ~10 pF
	455 K	10 pF ~50 pF	10 pF ~50 pF
	32 K	10 pF ~30 pF	20 pF ~50 pF



To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor range can be recommended for reference, but the higher capacitance also increases the start-up time.



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