

## 1. General Description

This 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 4K words of FLASH ROM, and 256 bytes of EEPROM, and 192 bytes of static RAM.

## 2. Features

The followings are some of the features on the hardware and software :

- ◆ Fully CMOS static design
- ◆ 8-bit data bus
- ◆ On chip FLASH ROM size: 4.0 K words
- ◆ Internal RAM size: 192 bytes
- ◆ 256 bytes of EEPROM
- ◆ 37 single word instructions
- ◆ 14-bit instructions
- ◆ 8-level stacks
- ◆ Operating voltage:
  - 2.5 V ~ 5.5 V (NORMAL)
  - 4.5 V ~ 5.5 V (PED High level)
- ◆ Operating frequency: DC ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset
- ◆ Power edge-detector Reset
  - Low level around 1.8V.
  - Middle level around 2.1V.
  - High level around 3.8V.
- ◆ Sleep Mode for power saving
- ◆ Capture, Compare, PWM module
- ◆ Synchronous serial port with SCM
- ◆ 12 interrupt sources:
  - External INT pin
  - TMR0 timer, TMR1 timer, TMR2 timer
  - A/D conversion completion
  - Port B<7:4> interrupt on change
  - EEPROM interrupt
  - CCP1, CCP2, SCM, USAR, USAT
- ◆ A/D converter module:
  - 5 analog inputs multiplexed into one A/D converter
  - 8 bit resolution
- ◆ TMR0: 8-bit timer/counter  
TMR1: 16-bit timer/counter  
TMR2: 8-bit timer
- ◆ 4 types of oscillator can be selected by programming option:
  - RC – Low cost RC oscillator
  - LFXT – Low frequency crystal oscillator
  - XTAL – Standard crystal oscillator
  - HFXT – High frequency crystal oscillator
- ◆ On-chip RC oscillator based Watchdog Timer (WDT)
- ◆ 22 I/O pins with their own independent direction control

## 3. Applications

The application areas of this MDT10F73 range from appliance motor control and high speed auto-motive to low power remote transmitters / receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral ... etc.

**4. Pin Assignment**

|                 |    |    |         |
|-----------------|----|----|---------|
| /MCLR           | 1  | 28 | PB7     |
| PA0/AIC0        | 2  | 27 | PB6     |
| PA1/AIC1        | 3  | 26 | PB5     |
| PA2/AIC2        | 4  | 25 | PB4     |
| PA3/AIC3/Vre    | 5  | 24 | PB3     |
| PA4/T0CKI       | 6  | 23 | PB2     |
| PA5/SSB AIC4    | 7  | 22 | PB1     |
| VSS             | 8  | 21 | PB0/INT |
| OSC1            | 9  | 20 | VDD     |
| OSC2            | 10 | 19 | VSS     |
| PC0/T1OSO/T1CKI | 11 | 18 | PC7     |
| PC1/T1OSI/CCP2  | 12 | 17 | PC6     |
| PC2/CCP1        | 13 | 16 | PC5/SDO |
| PC3/SC          | 14 | 15 | PC4/SDI |

MDT10F73K12(SKINNY)

MDT10F73S12(SOP)

MDT10F73SS12(SSOP)

**5. Order Information**

| Device       | ROM (Words) | RAM (Bytes) | I/O | A/D (8 bits) | Timer (8/16) | CCP | SCM/ USART | Package |
|--------------|-------------|-------------|-----|--------------|--------------|-----|------------|---------|
| MDT10F73K12  | 4K          | 192         | 22  | 5-channel    | 2/1          | 2   | YES/YES    | SKINNY  |
| MDT10F73S12  | 4K          | 192         | 22  | 5-channel    | 2/1          | 2   | YES/YES    | SOP     |
| MDT10F73SS12 | 4K          | 192         | 22  | 5-channel    | 2/1          | 2   | YES/YES    | SSOP    |

**6. Pin Function Description**

| Pin Name     | I/O | Function Description  |
|--------------|-----|---|
| PA0~PA3, PA5 | I/O | Port A, TTL input level / Analog input channel  |
| PA4          | I/O | PA4, Schmitt Trigger input levels, Open drain output  |
| PB0~PB7      | I/O | Port B, TTL input level / PB0: External interrupt input<br>PB4~PB7: Interrupt on pin change |
| PC0~PC7      | I/O | Port C, Schmitt Trigger input levels  |
| /MCLR        | I   | Master Clear, Schmitt Trigger input levels  |
| OSC1/CLKIN   | I   | Oscillator Input / external clock input   |
| OSC2/CLKOUT  | O   | Oscillator Output / in RC mode, the CLKOUT pin has 1/4 frequency of CLKIN                   |
| VDD          |     | Power supply  |
| VSS          |     | Ground  |

**7. Memory Map**

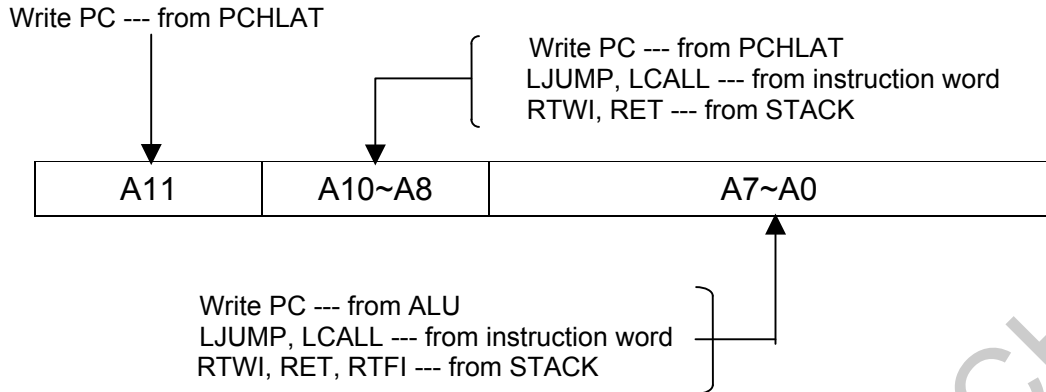
(A) Register Map

| Address      | Description                  |
|--------------|------------------------------|
| <b>BANK0</b> |                              |
| 00           | Indirect Addressing Register |
| 01           | RTCC                         |
| 02           | PCL                          |
| 03           | STATUS                       |
| 04           | MSR                          |
| 05           | Port A                       |
| 06           | Port B                       |
| 07           | Port C                       |
| 0A           | PCHLAT                       |
| 0B           | INTS                         |
| 0C           | PIFB1                        |
| 0D           | PIFB2                        |
| 0E           | TMR1L                        |
| 0F           | TMR1H                        |
| 10           | T1STA                        |
| 11           | TMR2                         |
| 12           | T2STA                        |
| 13           | SCMBUF                       |
| 14           | SCMCTL                       |
| 15           | CCP1L                        |
| 16           | CCP1H                        |
| 17           | CCP1CTL                      |
| 18           | RCSC                         |
| 19           | TXREG                        |
| 1A           | RCREG                        |
| 1B           | CCP2L                        |
| 1C           | CCP2H                        |
| 1D           | CCP2CTL                      |
| 1E           | ADRES                        |
| 1F           | ADS0                         |
| 20~7F        | General purpose register     |
| <b>BANK1</b> |                              |
| 81           | TMR                          |
| 85           | CPIO A                       |
| 86           | CPIO B                       |
| 87           | CPIO C                       |
| 8C           | PIEB1                        |
| 8D           | PIEB2                        |
| 8E           | PSTA                         |
| 92           | T2PER                        |
| 94           | SCMSTA                       |
| 98           | TXSC                         |
| 99           | BRREG                        |
| 9A           | EEDATA                       |
| 9B           | EEADR                        |
| 9C           | EECON1                       |
| 9D           | EECON2                       |
| 9F           | ADS1                         |
| A0~FF        | General purpose register     |

(1) IAR (Indirect Address Register): R00

(2) RTCC (Real Time Counter/Counter Register): R01

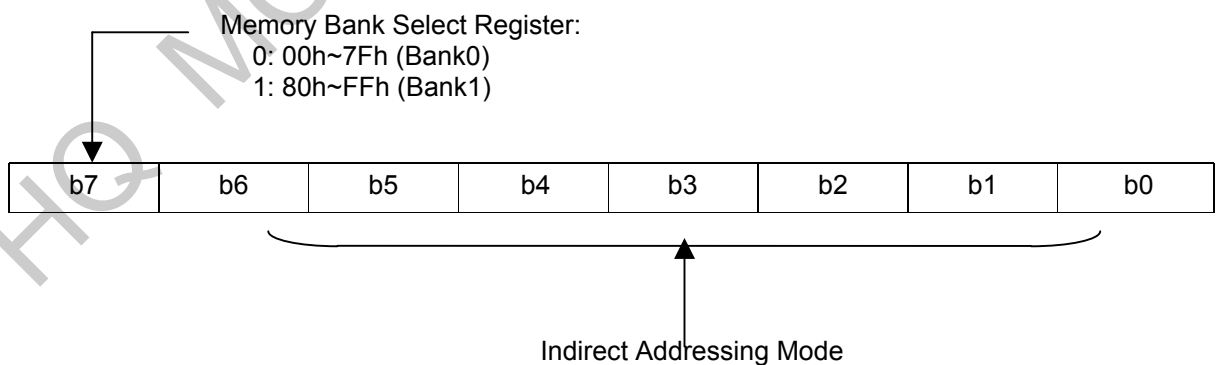
(3) PC (Program Counter): R02, R0A



(4) STATUS (Status register): R03

| Bit | Symbol | Function   |
|-----|--------|--|
| 0   | C      | Carry bit  |
| 1   | HC     | Half Carry bit   |
| 2   | Z      | Zero bit   |
| 3   | /PF    | Power down bit   |
| 4   | /TF    | WDT timer overflow bit   |
| 5   | RBS0   | Register Bank select bit<br>0: 00h~7Fh (Bank0)<br>1: 80h~FFh (Bank1) |
| 7~6 | --     | General purpose bit  |

(5) MSR (Memory Bank Select Register): R04



(6) PORT A: R05  
PA5~PA0, I/O Register

(7) PORT B: R06  
PB7~PB0, I/O Register

(8) PORT C: R07  
PC7~PC0, I/O Register

(9) PCHLAT: R0A

(10) INTS (Interrupt Status Register): R0B

| Bit | Symbol | Function  |
|-----|--------|---|
| 0   | RBIF   | PORT B change interrupt flag, Set when PB <7:4> inputs change             |
| 1   | INTF   | Set when INT interrupt occurs   |
| 2   | TIF    | Set when TMR0 overflows   |
| 3   | RBIE   | 0: Disable PB change interrupt<br>1: Enable PB change interrupt           |
| 4   | INTS   | 0: Disable INT interrupt<br>1: Enable INT interrupt                       |
| 5   | TIS    | 0: Disable TMR0 interrupt<br>1: Enable TMR0 interrupt                     |
| 6   | PEIE   | 0: Disable all peripheral interrupt<br>1: Enable all peripheral interrupt |
| 7   | GIS    | 0: Disable global interrupt<br>1: Enable global interrupt                 |

(11) PIFB1 (Peripheral Interrupt Flag Bit): R0C

| Bit | Symbol | Function   |
|-----|--------|--|
| 0   | TMR1IF | TMR1 interrupt flag<br>0: TMR1 did not overflow<br>1: TMR1 overflowed                                  |
| 1   | TMR2IF | TMR2 interrupt flag<br>0: No TMR2 to T2PER match occurred<br>1: TMR2 to T2PER match occurred           |
| 2   | CCP1IF | CCP1 interrupt flag<br>0: No TMR1 capture/compare occurred<br>1: A TMR1 capture/compare occurred       |
| 3   | SCMIF  | SCM interrupt flag<br>0: Waiting SCM transmit/receive<br>1: The SCM transmission/reception is complete |

| Bit | Symbol | Function   |
|-----|--------|--|
| 4   | TXIF   | USART transmit interrupt flag<br>0: The USART transmit buffer is full<br>1: The USART transmit buffer is empty |
| 5   | RCIF   | UASRT receive interrupt flag<br>0: The USART receive buffer is empty<br>1: The USART receive buffer is full    |
| 6   | ADIF   | A/D interrupt flag<br>0: A/D conversion is not complete<br>1: A/D conversion completed                         |
| 7   | --     | Unimplemented  |

(12) PIFB2 (Peripheral Interrupt Flag Bit): R0D

| Bit | Symbol | Function   |
|-----|--------|--|
| 0   | CCP2IF | CCP2 interrupt flag<br>0: No TMR1 capture/compare occurred<br>1: A TMR1 capture/compare occurred   |
| 1~3 | --     | Unimplemented  |
| 4   | EEIF   | EEIF : EEPROM Write Operation Interrupt Flag Bit.<br>0 = The EEPROM write operation is not completed or has not been start<br>1 = The EEPROM write operation completed (must be cleared in software) |
| 5~7 | --     | Unimplemented  |

(13) TMR1L: R0E

The LSB of the 16-bit TMR1

(14) TMR1H: R0F

The MSB of the 16-bit TMR1

(15) T1STA: R10

| Bit | Symbol  | Function   |
|-----|---------|--|
| 0   | TMR1ON  | 0: Stop TMR1<br>1: Enable TMR1                               |
| 1   | TMR1CLK | 0: Internal clock (Fosc/4)<br>1: External clock from pin PC0 |

| Bit | Symbol                  | Function  |
|-----|-------------------------|---|
| 2   | /T1SYNC                 | TMR1CLK = 1<br>0: Synchronize external clock<br>1: Do not synchronize external clock<br>TMR1CLK = 0 This bit is ignored |
| 3   | T1OSCEN                 | 0: TMR1 Oscillator is shut off<br>1: TMR1 Oscillator is enable  |
| 5~4 | T1CKPS1<br>~<br>T1CKPS0 | 1 1 = 1:8 Prescale value<br>1 0 = 1:4 Prescale value<br>0 1 = 1:2 Prescale value<br>0 0 = 1:1 Prescale value            |
| 7~6 | --                      | Unimplemented   |

(16) TMR2: R11

TMR2 register

(17) T2STA: R12

| Bit | Symbol                  | Function  |
|-----|-------------------------|---|
| 1~0 | T2CKPS1<br>~<br>T2CKPS0 | 0 0 = Prescaler is 1<br>0 1 = Prescaler is 4<br>1 x = Prescaler is 16 |
| 2   | TMR2ON                  | 0: TMR2 is off<br>1: TMR2 is on                                       |
| 7~3 | --                      | Unimplemented   |

(18) SCMBUF: R13

Serial communication port buffer

(19) SCMCTL: R14

| Bit | Symbol            | Function   |
|-----|-------------------|--|
| 3~0 | SCM3<br>~<br>SCM0 | 0 0 0 0: SCM master mode, clock = Fosc/4<br>0 0 0 1: SCM master mode, clock = Fosc/16<br>0 0 1 0: SCM master mode, clock = Fosc/64<br>0 0 1 1: SCM master mode, clock = TMR2 output/2<br>0 1 0 0: SCM slave mode, clock = SCK pin, SSB control enable<br>0 1 0 1: SCM slave mode, clock = SCK pin, SSB control disable |
| 4   | CKS               | 0: Transmit happens on rising edge, receive on falling edge, Idle state for clock is low level.<br>1: Transmit happens on falling edge, receive on rising edge, Idle state for clock is high level   |
| 5   | SCMEN             | 0: Disable SCM, then PC3, PC4, PC5 is I/O port.<br>1: Enable SCM   |
| 6   | SCMROI            | 0: No overflow<br>1: Overflow  |
| 7   | WCOL              | 0: No collision<br>1: The SCMBUF is written while it is still transmitting the previous word   |

(20) CCP1L: R15

Capture/Compare/PWM LSB

(21) CCP1H: R16

Capture/Compare/PWM MSB



(22) CCP1CTL: R17

| Bit | Symbol                | Function   |
|-----|-----------------------|--|
| 3~0 | CCP1M3<br>~<br>CCP1M0 | 0 0 0 0: CCP1 off<br>0 1 0 0: Capture1 mode, every falling edge<br>0 1 0 1: Capture1 mode, every rising edge<br>0 1 1 0: Capture1 mode, every 4 <sup>th</sup> rising edge<br>0 1 1 1: Capture1 mode, every 16 <sup>th</sup> rising edge<br>1 0 0 0: Compare1 mode, set output on match<br>1 0 0 1: Compare1 mode, clear output on match<br>1 0 1 0: Compare1 mode, generate software interrupt on match<br>1 0 1 1: Compare1 mode, trigger special event<br>1 1 x x: PWM1 mode |
| 5~4 | PWM1LSB               | These bits are the two LSBs of the PWM1 duty cycle   |
| 7~6 | --                    | Unimplemented  |

(23) RCSC: R18

| Bit | Symbol | Function  |
|-----|--------|---|
| 0   | RX9DF  | 9 <sup>th</sup> bit of received data                          |
| 1   | OERF   | 0: No overrun error<br>1: Overrun error                       |
| 2   | FERF   | 0: No framing error<br>1: Framing error                       |
| 3   | --     | Unimplemented   |
| 4   | CRENF  | 0: Disable continuous receive<br>1: Enable continuous receive |
| 5   | SRENF  | 0: Disable single receive<br>1: Enable single receive         |
| 6   | RX9ENF | 0: Select 8-bit reception<br>1: Select 9-bit reception        |
| 7   | SPENF  | 0: Serial port disable<br>1: Serial port enable               |

(24) TXREG: R19

USART transmit register

(25) RCREG: R1A  
 USART receive register

(26) CCP2L: R1B  
 Capture/Compare/PWM LSB

(27) CCP2H: R1C  
 Capture/Compare/PWM MSB

(28) CCP2CTL: R1D

| Bit | Symbol                | Function   |
|-----|-----------------------|--|
| 3~0 | CCP2M3<br>~<br>CCP2M0 | 0 0 0 0: CCP2 off<br>0 1 0 0: Capture2 mode, every falling edge<br>0 1 0 1: Capture2 mode, every rising edge<br>0 1 1 0: Capture2 mode, every 4 <sup>th</sup> rising edge<br>0 1 1 1: Capture2 mode, every 16 <sup>th</sup> rising edge<br>1 0 0 0: Compare2 mode, set output on match<br>1 0 0 1: Compare2 mode, clear output on match<br>1 0 1 0: Compare2 mode, generate software interrupt on match<br>1 0 1 1: Compare2 mode, trigger special event<br>1 1 x x: PWM2 mode |
| 5~4 | PWM2LSB               | These bits are the two LSBs of the PWM2 duty cycle   |
| 7~6 | --                    | Unimplemented  |

(29) ADRES: R1E  
 A/D result register high byte. The ADRES register is not a writable register.

(30) ADS0 ( A/D Status Register ): R1F

| Bit | Symbol   | Function  |
|-----|----------|---|
| 0   | ADRUN    | 0: A/D converter module is shut off and consumes no operating current<br>1: A/D converter module is operating |
| 1   | --       | Unimplemented   |
| 2   | GO/DONEB | 0: A/D conversion not in progress<br>1: A/D conversion in progress  |
| 5~3 | CHS2~0   | 000: AIC0 001: AIC1 010: AIC2 011: AIC3 100: AIC4   |
| 7~6 | ASCS1-0  | 00: fosc/2 01: fosc/8 10: fosc/32 11: f RC (*Note)  |

\*Note: determined by OSC mode, HF: fosc/32, XT: fosc/8, RC: fosc/2, LF: fosc/2

(31) TMR (Time Mode Register): R81

| Bit | Symbol | Function   |           |          |
|-----|--------|--|-----------|----------|
| 2~0 | PS2~0  | Prescaler Value  | RTCC rate | WDT rate |
|     |        | 0 0 0  | 1 : 2     | 1 : 1    |
|     |        | 0 0 1  | 1 : 4     | 1 : 2    |
|     |        | 0 1 0  | 1 : 8     | 1 : 4    |
|     |        | 0 1 1  | 1 : 16    | 1 : 8    |
|     |        | 1 0 0  | 1 : 32    | 1 : 16   |
|     |        | 1 0 1  | 1 : 64    | 1 : 32   |
|     |        | 1 1 0  | 1 : 128   | 1 : 64   |
|     |        | 1 1 1  | 1 : 256   | 1 : 128  |
| 3   | PSC    | Prescaler assignment bit<br>0: RTCC<br>1: Watchdog Timer   |           |          |
| 4   | TCE    | RTCC signal edge<br>0: Increment on low-to-high transition on RTCC pin<br>1: Increment on high-to-low transition on RTCC pin |           |          |
| 5   | TCS    | RTCC signal set<br>0: Internal instruction cycle clock<br>1: Transition on RTCC pin  |           |          |
| 6   | IES    | Interrupt edge select<br>0: Interrupt on falling edge on PB0<br>1: Interrupt on rising edge on PB0                           |           |          |
| 7   | PBPH   | PORTB7~0 pull-hi<br>0: PORTB7~0 pull-hi are enable<br>1: PORTB7~0 pull-hi are disable  |           |          |

(32) CPIO A (Control Port I/O Mode Register): R85

=“0”, I/O pin in output mode;

=“1”, I/O pin in input mode.

(33) CPIO B (Control Port I/O Mode Register): R86

=“0”, I/O pin in output mode;

=“1”, I/O pin in input mode.

(34) CPIO C (Control Port I/O Mode Register): R87

=“0”, I/O pin in output mode;

=“1”, I/O pin in input mode.

(35) PIEB1: R8C

| Bit | Symbol | Function   |
|-----|--------|--|
| 0   | TMR1IE | TMR1 interrupt enable bit<br>0: Disable TMR1 interrupt<br>1: Enable TMR1 interrupt |
| 1   | TMR2IE | TMR2 interrupt enable bit<br>0: Disable TMR2 interrupt<br>1: Enable TMR2 interrupt |

| Bit | Symbol | Function   |
|-----|--------|--|
| 2   | CCP1IE | CCP1 interrupt enable bit<br>0: Disable CCP1 interrupt<br>1: Enable CCP1 interrupt                                       |
| 3   | SCMIE  | SCM interrupt enable bit<br>0: Disable SCM interrupt<br>1: Enable SCM interrupt  |
| 4   | TXIE   | USART transmit interrupt enable bit<br>0: Disable the USART transmit interrupt<br>1: Enable the USART transmit interrupt |
| 5   | RCIE   | USART receive interrupt enable bit<br>0: Disable the USART receive interrupt<br>1: Enable the USART receive interrupt    |
| 6   | ADIE   | A/D interrupt enable bit<br>0: Disable A/D interrupt<br>1: Enable A/D interrupt  |
| 7   | --     | Unimplemented  |

(36) PIEB2: R8D

| Bit | Symbol | Function  |
|-----|--------|---|
| 0   | CCP2IE | 1:Enable CCP2 interrupt<br>0:Disable CCP2 interrupt                                     |
| 1~2 | --     | Unimplemented   |
| 4   | EEIE   | 1:Enable EEPROM Write Operation Interrupt<br>0:Disable EEPROM Write Operation Interrupt |
| 5~7 | --     | Unimplemented   |

(37) PSTA: R8E

| Bit | Symbol | Function  |
|-----|--------|---|
| 0   | PEDHB  | 0: Power edge-detector high level Reset occurred<br>1: No Power edge-detector high level Reset Occurred |
| 1   | PORB   | 0: Power on Reset occurred<br>1: No Power on Reset occurred   |
| 7~2 | --     | Unimplemented   |

(38) T2PER: R92  
Timer2 period

(39) SCMSTA: R94

| Bit | Symbol | Function                                       |
|-----|--------|--|
| 0   | BF     | 0: Receive not complete<br>1: Receive complete |
| 7~1 | --     | Unimplemented                                  |

(40) TXSC: R98

| Bit | Symbol | Function  |
|-----|--------|---|
| 0   | TX9DF  | 9 <sup>th</sup> bit of transmit data                    |
| 1   | TSRCF  | 0: TSR full<br>1: TSR empty                             |
| 2   | HBRCF  | 0: Low speed<br>1: High speed                           |
| 3   | --     | Unimplemented   |
| 4   | UMSF   | 0: USART asynchronous mode<br>1: USART synchronous mode |
| 5   | TXENF  | 0: Transmit disable<br>1: Transmit enable               |
| 6   | TX9ENF | 0: Select 8-bit reception<br>1: Select 9-bit reception  |
| 7   | CSSF   | 0: Slave mode<br>1: Master mode                         |

(41) BRREG: R99  
Baud rate register

(42) 9AH : EEPROM data register.

(43) 9BH : EEPROM address register.

(44) 9CH : EEPROM control register 1.

| Bit | Symbol | Function  |
|-----|--------|---|
| 0   | RD     | Read Control Bit.<br>0 = Does not initiate an EEPROM read.<br>1 = Initiates an EEPROM read (read takes once cycle. RD is cleared in hardware. The RD bit can only be set (not clear) in software.)                |
| 1   | WR     | Write Control Bit.<br>0 = Write cycle to the data EEPROM is complete<br>1 = Initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not clear) in software.) |
| 2   | WREN   | EEPROM Write Enable Bit.<br>0 = Inhibits write to the data EEPROM<br>1 = Allows write cycles  |
| 3   | WRERR  | EEPROM Write Error Flag Bit.<br>0 = The EEPROM write operation completed<br>1 = The EEPROM write operation is prematurely terminated (any MCLR reset or any WDT reset during normal operation)                    |

(45) 9DH : EEPROM control register 2.

Write only ; Read as "0"

When write data to the EEPROM must write 55/H to EECON2, and writ AA/H to EECON2 then set WR bit; the EEPROM can write data inside for write each byte.

Example : Data EEPROM Write

```

BSR    STATUS,PAGE    ;Select bank1
BCR    INTS,GIS       ;Disable interrupt
BSR    EECON1,WREN    ;Enable write
LDWI   55H
STWR   EECON2         ;Write 55/H
LDWI   0AAH
STWR   EECON2         ;Write AA/H
BSR    EECON1,WR      ;Begin write
    
```

(46) ADS1 (A/D Status Register): R9F

| Bit | Symbol  | Function   |
|-----|---------|--|
| 2~0 | PAVM2~0 | 0 0 0: PA0~3,PA5 = analog input. VREF = VDD<br>0 0 1: PA0~2,PA5 = analog input. PA3 = ref input, VREF = PA3<br>0 1 0: PA0~3,PA5 = analog input. VREF = VDD<br>0 1 1: PA0~2,PA5 = analog input. PA3 = ref input, VREF = PA3<br>1 0 0: PA0, 1, 3 = analog input. PA2, 5 = digital I/O, VREF = VDD<br>1 0 1: PA0, 1 = analog input. PA2, 5 = digital I/O, VREF = PA3<br>1 1 x: PA0~3, 5 = digital I/O |
| 7~3 | --      | Unimplemented  |

(47) Configurable options (Set by writer)

| Oscillator Type |
|-----------------|
| RC Oscillator   |
| HFXT Oscillator |
| XTAL Oscillator |
| LFXT Oscillator |

| Watchdog Timer control              |
|-------------------------------------|
| Watchdog timer disable all the time |
| Watchdog timer enable all the time  |

| Oscillator-start Timer control |
|--------------------------------|
| 0ms                            |
| 75ms                           |

| Power-edge Detect |
|-------------------|
| PED Disable       |
| Low level         |
| Middle level      |
| High level        |

| Security state   |
|------------------|
| Security Disable |
| Security Enable  |

(B) Program Memory

| Address | Description   |
|---------|---|
| 000-FFF | Program memory  |
| 000     | The starting address of power on, external reset or WDT time-out reset. |
| 004     | Interrupt vector  |

**8. Reset Condition for all Registers**

| Register | Address | Power-On Reset | /MCLR or WDT Reset | Wake-up from SLEEP |
|----------|---------|----------------|--------------------|--------------------|
| IAR      | 00h     | N/A            | N/A                | N/A                |
| RTCC     | 01h     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| PC       | 0Ah,02h | 0000 0000 0000 | 0000 0000 0000     | PC+1               |
| STATUS   | 03h     | 0001 1xxx      | 000# #uuu          | 000# #uuu          |
| MSR      | 04h     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| PORT A   | 05h     | --xx xxxx      | --uu uuuu          | --uu uuuu          |
| PORT B   | 06h     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| PORT C   | 07h     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| PCHLAT   | 0Ah     | ---0 0000      | ---0 0000          | ---u uuuu          |
| INTS     | 0Bh     | 0000 000x      | 0000 000u          | uuuu uuuu          |
| PIFB1    | 0Ch     | -000 0000      | -000 0000          | -uuu uuuu          |
| PIFB2    | 0Dh     | ---- ---0      | ---- ---0          | ---- ---u          |
| TMR1L    | 0Eh     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| TMR1H    | 0Fh     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| T1STA    | 10h     | --00 0000      | --uu uuuu          | --uu uuuu          |
| TMR2     | 11h     | 0000 0000      | 0000 0000          | uuuu uuuu          |
| T2STA    | 12h     | ---- -000      | ---- -uuu          | ---- -uuu          |
| SCMBUF   | 13h     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| SCMCTL   | 14h     | 0000 0000      | 0000 0000          | uuuu uuuu          |
| CCP1L    | 15h     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| CCP1H    | 16h     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| CCP1CTL  | 17h     | --00 0000      | --00 0000          | --uu uuuu          |
| RCSC     | 18h     | 0000 -00x      | 0000 -00x          | uuuu -uuu          |
| TXREG    | 19h     | 0000 0000      | 0000 0000          | uuuu uuuu          |
| RCREG    | 1Ah     | 0000 0000      | 0000 0000          | uuuu uuuu          |
| CCP2L    | 1Bh     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| CCP2H    | 1Ch     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |



| Register | Address | Power-On Reset | /MCLR or WDT Reset | Wake-up from SLEEP |
|----------|---------|----------------|--------------------|--------------------|
| CCP2CTL  | 1Dh     | --00 0000      | --00 0000          | --uu uuuu          |
| ADRES    | 1Eh     | xxxx xxxx      | uuuu uuuu          | uuuu uuuu          |
| ADS0     | 1Fh     | 0000 00-0      | 0000 00-0          | uuuu uu-u          |
| TMR      | 81h     | 1111 1111      | 1111 1111          | uuuu uuuu          |
| CPIOA    | 85h     | --11 1111      | --11 1111          | --uu uuuu          |
| CPIOB    | 86h     | 1111 1111      | 1111 1111          | uuuu uuuu          |
| CPIOC    | 87h     | 1111 1111      | 1111 1111          | uuuu uuuu          |
| PIEB1    | 8Ch     | -000 0000      | -000 0000          | -uuu uuuu          |
| PSTA     | 8Eh     | ---- --0u      | ---- --uu          | ---- --uu          |
| T2PER    | 92h     | 1111 1111      | 1111 1111          | 1111 1111          |
| SCMSTA   | 94h     | ---- ---0      | ---- ---0          | ---- ---u          |
| PBPHR    | 95h     | 1111 1111      | 1111 1111          | uuuu uuuu          |
| PCPHR    | 96h     | 1111 1111      | 1111 1111          | uuuu uuuu          |
| TXSC     | 98h     | 0000 -010      | 0000 -010          | uuuu -uuu          |
| BRREG    | 99h     | 0000 0000      | 0000 0000          | uuuu uuuu          |
| EEDATA   | 9Ah     | 0000 0000      | 0000 0000          | uuuu uuuu          |
| EEADR    | 9Bh     | -000 0000      | -000 0000          | -uuu uuuu          |
| EECON1   | 9Ch     | ---- x000      | ---- #000          | ---- #uuu          |
| EECON2   | 9Dh     | ---- ----      | ---- ----          | ---- ----          |
| ADS1     | 9Fh     | ---- -000      | ---- -000          | ---- -uuu          |

Note : u=unchanged, x=unknown, - =unimplemented, read as "0"

#= value depends on the condition of the following table

| Condition                      | Status: bit 4 | Status: bit 3 | PSTA: bit 1 | PSTA: bit 0 |
|--------------------------------|---------------|---------------|-------------|-------------|
| /MCLR reset (not during SLEEP) | u             | u             | u           | u           |
| /MCLR reset during SLEEP       | 1             | 0             | u           | u           |
| WDT reset (not during SLEEP)   | 0             | 1             | u           | u           |
| WDT reset during SLEEP         | 0             | 0             | u           | u           |
| Power-on reset                 | 1             | 1             | 0           | x           |
| Power-range reset              | 1             | 1             | u           | 0           |

Note : u=unchanged, x=unknown, - =unimplemented, read as "0"

**9. Instruction Set**

| Instruction Code | Mnemonic Operands | Function                         | Operating                       | Status   |
|------------------|-------------------|----------------------------------|---------------------------------|----------|
| 010000 00000000  | NOP               | No operation                     | None                            |          |
| 010000 00000001  | CLRWT             | Clear Watchdog timer             | 0→WT                            | TF, PF   |
| 010000 00000010  | SLEEP             | Sleep mode                       | 0→WT, stop OSC                  | TF, PF   |
| 010000 00000011  | TMODE             | Load W to TMODE register         | W→TMODE                         | None     |
| 010000 00000100  | RET               | Return from subroutine           | Stack→PC                        | None     |
| 010000 00000rrr  | CPIO R            | Control I/O port register        | W→CPIO R                        | None     |
| 010001 1rrrrrrr  | STWR R            | Store W to register              | W→R                             | None     |
| 011000 trrrrrrr  | LDR R, t          | Load register                    | R→t                             | Z        |
| 111010 iiiiii    | LDWI i            | Load immediate to W              | i→W                             | None     |
| 010111 trrrrrrr  | SWAPR R, t        | Swap halves register             | [R(0~3)<br>↔R(4~7)]→t           | None     |
| 011001 trrrrrrr  | INCR R, t         | Increment register               | R + 1→t                         | Z        |
| 011010 trrrrrrr  | INCRSZ R, t       | Increment register, skip if zero | R + 1→t                         | None     |
| 011011 trrrrrrr  | ADDWR R, t        | Add W and register               | W + R→t                         | C, HC, Z |
| 011100 trrrrrrr  | SUBWR R, t        | Subtract W from register         | R - W→t or<br>(R+/W+1→t)        | C, HC, Z |
| 011101 trrrrrrr  | DECR R, t         | Decrement register               | R - 1→t                         | Z        |
| 011110 trrrrrrr  | DECRSZ R, t       | Decrement register, skip if zero | R - 1→t                         | None     |
| 010010 trrrrrrr  | ANDWR R, t        | AND W and register               | R ∩ W→t                         | Z        |
| 110100 iiiiii    | ANDWI i           | AND W and immediate              | i ∩ W→W                         | Z        |
| 010011 trrrrrrr  | IORWR R, t        | Inclu. OR W and register         | R ∪ W→t                         | Z        |
| 110101 iiiiii    | IORWI i           | Inclu. OR W and immediate        | i ∪ W→W                         | Z        |
| 010100 trrrrrrr  | XORWR R, t        | Exclu. OR W and register         | R ⊕ W→t                         | Z        |
| 110110 iiiiii    | XORWI i           | Exclu. OR W and immediate        | i ⊕ W→W                         | Z        |
| 011111 trrrrrrr  | COMR R, t         | Complement register              | /R→t                            | Z        |
| 010110 trrrrrrr  | RRR R, t          | Rotate right register            | R(n) →R(n-1),<br>C→R(7), R(0)→C | C        |
| 010101 trrrrrrr  | RLR R, t          | Rotate left register             | R(n)→r(n+1),<br>C→R(0), R(7)→C  | C        |
| 010000 1xxxxxxx  | CLRW              | Clear working register           | 0→W                             | Z        |
| 010001 0rrrrrrr  | CLRR R            | Clear register                   | 0→R                             | Z        |
| 0000bb brrrrrrr  | BCR R, b          | Bit clear                        | 0→R(b)                          | None     |
| 0010bb brrrrrrr  | BSR R, b          | Bit set                          | 1→R(b)                          | None     |
| 0001bb brrrrrrr  | BTSC R, b         | Bit Test, skip if clear          | Skip if R(b)=0                  | None     |
| 0011bb brrrrrrr  | BTSS R, b         | Bit Test, skip if set            | Skip if R(b)=1                  | None     |
| 100nnn nnnnnnnn  | LCALL n           | Long CALL subroutine             | n→PC,<br>PC+1→Stack             | None     |

| Instruction Code | Mnemonic Operands | Function                     | Operating      | Status |
|------------------|-------------------|------------------------------|----------------|--------|
| 101nnn nnnnnnnn  | LJUMP n           | Long JUMP to address         | n→PC           | None   |
| 110111 iiiiii    | ADDWI i           | Add immediate to W           | W+i→W          | C,HC,Z |
| 110001 iiiiii    | RTWI i            | Return, place immediate to W | Stack→PC,i→W   | None   |
| 111000 iiiiii    | SUBWI i           | Subtract W from immediate    | i-W→W          | C,HC,Z |
| 010000 00001001  | RTFI              | Return from interrupt        | Stack→PC,1→GIS | None   |

Note :

|        |                             |    |                             |
|--------|-----------------------------|----|-----------------------------|
| W      | : Working register          | b  | : Bit position              |
| WT     | : Watchdog timer            | t  | : Target                    |
| TMODE  | : TMODE mode register       | 0  | : Working register          |
| CPIO   | : Control I/O port register | 1  | : General register          |
| TF     | : Timer overflow flag       | R  | : General register address  |
| PF     | : Power loss flag           | C  | : Carry flag                |
| PC     | : Program Counter           | HC | : Half carry                |
| OSC    | : Oscillator                | Z  | : Zero flag                 |
| Inclu. | : Inclusive 'U'             | /  | : Complement                |
| Exclu. | : Exclusive '⊕'             | x  | : Don't care                |
| AND    | : Logic AND '∩'             | i  | : Immediate data ( 8 bits ) |
|        |                             | n  | : Immediate address         |

## 10. Electrical Characteristics

\*Note: Temperature=25°C

### 1. Operation Current:

(1) HF (C=10p), WDT – disable, PRD – disable

|      | 4M    | 10M   | 20M   | Sleep |
|------|-------|-------|-------|-------|
| 2.5V | 500uA | 1.1mA | 2.2mA | 1uA   |
| 3.0V | 700uA | 1.4mA | 2.6mA | 1uA   |
| 4.0V | 1.1mA | 2.1mA | 4.1mA | 1uA   |
| 5.0V | 1.6mA | 3.1mA | 5.4mA | 1uA   |
| 5.5V | 1.9mA | 4.2mA | 6.9mA | 1uA   |

These parameters are for reference only.

(2) XT (C=10p), WDT – disable, PRD – disable

|      | 1M    | 4M    | 10M   | Sleep |
|------|-------|-------|-------|-------|
| 2.5V | 150uA | 500uA | 1.2mA | 1uA   |
| 3.0V | 180uA | 600uA | 1.5mA | 1uA   |
| 4.0V | 420uA | 950uA | 2.2mA | 1uA   |
| 5.0V | 720uA | 1.5mA | 3.2mA | 1uA   |
| 5.5V | 960uA | 1.8mA | 3.6mA | 1uA   |

These parameters are for reference only.

(3) LF (C=10p), WDT – disable, PRD – disable

|      | 32K   | 455K  | 1M    | Sleep |
|------|-------|-------|-------|-------|
| 2.5V | 40uA  | 100uA | 190uA | 1uA   |
| 3.0V | 50uA  | 140uA | 230uA | 1uA   |
| 4.0V | 100uA | 240uA | 440uA | 1uA   |
| 5.0V | 200uA | 480uA | 630uA | 1uA   |
| 5.5V | 290uA | 650uA | 950uA | 1uA   |

These parameters are for reference only.

(4) RC, WDT – disable, PRD – disable, @VDD = 5.0V

| C    | R    | Freq. | Current |
|------|------|-------|---------|
| 3p   | 4.7k | 9.5M  | 4.2mA   |
|      | 10k  | 5.1M  | 2.2mA   |
|      | 47k  | 1.2M  | 650uA   |
|      | 100k | 550K  | 450uA   |
|      | 300k | 190K  | 300uA   |
|      | 470k | 120K  | 250uA   |
| 20p  | 4.7k | 4.2M  | 1.9mA   |
|      | 10k  | 2.2M  | 1.5mA   |
|      | 47k  | 520K  | 500uA   |
|      | 100k | 250K  | 350uA   |
|      | 300k | 80K   | 250uA   |
|      | 470k | 50K   | 200uA   |
| 100p | 4.7k | 1.3M  | 1.3mA   |
|      | 10k  | 700K  | 700uA   |
|      | 47k  | 150K  | 320uA   |
|      | 100k | 70K   | 270uA   |
|      | 300k | 22K   | 240uA   |
|      | 470k | 15K   | 220uA   |
| 300p | 4.7k | 570K  | 990uA   |
|      | 10k  | 270K  | 670uA   |
|      | 47k  | 60K   | 280uA   |
|      | 100k | 30K   | 230uA   |
|      | 300k | 8K    | 220uA   |
|      | 470k | 6K    | 210uA   |

These parameters are for reference only.

(5) RC, WDT – disable, PRD – disable, @VDD = 3.0V

| C    | R    | Freq. | Current |
|------|------|-------|---------|
| 3p   | 4.7k | 9.5M  | 1.8mA   |
|      | 10k  | 5.5M  | 1.1mA   |
|      | 47k  | 1.4M  | 300uA   |
|      | 100k | 680K  | 160uA   |
|      | 300k | 232K  | 80uA    |
|      | 470k | 147K  | 80uA    |
| 20p  | 4.7k | 5.1M  | 990uA   |
|      | 10k  | 2.8M  | 550uA   |
|      | 47k  | 6.7M  | 170uA   |
|      | 100k | 325K  | 100uA   |
|      | 300k | 110K  | 60uA    |
|      | 470k | 65K   | 60uA    |
| 100p | 4.7k | 1.8M  | 700uA   |
|      | 10k  | 950K  | 350uA   |
|      | 47k  | 210K  | 100uA   |
|      | 100k | 110K  | 80uA    |
|      | 300k | 35K   | 60uA    |
|      | 470k | 20K   | 60uA    |
| 300p | 4.7k | 820K  | 620uA   |
|      | 10k  | 417K  | 200uA   |
|      | 47k  | 75K   | 100uA   |
|      | 100k | 52K   | 66uA    |
|      | 300k | 42K   | 55uA    |
|      | 470k | 40K   | 48uA    |

These parameters are for reference only.

2. Input Voltage (VDD = 5V):

|     | PA~PC           | Min   | Max   |
|-----|-----------------|-------|-------|
| Vil | TTL             | VSS   | 1.45V |
|     | Schmitt trigger | VSS   | 1.21V |
| Vih | TTL             | 1.55V | VDD   |
|     | Schmitt trigger | 3.06V | VDD   |

These parameters are for reference only.

Input Voltage (VDD = 3V):

|     | PA~PC           | Min  | Max   |
|-----|-----------------|------|-------|
| Vil | TTL             | VSS  | 1.03V |
|     | Schmitt trigger | VSS  | 0.95V |
| Vih | TTL             | 1.1V | VDD   |
|     | Schmitt trigger | 1.7V | VDD   |

These parameters are for reference only.

3. Output Voltage (VDD = 5V):

|     | PA~PC | Condition   |
|-----|-------|-------------|
| Voh | 3.3V  | Ioh = -20mA |
| Vol | 0.5V  | Iol = 20mA  |
| Voh | 4.5V  | Ioh = -5mA  |
| Vol | 0.2V  | Iol = 5mA   |

These parameters are for reference only.

Output Voltage (VDD = 3V):

|     | PA~PC | Condition   |
|-----|-------|-------------|
| Voh | 1.5V  | Ioh = -10mA |
| Vol | 0.3V  | Iol = 10mA  |
| Voh | 2.4V  | Ioh = -5mA  |
| Vol | 0.2V  | Iol = 5mA   |

These parameters are for reference only.

4. Output Current (Max.) (VDD = 5V):

|                | Current |
|----------------|---------|
| Source current | 6mA     |
| Sink current   | 18mA    |

These parameters are for reference only.

5. The basic WDT time-out cycle time:

|      | Time |
|------|------|
| 2.5V | 35ms |
| 3.0V | 30ms |
| 4.0V | 28ms |
| 5.0V | 25ms |
| 5.5V | 23ms |

These parameters are for reference only.

6. PRD:

(1) PRD reset voltage:

|     |          |
|-----|----------|
|     | Voltage  |
| Vih | 4.2V±10% |
| Vil | 3.8V±10% |

These parameters are for reference only.

(2) PRD reset current:

|      |         |
|------|---------|
|      | Current |
| 5.0V | 120uA   |
| 4.0V | 100uA   |

These parameters are for reference only.

7. Pull high resistor:

|       |          |           |
|-------|----------|-----------|
| VDD   | 5V       | 3V        |
| PB7~0 | 50KΩ±20% | 100KΩ±20% |

These parameters are for reference only.

8. MCLR filter time:

|      |            |
|------|------------|
| VDD  | 5V         |
| Time | 1000ns±20% |

These parameters are for reference only.



扫一扫 关注公众号



扫一扫 关注阿里旺铺

联系我们  
 深圳市华琦微科技有限公司  
 SHENZHEN HUAQIWEI TECHNOLOGY CO., LTD  
 WEB: www.hqwtech.com  
 TEL: 0755-88603251  
 FAX: 0755-88609209  
 ADDRESS: 深圳市福田区深南中路嘉汇新城汇商中心2727