TPS61087-Q1 650-kHz or 1.2-MHz, 18.5-V Step-Up DC-DC Converter With 3.2-A Switch

1 Features

- Qualified for Automotive Applications
- 2.5-V to 6-V Input Voltage Range
- 18.5-V Boost Converter With 3.2-A Switch Current
- 650-kHz or 1.2-MHz Selectable Switching Frequency
- Adjustable Soft Start
- Thermal Shutdown
- Undervoltage Lockout
- 10-Pin VQFN Package with Wettable Flanks

2 Applications

- Automotive Infotainment Clusters
  - Instrument Clusters, Head Units
  - Radio, Navigation
  - Audio Amplifiers
- Automotive Body Electronics
  - Body Control Modules
  - Gateway
- Telemetrics and eCall
- Advanced Driver Assistance System (ADAS)

3 Description

The TPS61087-Q1 is a high-frequency, high-efficiency DC-to-DC converter with an integrated 3.2-A, 0.13-Ω power switch capable of providing an output voltage up to 18.5 V. The selectable frequency of 650 kHz or 1.2 MHz allows the use of small external inductors and capacitors, and provides fast transient response. The external compensation allows optimizing the application for specific conditions. A capacitor connected to the soft-start pin minimizes inrush current at start-up.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61087-Q1	VSON (10)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

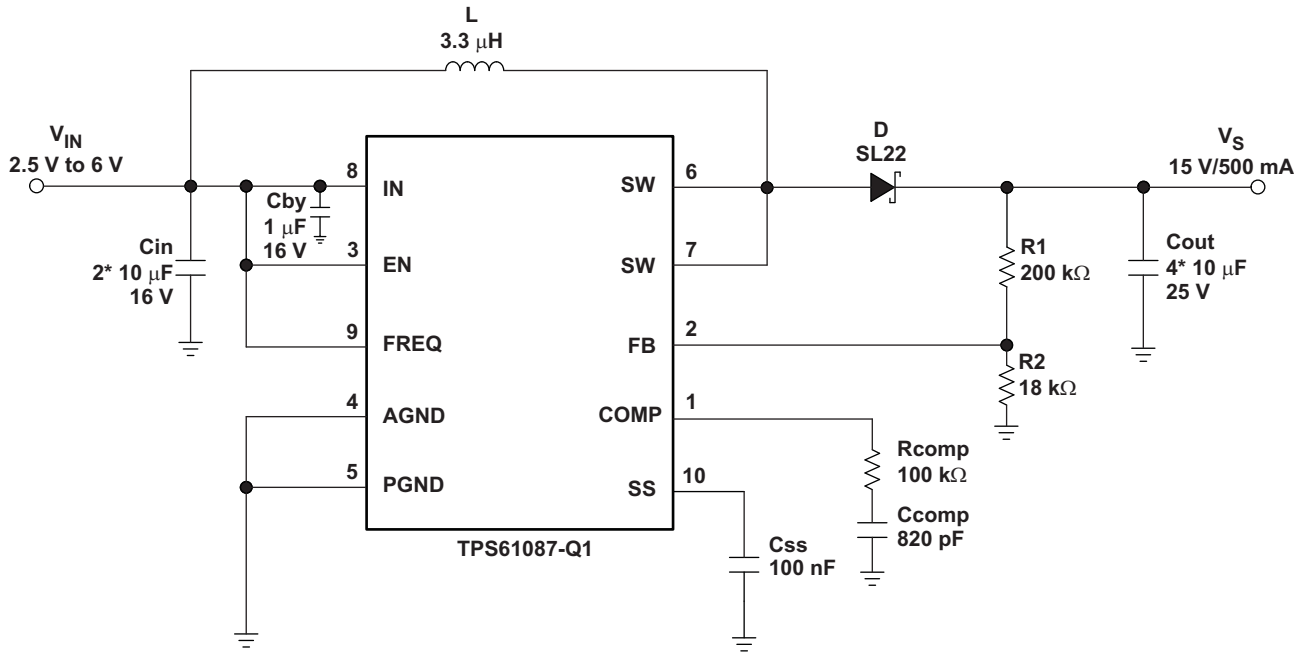


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2016) to Revision B **Page**

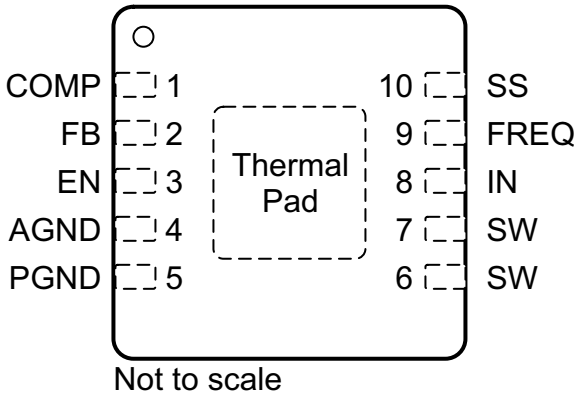
- Changed *ESD Ratings* table to use AEC-Q100 specification ... 4
- Added the *Documentation Support* and *Receiving Notification of Documentation Updates* sections ... 22

Changes from Original (December 2011) to Revision A **Page**

- Added *Applications* section, *Device Information* table, *Table of Contents*, *Revision History* section, *Specifications* section, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DRC and WDRC Packages
10 Pin VSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	1	I/O	Compensation pin
FB	2	I	Feedback pin
EN	3	I	Shutdown control input. Connect this pin to logic high level to enable the device
AGND	4	—	Analog ground
PGND	5	—	Power ground
SW	6, 7	I	Switch pin
IN	8	I	Input supply pin
FREQ	9	I	Frequency select pin. The power switch operates at 650 kHz if FREQ is connected to GND and at 1.2 MHz if FREQ is connected to IN
SS	10	O	Soft-start control pin. Connect a capacitor to this pin if soft start is needed. Open = no soft start
Thermal Pad		—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Input voltage range(2)	IN	–0.3	7	V
Voltage range	EN, FB, SS, FREQ, COMP	–0.3	7	V
	SW	–0.3	20	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	2.5	6	V
V_S	Boost output voltage range	V_{IN} + 0.5	18.5	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS61087-Q1		UNIT
		DRC (VSON)	WDRC (VSON)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57	51.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.5	81.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	26.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.9	4.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.6	26.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = 5 V, EN = V_{IN}, V_S = 15 V, T_A = T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		6	V
I_Q	Operating quiescent current into IN pin	Device not switching, V_{FB} = 1.3 V		75	100	µA
I_{SDVIN}	Shutdown current into IN pin	EN = GND			4	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling			2.4	V
		V_{IN} rising			2.5	V
T_{SD}	Thermal shutdown	Temperature rising		150		°C
T_{SDHYS}	Thermal shutdown hysteresis			14		°C
LOGIC SIGNALS EN, FREQ						
V_{IH}	High level input voltage	V_{IN} = 2.5 V to 6 V	2			V
V_{IL}	Low level input voltage	V_{IN} = 2.5 V to 6 V			0.5	V
I_{INLEAK}	Input leakage current	EN = FREQ = GND			0.1	µA

Electrical Characteristics (continued)

V_{IN} = 5 V, EN = V_{IN}, V_S = 15 V, T_A = T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONVERTER						
V_S	Boost output voltage		V_{IN} + 0.5		18.5	V
V_{FB}	Feedback regulation voltage		1.23	1.238	1.25	V
gm	Transconductance error amplifier			107		µA/V
I_{FB}	Feedback input bias current	V_{FB} = 1.238 V			0.1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 5 V, I_{SW} = current limit		0.13	0.18	Ω
		V_{IN} = V_{GS} = 3 V, I_{SW} = current limit		0.16	0.23	
I_{SWLEAK}	SW leakage current	EN = GND, V_{SW} = V_{IN} = 6 V			2	µA
I_{LIM}	N-Channel MOSFET current limit		3.2	4	4.8	A
I_{SS}	Soft-start current	V_{SS} = 1.238 V	7	10	13	µA
f_S	Oscillator frequency	FREQ = V_{IN}	0.9	1.2	1.5	MHz
		FREQ = GND	480	650	820	kHz
	Line regulation	V_{IN} = 2.5 V to 6 V, I_{OUT} = 10 mA		0.0002		%/V
	Load regulation	V_{IN} = 5 V, I_{OUT} = 1 mA to 1 A		0.11		%/A

6.6 Typical Characteristics

The typical characteristics are measured with the inductors 7447789003 3.3 µH (high frequency) or 74454068 6.8 µH (low frequency) from Wurth and the rectifier diode SL22.

Table 1. Table of Graphs

			FIGURE
$I_{OUT(max)}$	Maximum load current	vs Input voltage at High frequency (1.2 MHz)	Figure 1
$I_{OUT(max)}$	Maximum load current	vs Input voltage at Low frequency (650 kHz)	Figure 2
η	Efficiency	vs Load current, V_S = 15 V, V_{IN} = 5 V	Figure 3
		vs Load current, V_S = 9 V, V_{IN} = 3.3 V	Figure 4
	Supply current	vs Supply voltage	Figure 5
	Oscillator frequency	vs Load current	Figure 6
	Oscillator frequency	vs Supply voltage	Figure 7

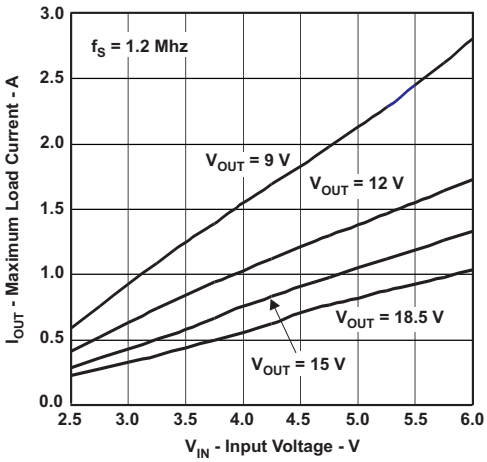


Figure 1. Maximum Load Current vs Input Voltage

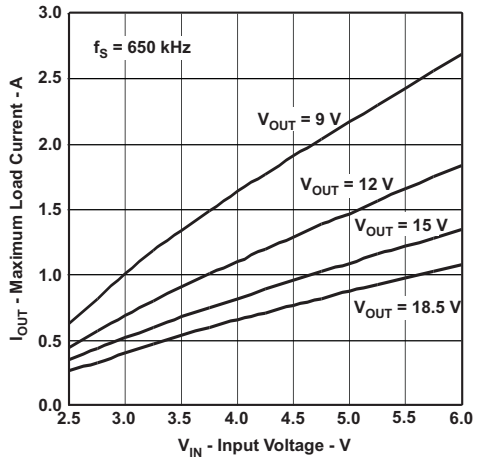


Figure 2. Maximum Load Current vs Input Voltage

Typical Characteristics (continued)

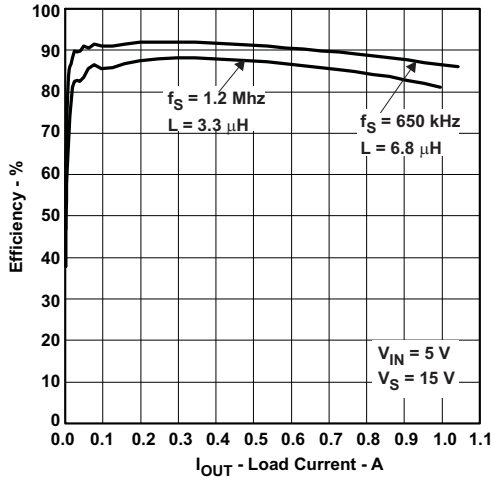


Figure 3. Efficiency vs Load Current

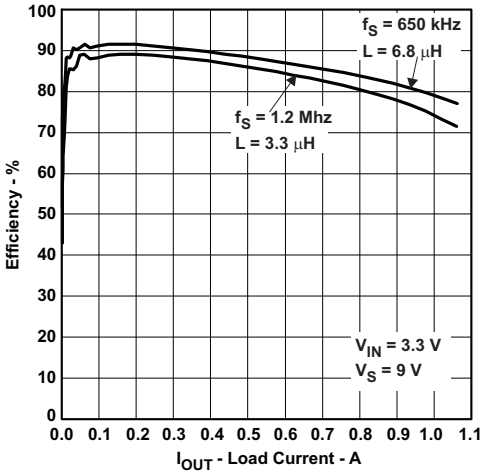


Figure 4. Efficiency vs Load Current

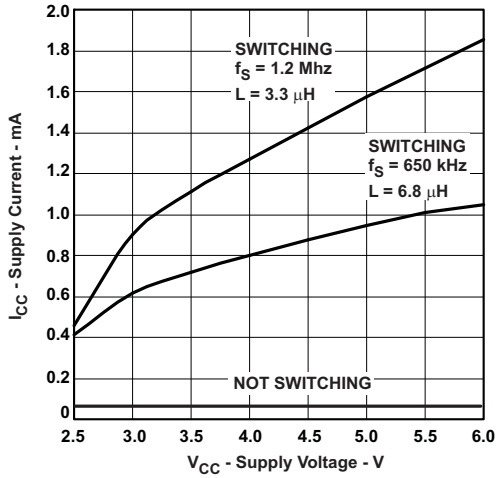


Figure 5. Supply Current vs Supply Voltage

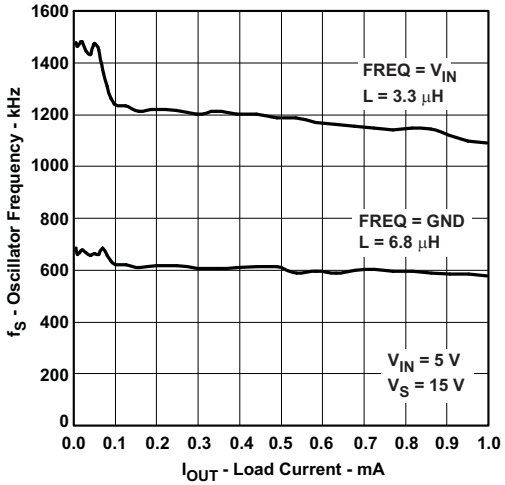


Figure 6. Oscillator Frequency vs Load Current

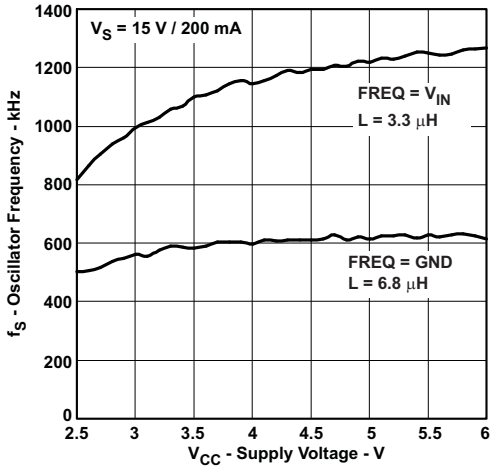


Figure 7. Oscillator Frequency vs Supply Voltage

7 Detailed Description

7.1 Overview

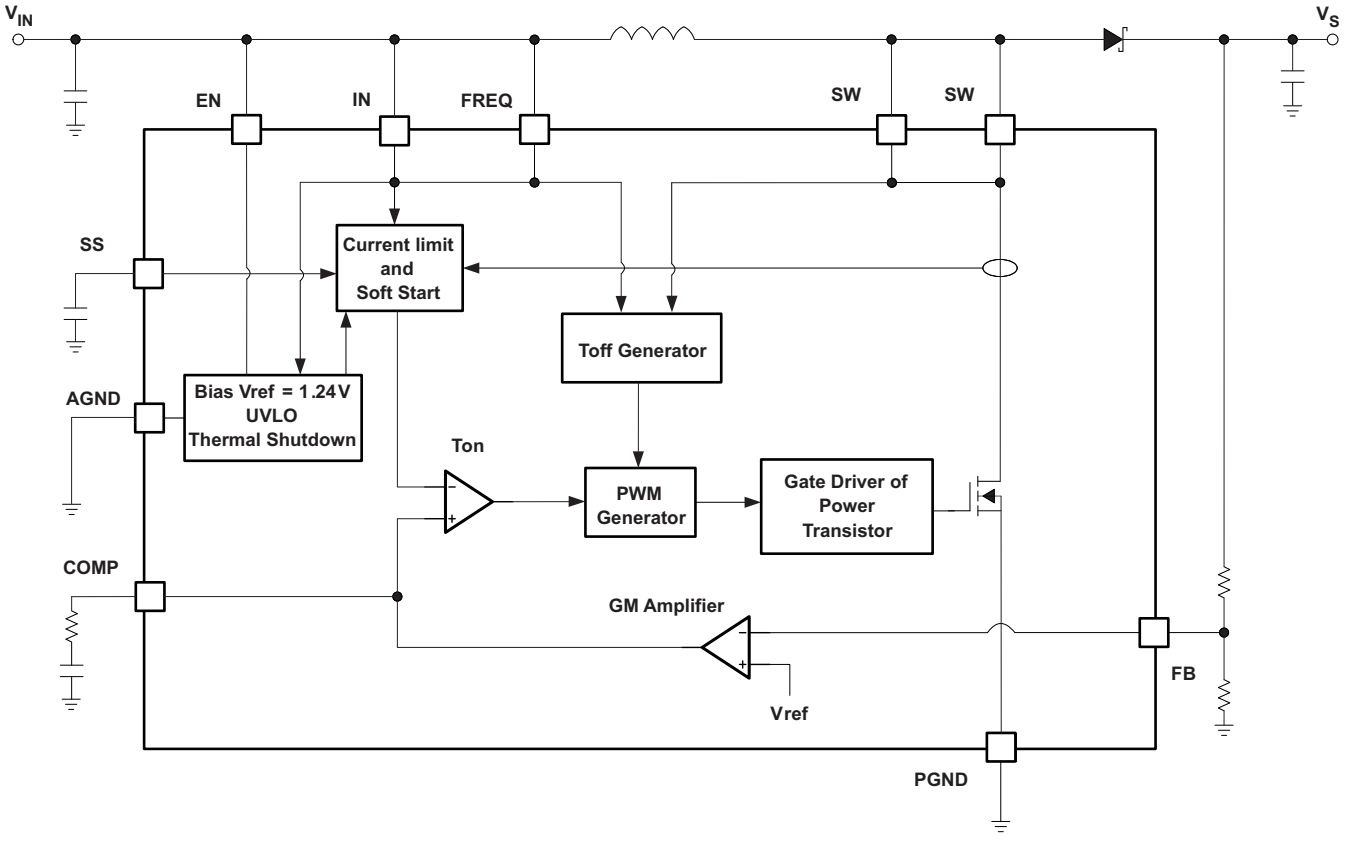
The TPS61087-Q1 boost converter is designed for output voltages up to 18.5 V with a switch peak current limit of 3.2-A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is selectable from 650 kHz to 1.2 MHz and the minimum input voltage is 2.5 V. To limit the inrush current at start-up a soft-start pin is available.

TPS61087-Q1 boost converter's novel topology using adaptive OFF-time provides superior load and line transient responses and operates also over a wider range of applications than conventional converters.

The selectable switching frequency offers the possibility to optimize the design either for the use of small sized components (1.2 MHz) or for higher system efficiency (650 kHz). However, the frequency changes slightly because the voltage drop across the $r_{DS(on)}$ has some influence on the current and voltage measurement and thus on the ON-time (the OFF-time remains constant).

Depending on the load current, the converter operates in continuous conduction mode (CCM), discontinuous conduction mode (DCM), or pulse skip mode to maintain the output voltage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start

The boost converter has an adjustable soft start to prevent high inrush current during start-up. To minimize the inrush current during start-up an external capacitor, connected to the SS pin and charged with a constant current, is used to slowly ramp up the internal current limit of the boost converter. When the EN pin is pulled high, the soft-start capacitor (C_{SS}) is immediately charged to 0.3 V. The capacitor is then charged at a constant current of 10 µA typically until the output of the boost converter V_S has reached its Power Good threshold (roughly 98% of V_S nominal value). During this time, the SS voltage directly controls the peak inductor current, starting with 0 A at V_{SS} = 0.3 V up to the full current limit at V_{SS} = 800 mV. The maximum load current is available after the soft start is completed. As the size of the capacitor increases the ramp of the current limit slows and the soft-start time increases. A 100-nF capacitor is usually sufficient for most of the applications. When the EN pin is pulled low, the soft-start capacitor is discharged to ground.

7.3.2 Frequency Select Pin (FREQ)

The switching frequency of the device is set using the frequency select pin (FREQ) to 650 kHz (FREQ = low) or 1.2 MHz (FREQ = high). Higher switching frequency improves load transient response but slightly reduces the efficiency. Another benefit of higher switching frequency is a lower output ripple voltage. Unless light load efficiency is a major concern, TI recommends using a 1.2-MHz switching frequency.

7.3.3 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout is included, which disables the device if the input voltage falls below 2.4 V.

7.3.4 Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically the thermal shutdown happens at a junction temperature of 150°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 136°C. Then the device starts switching again.

7.3.5 Overvoltage Prevention

If overvoltage is detected on the FB pin (typically 3% above the nominal value of 1.238 V) the part stops switching immediately until the voltage on this pin drops to its nominal value. This prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

7.4 Device Functional Modes

The converter operates in continuous conduction mode (CCM) as soon as the input current increases above half the ripple current in the inductor; for lower load currents, the converter switches into discontinuous conduction mode (DCM). If the load is further reduced, the part starts to skip pulses to maintain the output voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61087-Q1 is designed for output voltages up to 18.5 V with a switch peak current limit of 3.2-A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is selectable from 650 kHz to 1.2 MHz, and the input voltage range is from 2.3 V to 6 V. To control the inrush current at start-up a soft-start pin is available. The following section provides a step-by-step design approach for configuring the TPS61087-Q1 as a voltage regulating boost converter.

8.2 Typical Applications

8.2.1 Typical Application Circuit: 5 V to 15 V (f_S = 1.2 MHz)

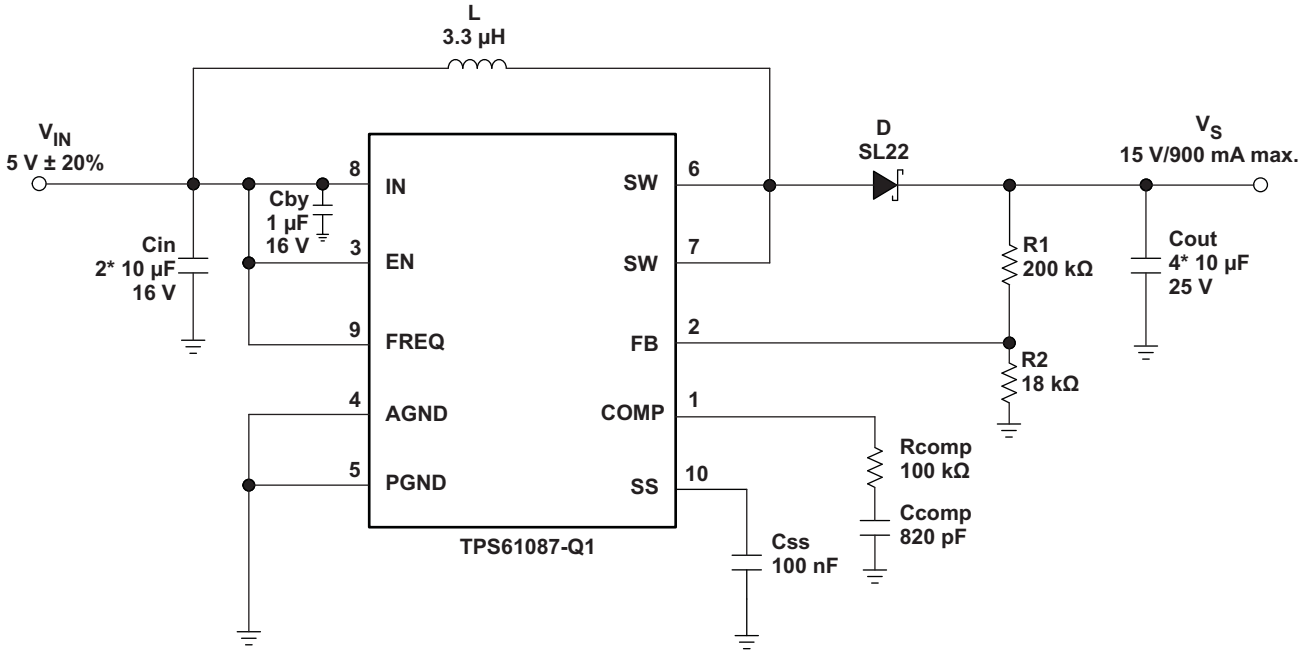


Figure 8. 5 V to 15 V (f_S = 1.2 MHz) Application Diagram

8.2.1.1 Design Requirements

For this design example, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage	5 V ± 20%
Output voltage	15 V
Output current	900 mA
Switching frequency	1.2 MHz

8.2.1.2 Detailed Design Procedure

The first step in the design procedure is to verify that the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency (for example: 90%).

Duty cycle (D) is calculated with Equation 1.

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_S} \tag{1}$$

Maximum output current ($I_{out(max)}$) is calculated with Equation 2.

$$I_{out(\max)} = \left(I_{LIM(\min)} - \frac{\Delta I_L}{2} \right) \cdot (1 - D) \tag{2}$$

Peak switch current in application (I_{swpeak}) is calculated with Equation 3.

$$I_{swpeak} = \frac{\Delta I_L}{2} + \frac{I_{out}}{1 - D} \tag{3}$$

The inductor peak-to-peak ripple current (ΔI_L) is calculated with Equation 4.

$$\Delta I_L = \frac{V_{IN} \cdot D}{f_S \cdot L} \tag{4}$$

where

- V_{IN} is the minimum input voltage.
- V_S is the output voltage.
- $I_{LIM(min)}$ is the converter switch current limit (minimum switch current limit = 3.2 A).
- f_S is the converter switching frequency (typically 1.2 MHz or 650 kHz).
- L is the selected inductor value.
- η is the estimated converter efficiency (use the number from the efficiency plots or 90% as an estimation).

The peak switch current is the steady state peak switch current that the integrated switch, inductor, and external Schottky diode must be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

8.2.1.2.1 Inductor Selection

The TPS61087-Q1 is designed to work with a wide range of inductors. The main parameter for the inductor selection is the saturation current of the inductor which must be higher than the peak switch current as calculated in Equation 3 with additional margin to cover for heavy load transients. A more conservative alternative is to choose an inductor with a saturation current at least as high as the maximum switch current limit of 4.8 A. The other important parameter is the inductor DC resistance. As the DC resistance decreases, the efficiency usually increases. It is important to note that the inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well. At high switching frequencies of 1.2 MHz inductor core losses, proximity effects, and skin effects become more important. An inductor with a larger form factor usually gives higher efficiency. The efficiency difference between different inductors can vary from 2% to 10%. For the TPS61087-Q1, inductor values from 3 µH to 6 µH are a good choice with a switching frequency of 1.2 MHz, typically 3.3 µH. At 650 kHz, TI recommends inductors from 6 µH to 13 µH, typically 6.8 µH. See Table 3 for inductor selection. Customers must verify and validate selected components for suitability with their application.

TI recommends that the inductor current ripple is below 35% of the average inductor current. Equation 5 can be used to calculate the inductor value (L).

$$L = \left(\frac{V_{IN}}{V_S}\right)^2 \cdot \left(\frac{V_S - V_{IN}}{I_{out} \cdot f_S}\right) \cdot \left(\frac{\eta}{0.35}\right) \quad (5)$$

where

- I_{out} is the maximum output current in the application.

Table 3. Inductor Selection

INDUCTOR VALUE	TYPICAL DCR	I_{sat}	SUPPLIER	SIZE (L × W × H mm)	COMPONENT CODE
1.2 MHz					
4.2 µH	23 mΩ	2.2 A	Sumida	5.7 × 5.7 × 3	CDRH5D28
4.7 µH	60 mΩ	2.5 A	Wurth Elektronik	5.9 × 6.2 × 3.3	7447785004
5 µH	24 mΩ	2.9 A	Coilcraft	7.3 × 7.3 × 4.1	MSS7341
5 µH	23 mΩ	2.4 A	Sumida	7 × 7 × 3	CDRH6D28
4.6 µH	38 mΩ	3.15 A	Sumida	7.6 × 7.6 × 3	CDR7D28
4.7 µH	33 mΩ	3.9 A	Wurth Elektronik	7.3 × 7.3 × 3.2	7447789004
3.3 µH	30 mΩ	4.2 A	Wurth Elektronik	7.3 × 7.3 × 3.2	7447789003
650 kHz					
10 µH	51 mΩ	2.2 A	Wurth Elektronik	7.3 × 7.3 × 3.2	744778910
10 µH	36 mΩ	2.7 A	Sumida	8.3 × 8.3 × 3	CDRH8D28
6.8 µH	52 mΩ	2.9 A	Sumida	7 × 7 × 2.8	CDRH6D26HPNP
6.2 µH	25 mΩ	3.3 A	Sumida	8.3 × 8.3 × 6	CDRH8D58
10 µH	80 mΩ	3.5 A	Coilcraft	12.95 × 9.4 × 5.08	DS3316P
10 µH	29 mΩ	4 A	Sumida	8.3 × 8.3 × 4.5	CDRH8D43
6.8 µH	55 mΩ	4.1 A	Wurth Elektronik	12.7 × 10 × 4.9	74454068

8.2.1.2.2 Rectifier Diode Selection

To achieve high efficiency a Schottky type must be used for the rectifier diode. The reverse voltage rating must be higher than the maximum output voltage of the converter. The averaged rectified forward current (I_{avg}), the Schottky diode must be rated for, is equal to the output current (I_{out}).

$$I_{avg} = I_{out} \quad (6)$$

Usually a Schottky diode with 2-A maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current but must be able to dissipate the power. The dissipated power (P_D) is the average rectified forward current times the diode forward voltage ($V_{forward}$).

$$P_D = I_{avg} \cdot V_{forward} \quad (7)$$

Typically the diode must be able to dissipate around 500 mW depending on the load current and forward voltage. See Table 4 for diode selection. Customers must verify and validate selected components for suitability with their application.

Table 4. Rectifier Diode Selection

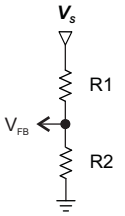
I_{avg}	V_R	$V_{forward}$	SUPPLIER	COMPONENT CODE
2 A	20 V	0.44 V	Vishay Semiconductor	SL22
2 A	20 V	0.5 V	Fairchild Semiconductor	SS22

8.2.1.2.3 Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 50 µA flowing through the feedback divider gives good accuracy and noise covering. A standard low side resistor of 18 kΩ is typically selected. The resistors are then calculated as shown in Equation 8:

$$R2 = \frac{V_{FB}}{70\mu A} \approx 18k\Omega \qquad R1 = R2 \cdot \left(\frac{V_S}{V_{FB}} - 1 \right)$$

$$V_{FB} = 1.238V$$



(8)

8.2.1.2.4 Compensation (COMP)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier.

Equation 9 can be used to calculate R_{COMP} and C_{COMP}.

$$R_{COMP} = \frac{110 \cdot V_{IN} \cdot V_S \cdot C_{out}}{L \cdot I_{out}} \qquad C_{COMP} = \frac{V_S \cdot C_{out}}{7.5 \cdot I_{out} \cdot R_{COMP}}$$

where

- C_{out} is the output capacitance. (9)

Make sure that R_{COMP} < 120 kΩ and C_{COMP} > 820 pF, independent of the results of the above formulas.

See Table 5 for dedicated compensation networks giving an improved load transient response. These conservative R_{COMP} and C_{COMP} values for certain inductors, input, and output voltages provide a very stable system. For a faster response time, a higher R_{COMP} value can be used to enlarge the bandwidth, as well as a slightly lower value of C_{COMP} to keep enough phase margin. These adjustments must be performed in parallel with the load transient response monitoring of TPS61087-Q1.

Standard values of R_{COMP} = 16 kΩ and C_{COMP} = 2.7 nF works for the majority of the applications.

Table 5. Recommended Compensation Network Values at High and Low Frequency

FREQUENCY	L	V_S	V_{IN} ± 20%	R_{COMP}	C_{COMP}
High (1.2 MHz)	3.3 µH	15 V	5 V	100 kΩ	820 pF
			3.3 V	91 kΩ	1.2 nF
		12 V	5 V	68 kΩ	820 pF
			3.3 V	68 kΩ	1.2 nF
		9 V	5 V	39 kΩ	820 pF
			3.3 V	39 kΩ	1.2 nF
Low (650 kHz)	6.8 µH	15 V	5 V	51 kΩ	1.5 nF
			3.3 V	47 kΩ	2.7 nF
		12 V	5 V	33 kΩ	1.5 nF
			3.3 V	33 kΩ	2.7 nF
		9 V	5 V	18 kΩ	1.5 nF
			3.3 V	18 kΩ	2.7 nF

8.2.1.2.5 Input Capacitor Selection

TI recommends low ESR ceramic capacitors for good input voltage filtering. TPS61087-Q1 has an analog input (IN). Therefore, TI recommends placing a 1-µF bypass capacitor as close as possible to the IC from IN to GND.

Two 10-µF (or one 22-µF) ceramic input capacitors are sufficient for most of the applications. For better input voltage filtering this value can be increased. See Table 6 for output capacitor selection. Customers must verify and validate selected components for suitability with their application.

8.2.1.2.6 Output Capacitor Selection

TI recommends low ESR ceramic capacitors for best output voltage filtering. Four 10-µF (or two 22-µF) ceramic output capacitors work for most of the applications. Higher capacitor values can be used to improve the load transient response. See Table 6 for output capacitor selection. DC voltage derating factor must also be considered while choosing capacitors. Customers must verify and validate selected components for suitability with their application.

Table 6. Rectifier Input and Output Capacitor Selection

	CAPACITOR (SIZE)	VOLTAGE RATING	SUPPLIER	COMPONENT CODE
C_{IN}	22 µF (1206)	16 V	Taiyo Yuden	EMK316 BJ 226ML
IN bypass	1 µF (0603)	16 V	Taiyo Yuden	EMK107 BJ 105KA
C_{OUT}	10 µF (1206)	25 V	Taiyo Yuden	TMK316 BJ 106KL

To calculate the output voltage ripple, use Equation 10.

$$\Delta V_C = \frac{V_S - V_{IN}}{V_S \cdot f_S} \cdot \frac{I_{out}}{C_{out}} \qquad \Delta V_{C\_ESR} = I_{L(peak)} \cdot R_{C\_ESR}$$

where

- ΔV_C is the output voltage ripple dependent on output capacitance, output current, and switching frequency.
- ΔV_{C_ESR} is the output voltage ripple due to output capacitors ESR (equivalent series resistance).
- I_{swpeak} is the inductor peak switch current in the application.
- R_{C_ESR} is the output capacitors equivalent series resistance (ESR). (10)

ΔV_{C_ESR} can be neglected in many cases because ceramic capacitors provide low ESR.

8.2.1.3 Application Curves

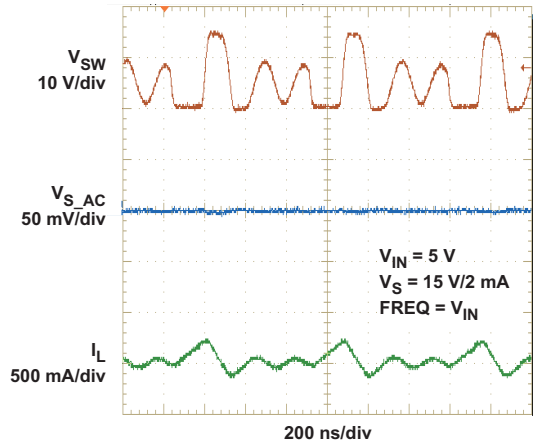


Figure 9. PWM Switching Discontinuous Conduction Mode

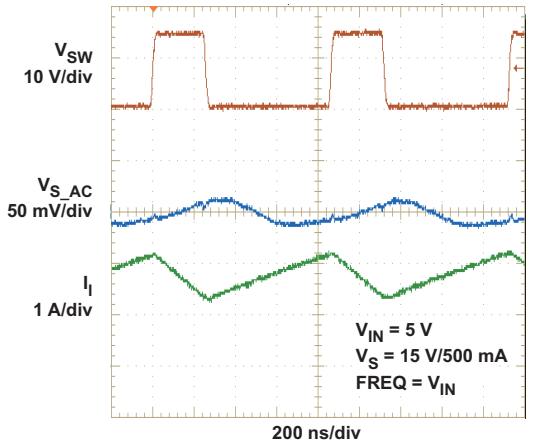


Figure 10. PWM Switching Continuous Conduction Mode

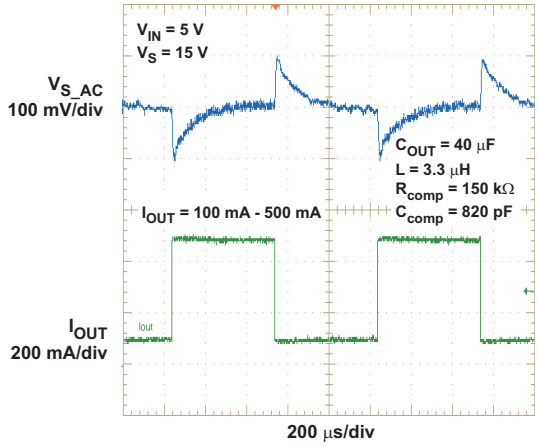


Figure 11. Load Transient Response High Frequency (1.2 MHz)

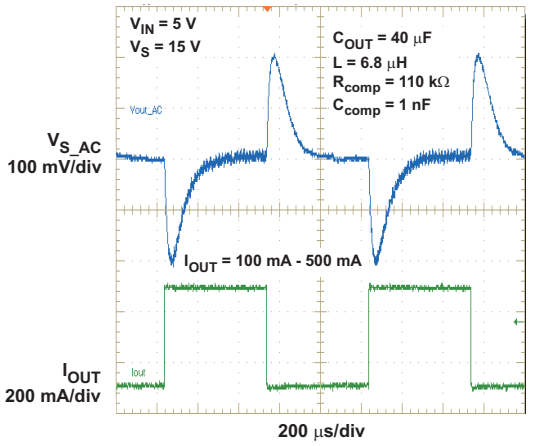


Figure 12. Load Transient Response Low Frequency (650 kHz)

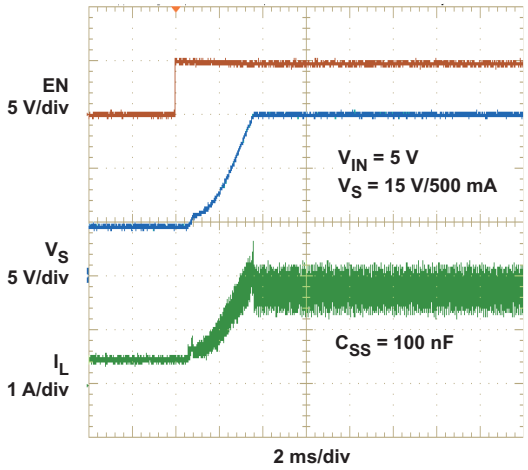
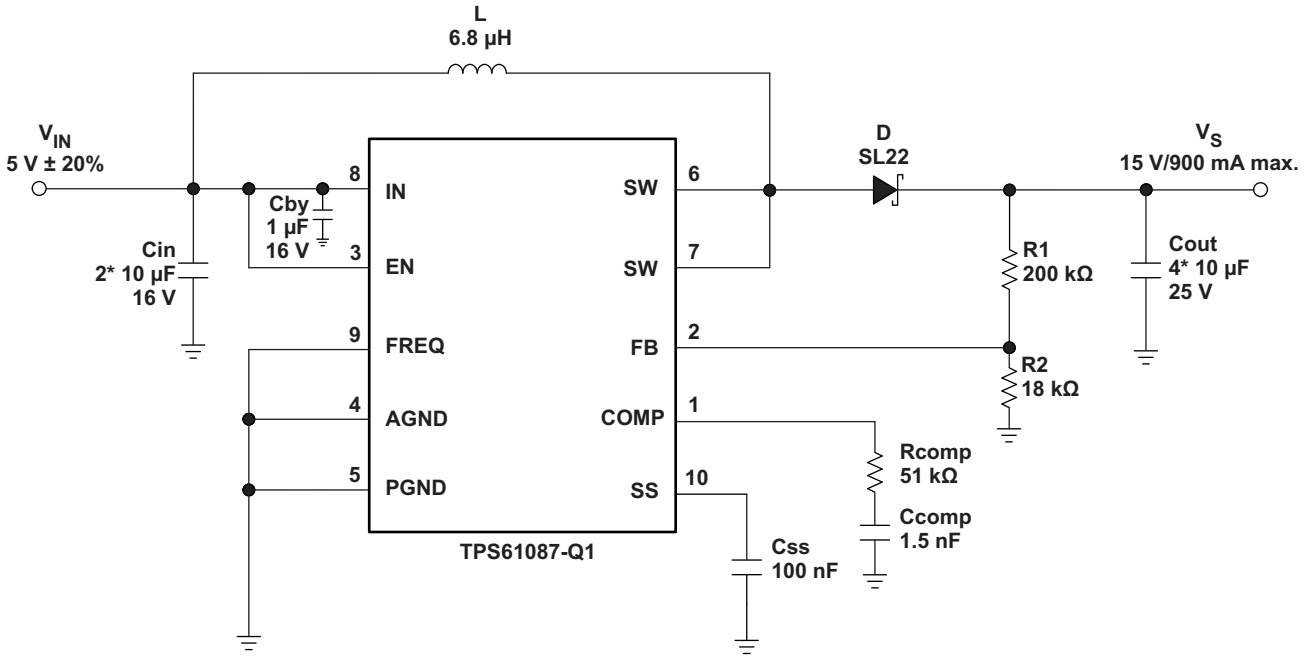


Figure 13. Soft Start

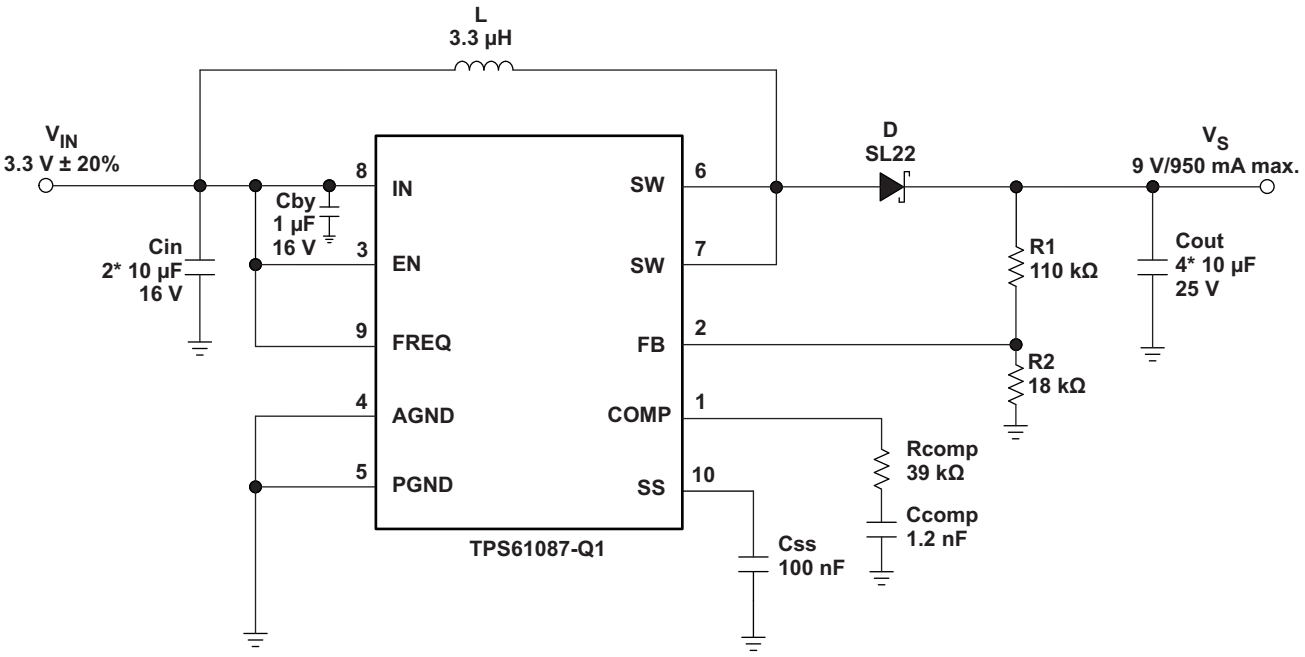
8.2.2 Other Application Circuit Examples

Figure 14 to Figure 22 show application circuit examples using the TPS61087-Q1 device. These circuits must be fully validated and tested by customers before using these circuits in their designs. TI does not warrant the accuracy or completeness of these circuits, nor does TI accept any responsibility for them.



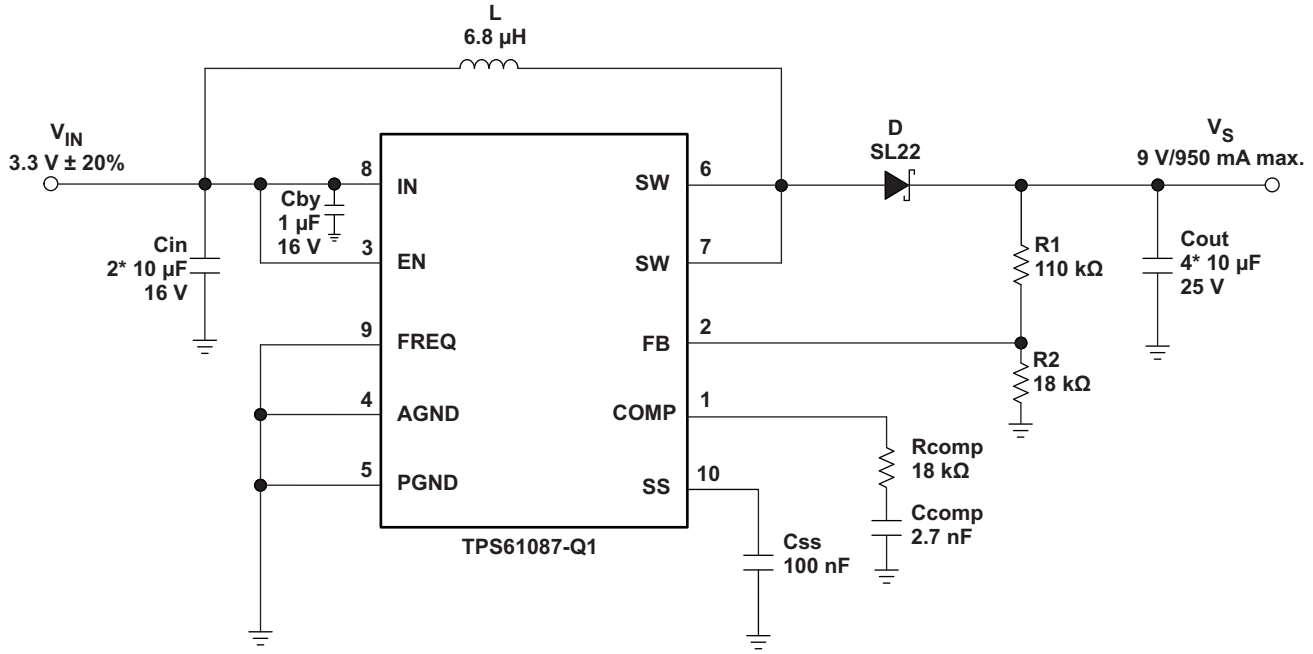
f_S = 650 kHz V_S = 15 V $I_{OUT(max)}$ = 900 mA

Figure 14. 5-V to 15-V Application Diagram



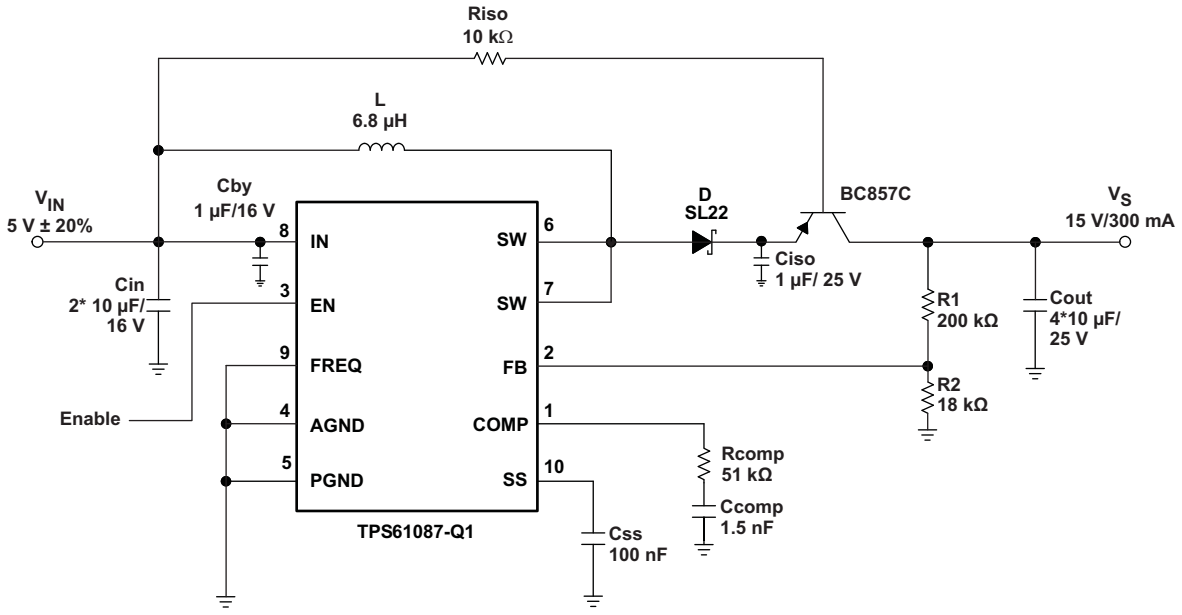
f_S = 1.2 MHz V_S = 9 V $I_{OUT(max)}$ = 950 mA

Figure 15. 3.3-V to 9-V Application Diagram



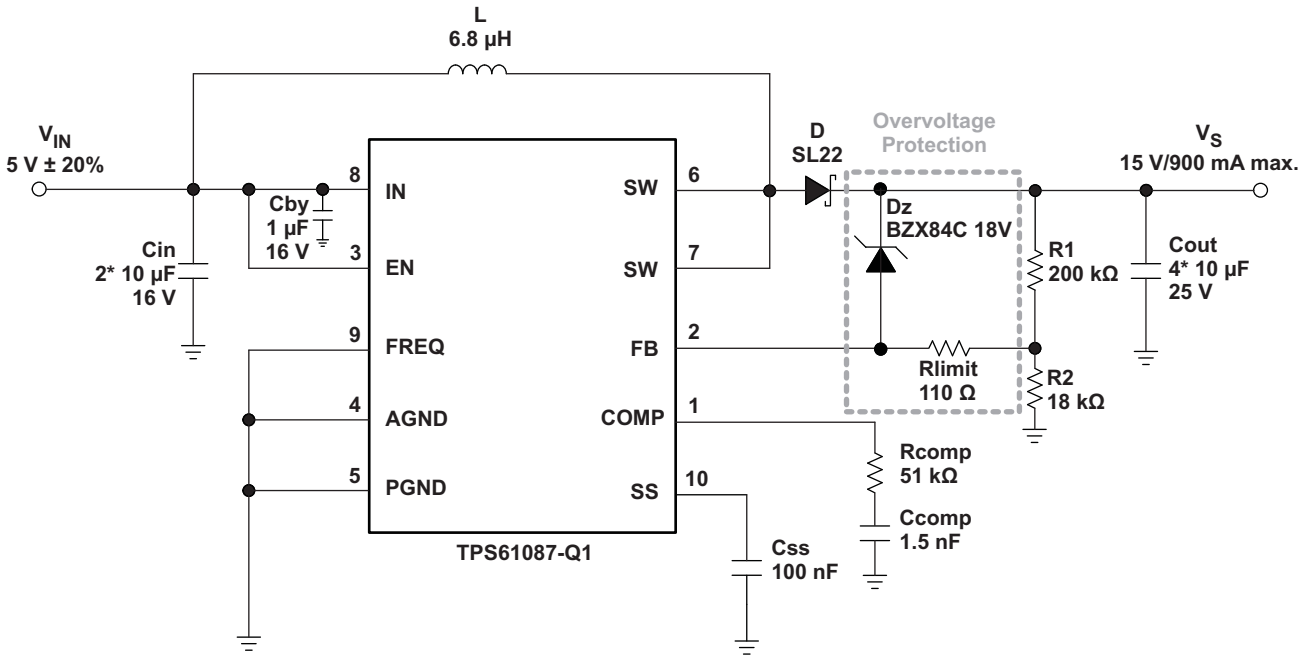
f_S = 650 kHz V_S = 9 V $I_{OUT(max)}$ = 950 mA

Figure 16. 3.3-V to 9-V Application Diagram



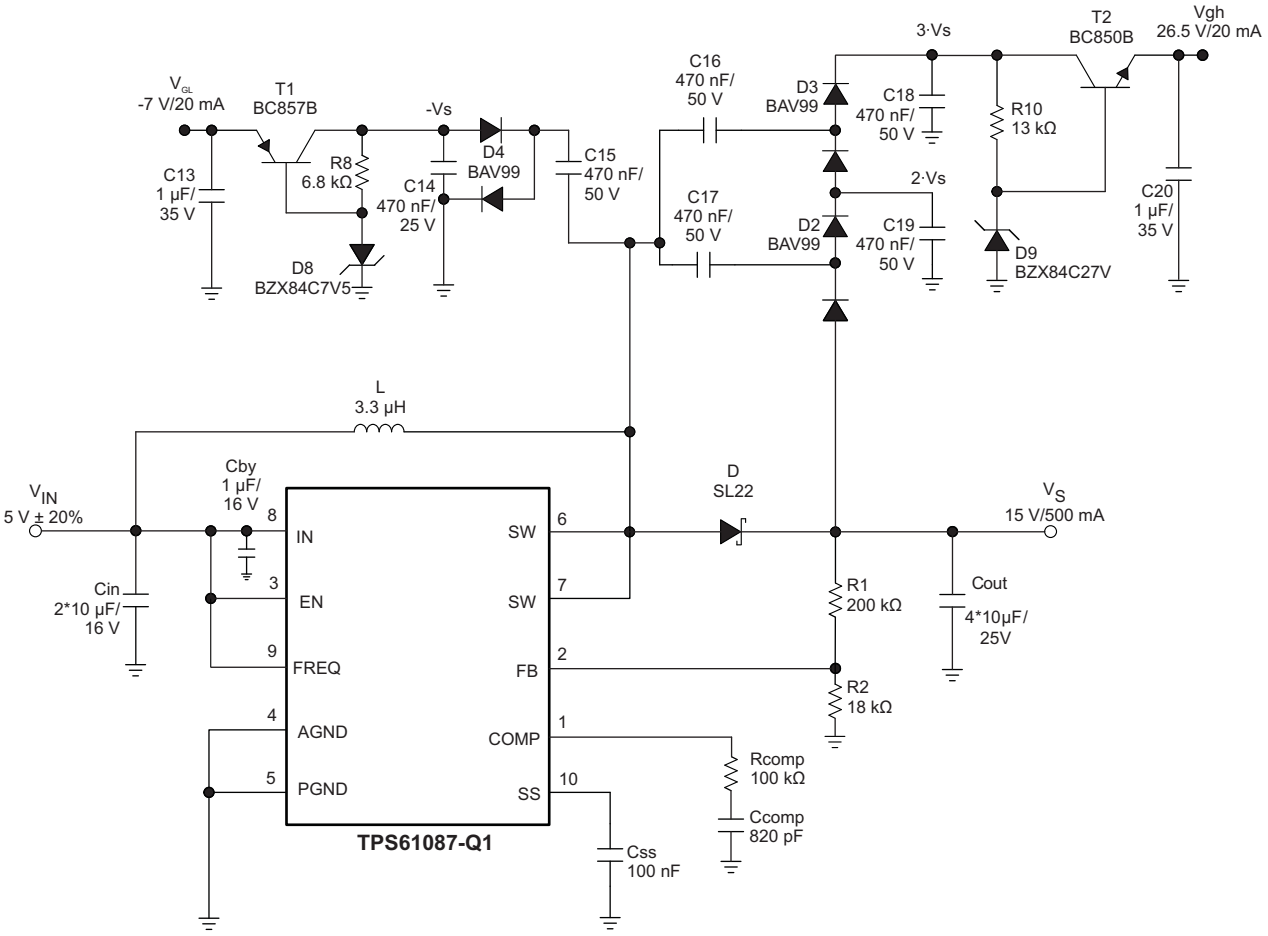
f_S = 650 kHz V_S = 15 V I_{OUT} = 300 mA

Figure 17. Diagram for Application With External Load Disconnect Switch



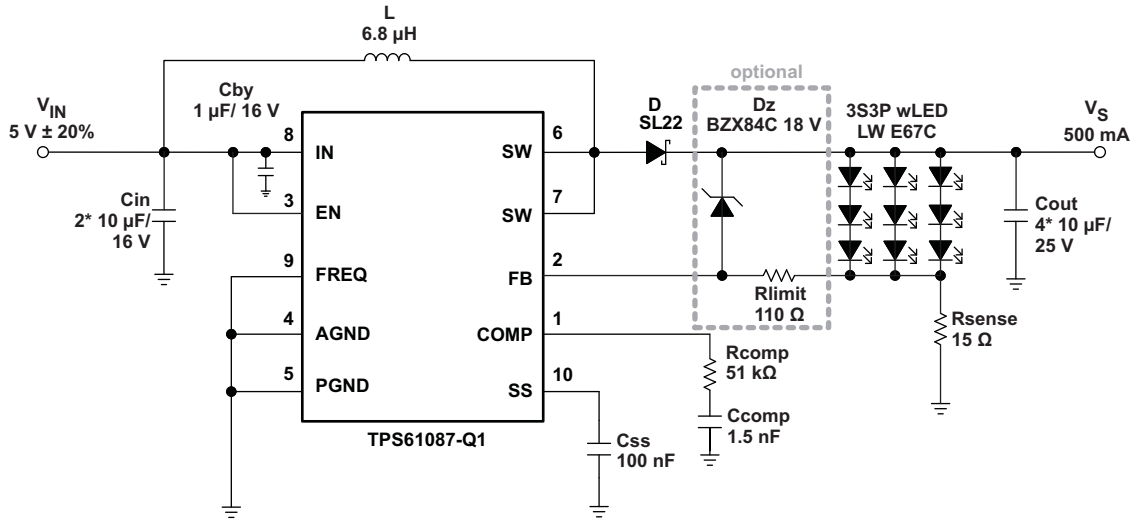
f_S = 650 kHz V_S = 15 V $I_{OUT(max)}$ = 900 mA

Figure 18. Application Diagram for 5 V to 15 V With Overvoltage Protection



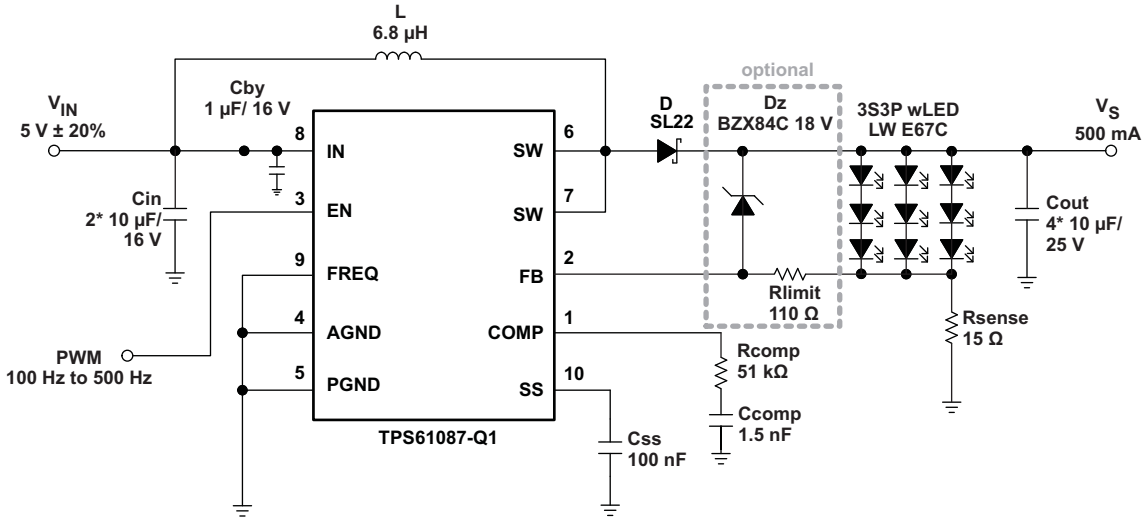
f_S = 1.2 MHz V_S = 15 V I_{OUT} = 500 mA

Figure 19. Application Diagram for 5 V to 15 V for TFT LCD With External Charge Pumps (VGH, VGL)



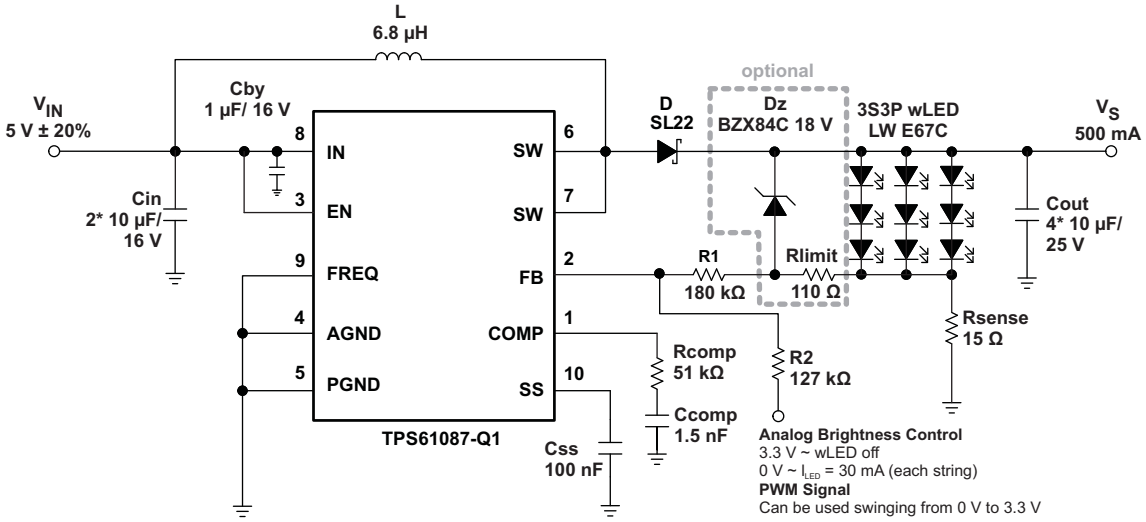
f_S = 650 kHz I_{OUT} = 500 mA

Figure 20. Application Diagram for wLED Supply (3S3P) With Optional Clamping Zener Diode



f_S = 650 kHz I_{OUT} = 500 mA

Figure 21. Application Diagram for wLED Supply (3S3P) With Adjustable Brightness Control Using A PWM Signal On The Enable Pin With Optional Clamping Zener Diode



f_S = 650 kHz I_{OUT} = 500 mA

Figure 22. Application Diagram for wLED Supply (3S3P) With Adjustable Brightness Control Using An Analog Signal On The Feedback Pin With Optional Clamping Zener Diode

9 Power Supply Recommendations

The TPS61087-Q1 is designed to operate from an input voltage supply range from 2.3 V to 6 V. The power supply to the TPS61087-Q1 must have a current rating according to the supply voltage, output voltage, and output current of the TPS61087-Q1.

10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems.

Figure 23 provides an example of layout design with the TPS61087-Q1 device.

- Use wide and short traces for the main current path and for the power ground tracks.
- The input capacitor, output capacitor, and the inductor must be placed as close as possible to the IC.
- Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at the GND terminal of the IC.
- The most critical current path for all boost converters is from the switching FET, through the rectifier diode, then the output capacitors, and back to ground of the switching FET. Therefore, the output capacitors and their traces must be placed on the same board layer as the IC and as close as possible between the SW pin and the GND terminal of the IC.

10.2 Layout Example

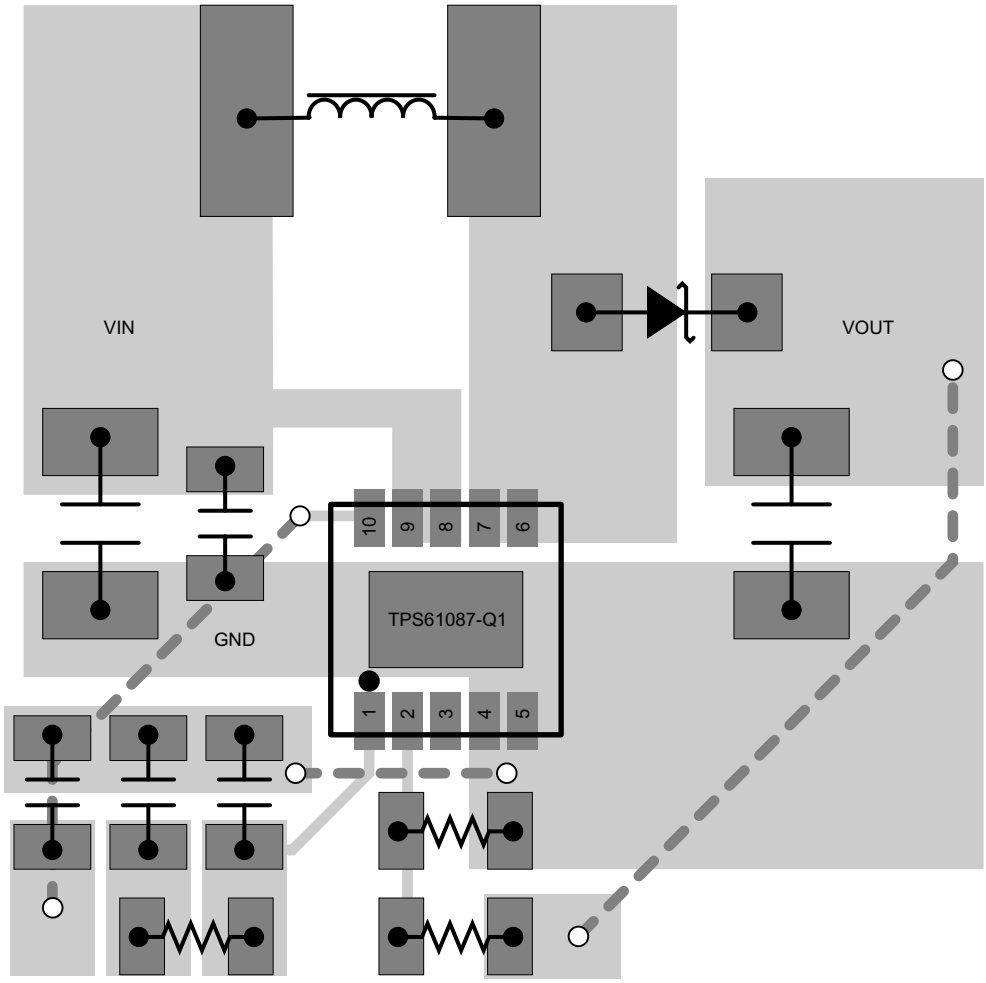


Figure 23. TPS61087-Q1 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Performing Accurate PFM Mode Efficiency Measurements*
- *QFN/SON PCB Attachment*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61087QDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	PMOQ	Samples
TPS61087QWDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	11ZC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS61087-Q1 :

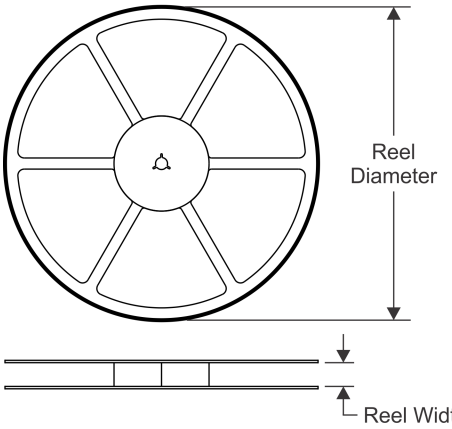
- Catalog: TPS61087

NOTE: Qualified Version Definitions:

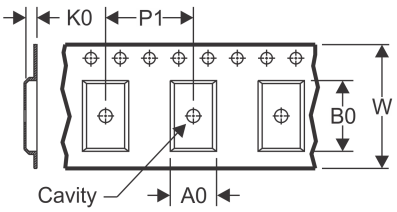
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

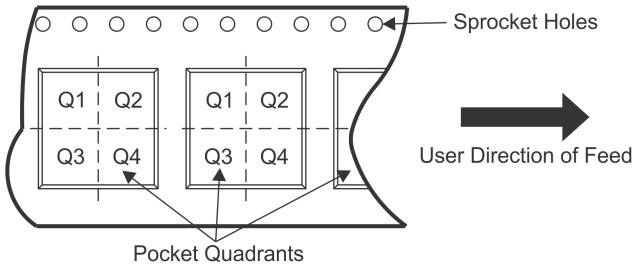


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

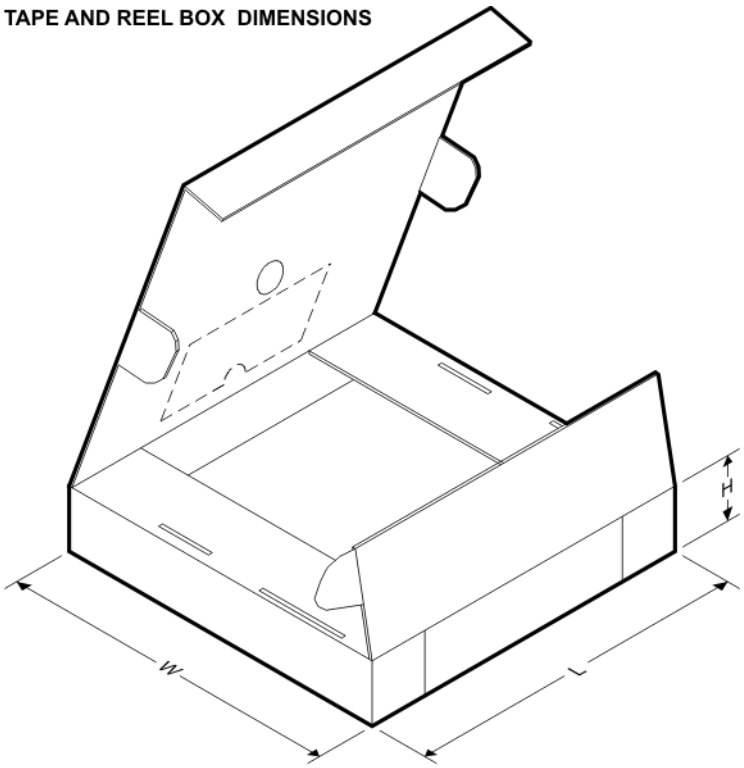
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61087QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



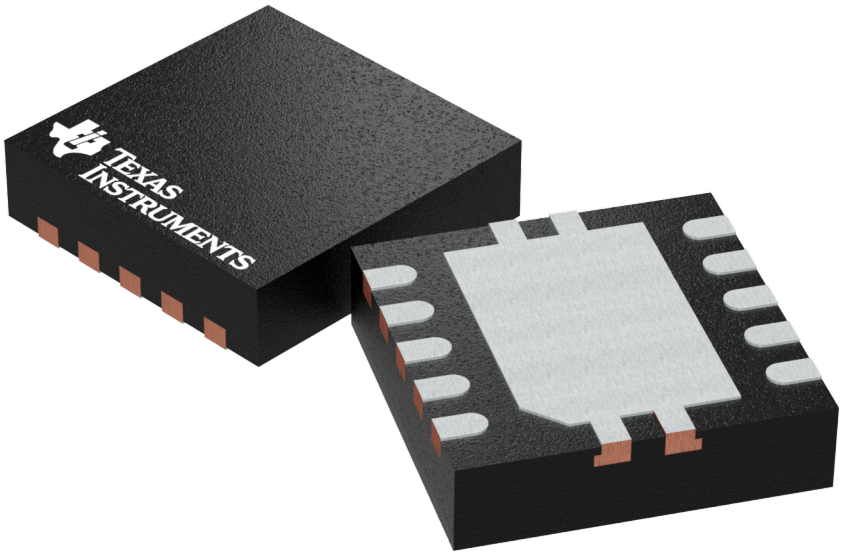
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61087QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0

DRC 10

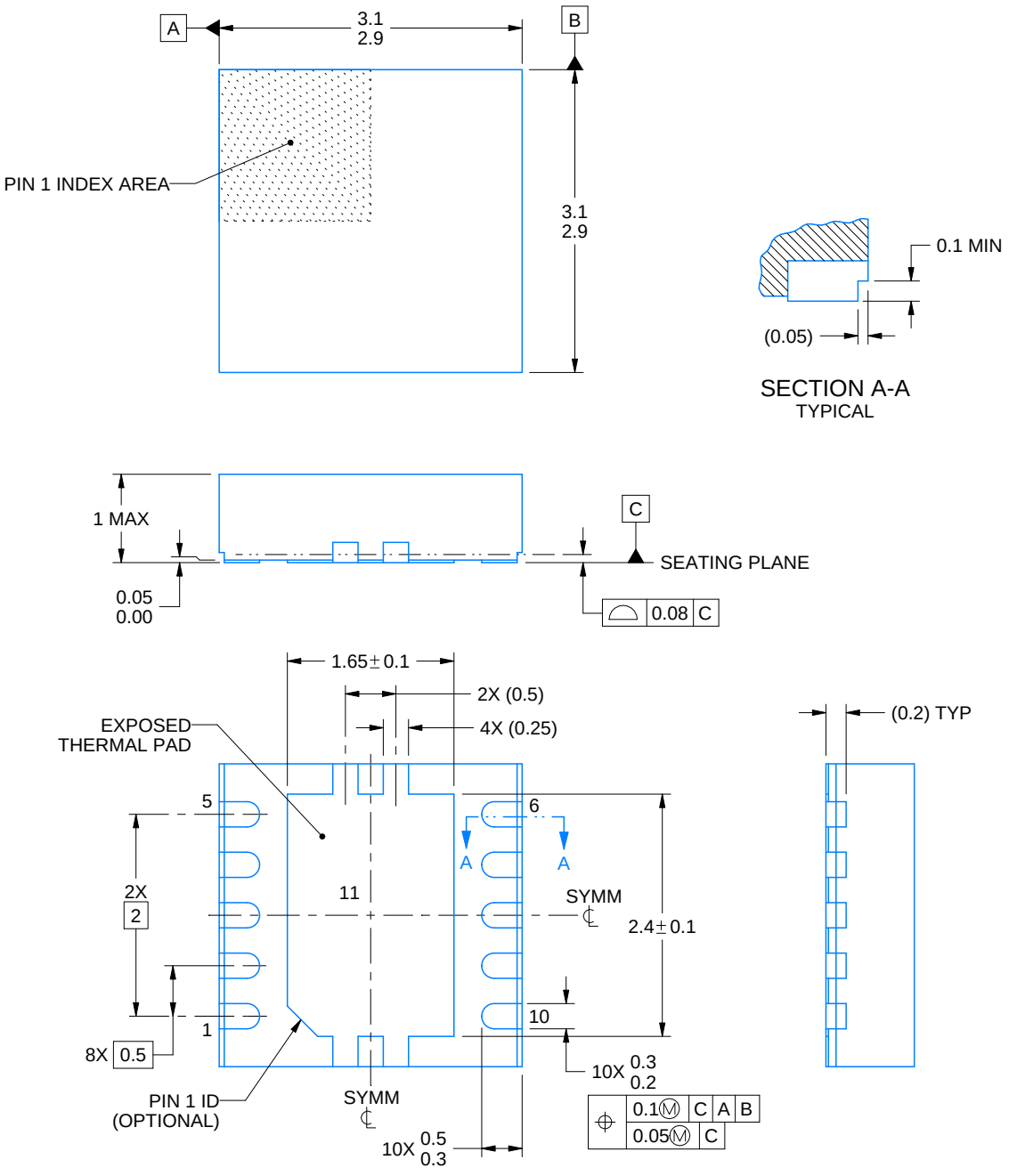
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



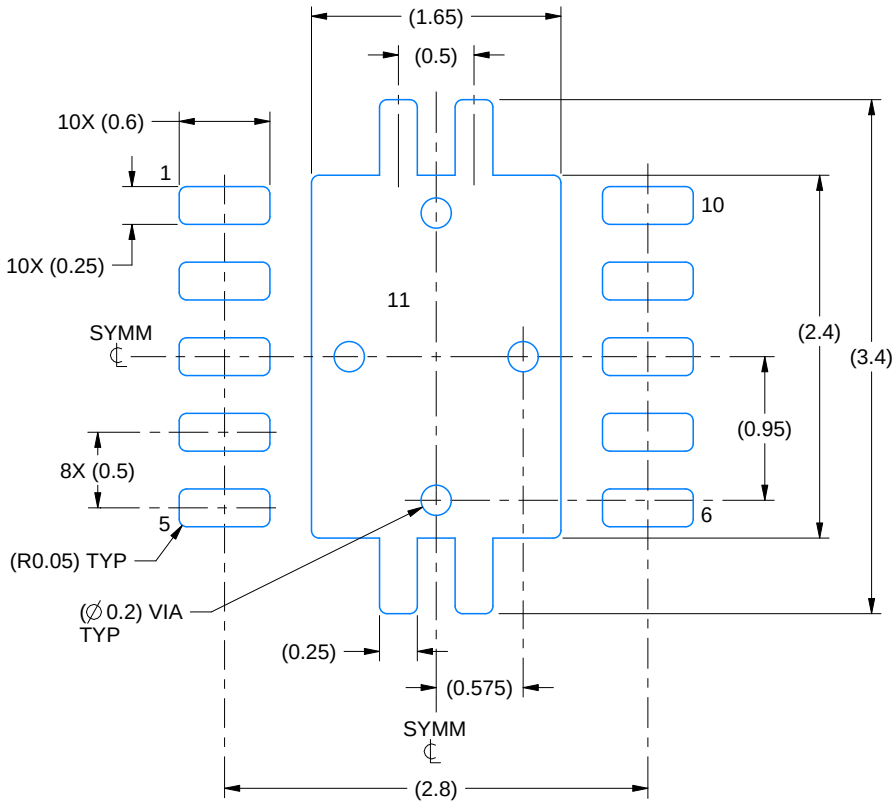
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

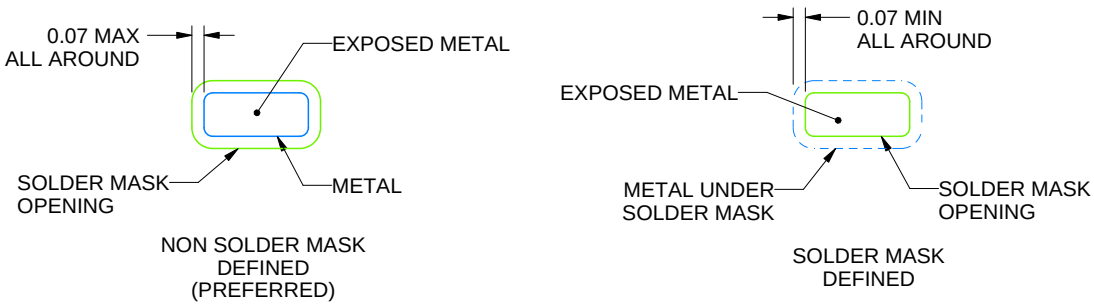


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

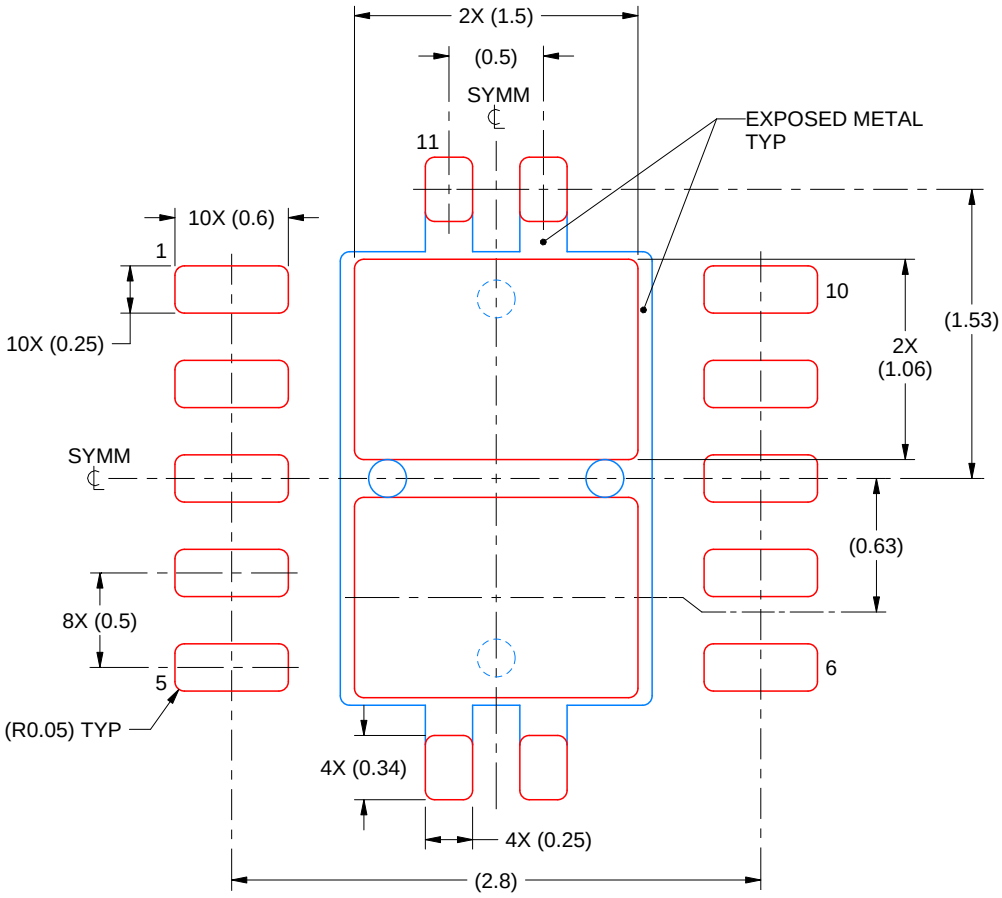


SOLDER MASK DETAILS

4223412/A 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4223412/A 01/2017

NOTES: (continued)

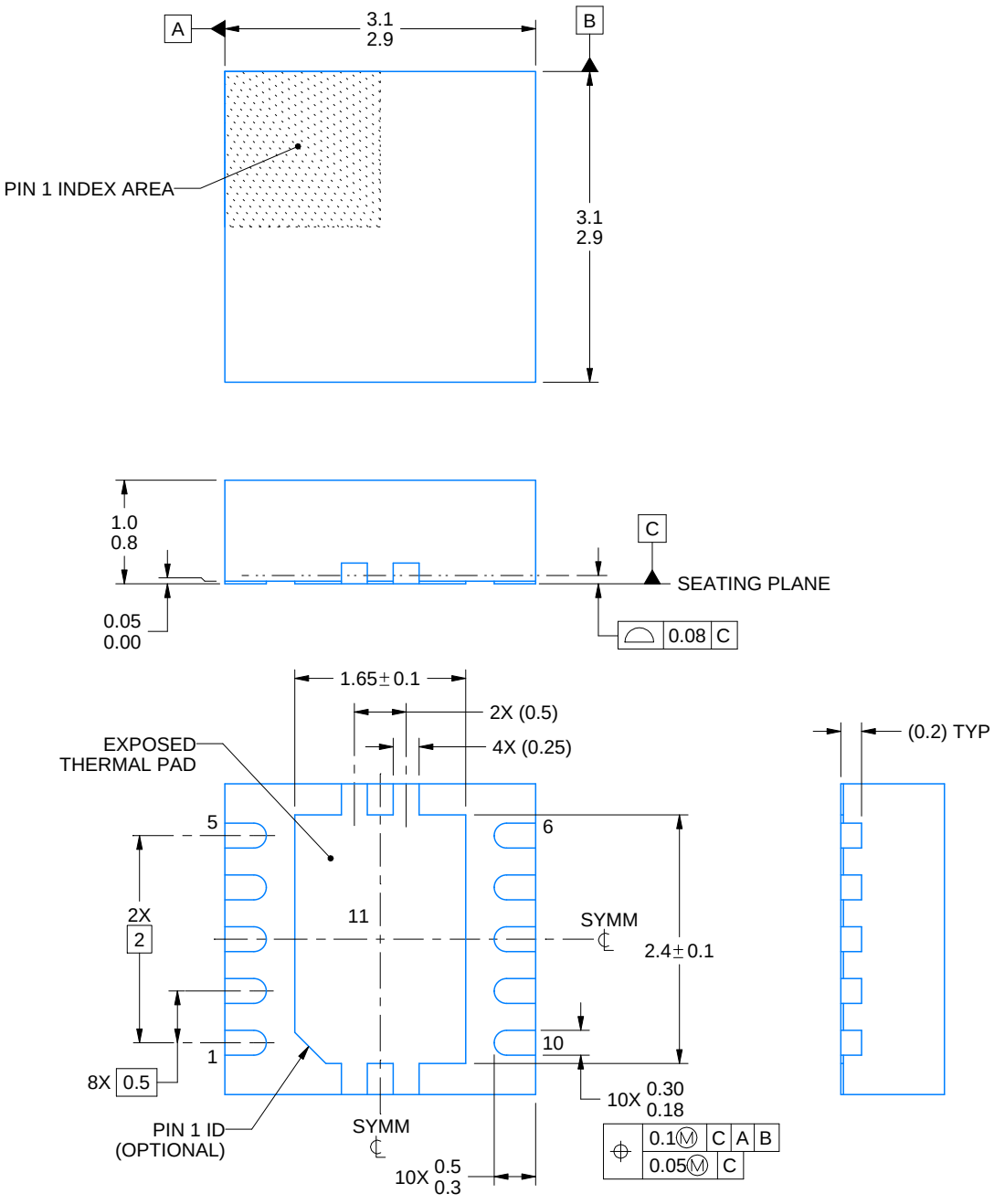
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRC0010J

PACKAGE OUTLINE

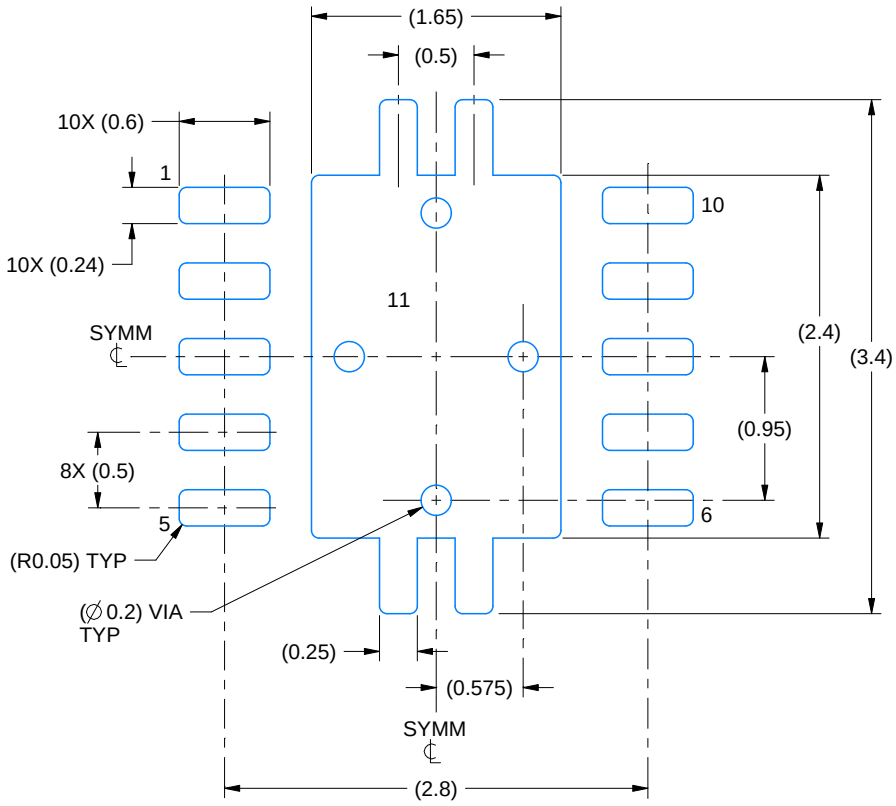
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

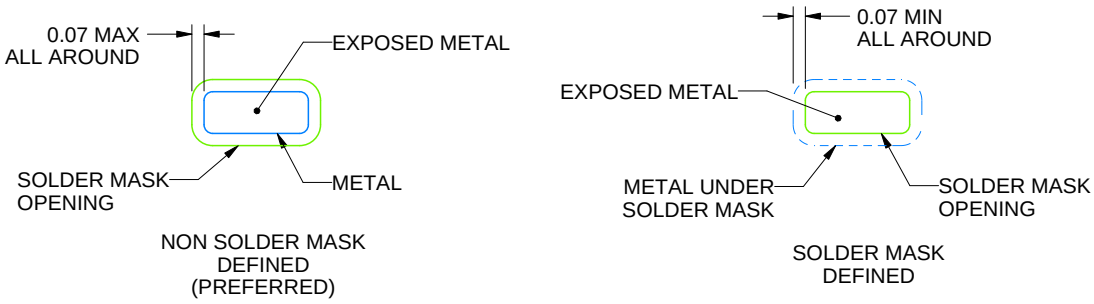


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

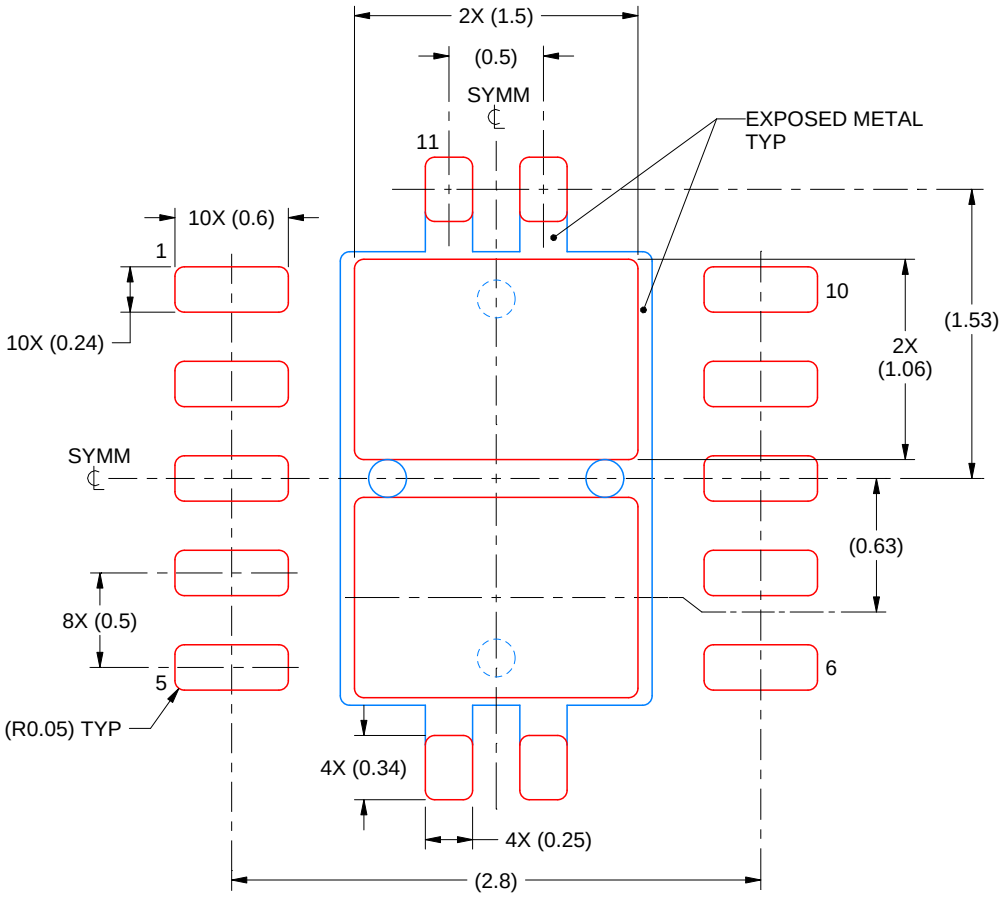
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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