Ultra Low Capacitance ESD Protection –ESD1065P

Description

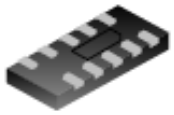
The ESD1065P have a typical capacitance of only 0.25pF between I/O pins. This allows it to be used on circuits operating in excess of 4GHz without signal attenuation. They have been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients). They used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Features

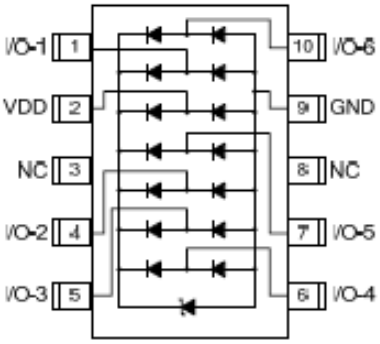
- Case :DFN-10-4.1*2.0*0.5-0.8
- Package design optimized for high speed lines
- Low clamping voltage
- Low capacitance :0.25 pF typical (I/O to I/O)
- Protection six I/O Lines and one VDD line
- Compatible with IEC 61000-4-2(ESD) :Air 15KV , Contact 8KV
- For 5V and below 5V operating voltage
- ROHS

Applications

- USB3.0
- HDMI 1.4
- Digital Visual Interface (DVI)
- VGA
- 10/100/1000Ethernet interface
- High speed I/O Ports in any electronic product.

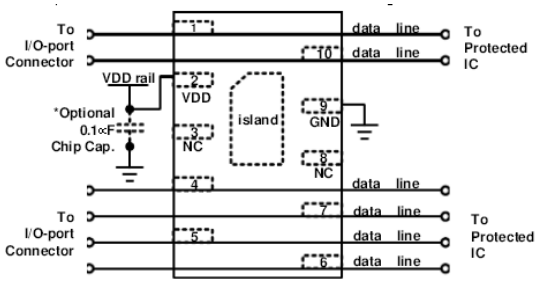


DFN-10-4.1x2x0.5-0.80



DFN-10-4.1x2x0.5-0.80
(Top view)

Schematic & Pin configuration



Data line and power rails connection of ESD1065P

Absolute Maximum Ratings

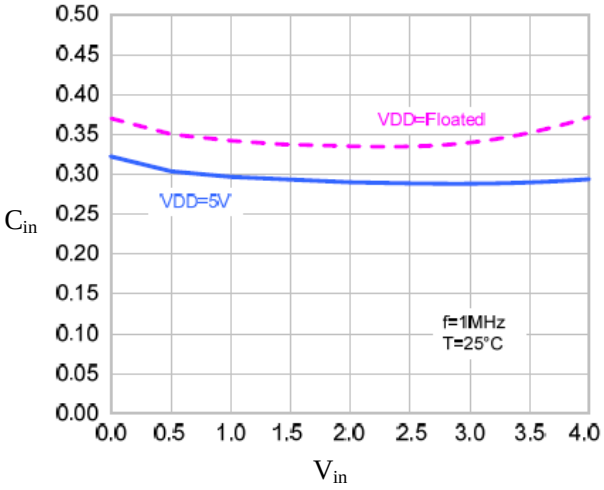
Parameter	Symbol	Value	Units
Peak Current (tp =8/20μs)	P_{PK}	150	W
Peak Current (tp =8/20μs)	I_{PP}	5	A
IEC61000-4-2 (Contact)	V_{ESD}	±8	kV
IEC61000-4-2 (Air)	V_{ESD}	±15	kV
Lead Soldering Temperature	T_L	260 (10 sec)	° C
Operating Temperature	T_J	-55 to +125	° C
Storage Temperature Range	T_{STG}	-55 to +150	° C

Electrical Characteristics (T =25° C)

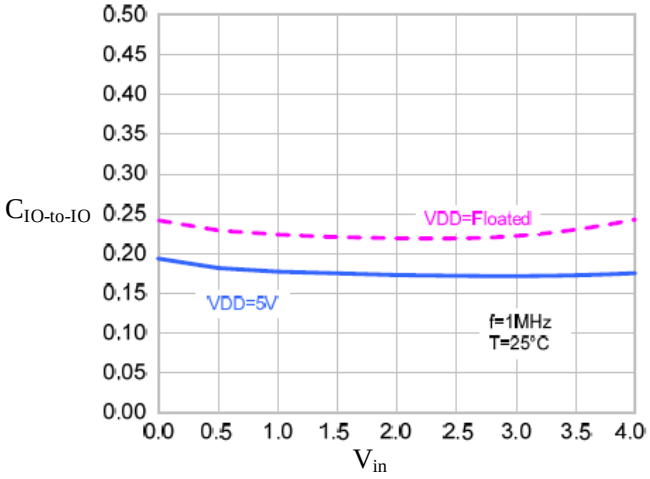
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-off Voltage	V_{RWM}	Any I/O pin to ground			5	V
Reverse Breakdown Voltage	V_{BR}	It = 1mA Any I/O pin to ground	6			V
Reverse Leakage Current	I_R	V_{RWM} =5.0V, T=25℃ Any I/O pin to ground			1	μA
Clamping Voltage	V_C	I_{PP} = 1A, t_P = 8/20μs Any I/O pin to ground		8.5	12.0	
Junction Capacitance	C_{J1}	V_R=0V, f = 1MHz Between I/0 pins		0.2	0.25	pF
	C_{J2}	V_R=0V, f = 1MHz Any I/O pin to ground			0.4	pF

Rating & Characteristic Curves

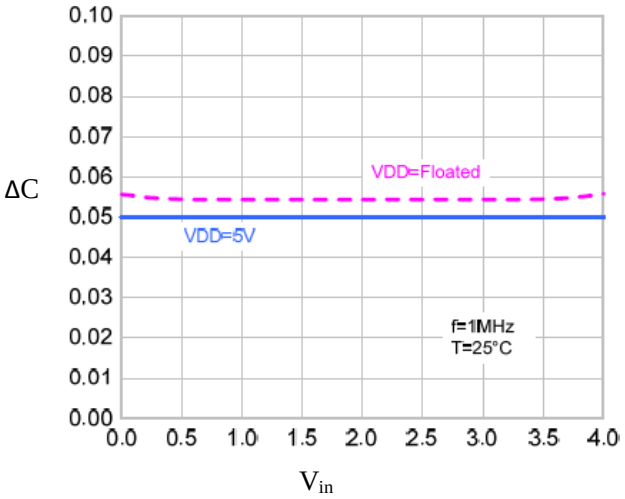
Typical variation of C_{in} VS. V_{in}



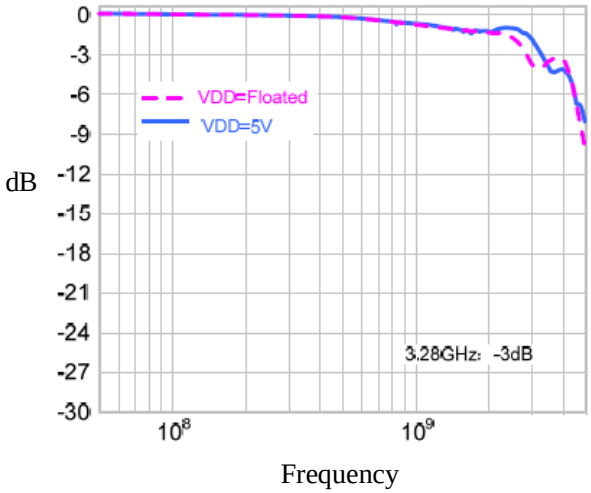
Typical variation of $C_{IO\text{-}to\text{-}IO}$ VS. V_{in}



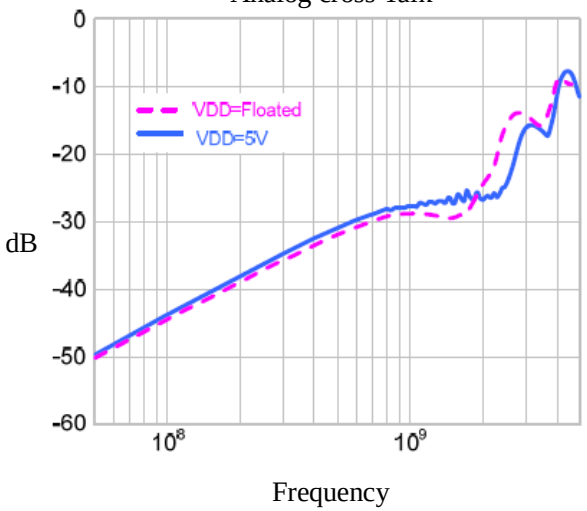
Typical variation of $\Delta C_{IO\text{-}to\text{-}IO}$ VS. V_{in}



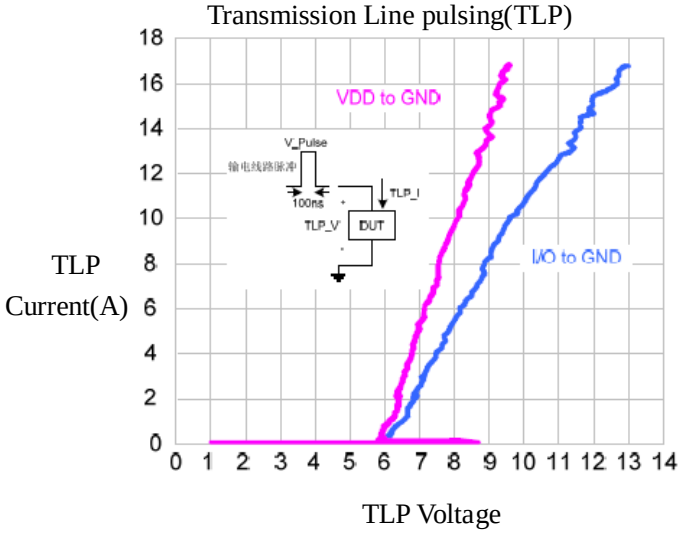
Insertion Loss S21(I/O-to-GND)



Analog cross Talk



Transmission Line pulsing(TLP)



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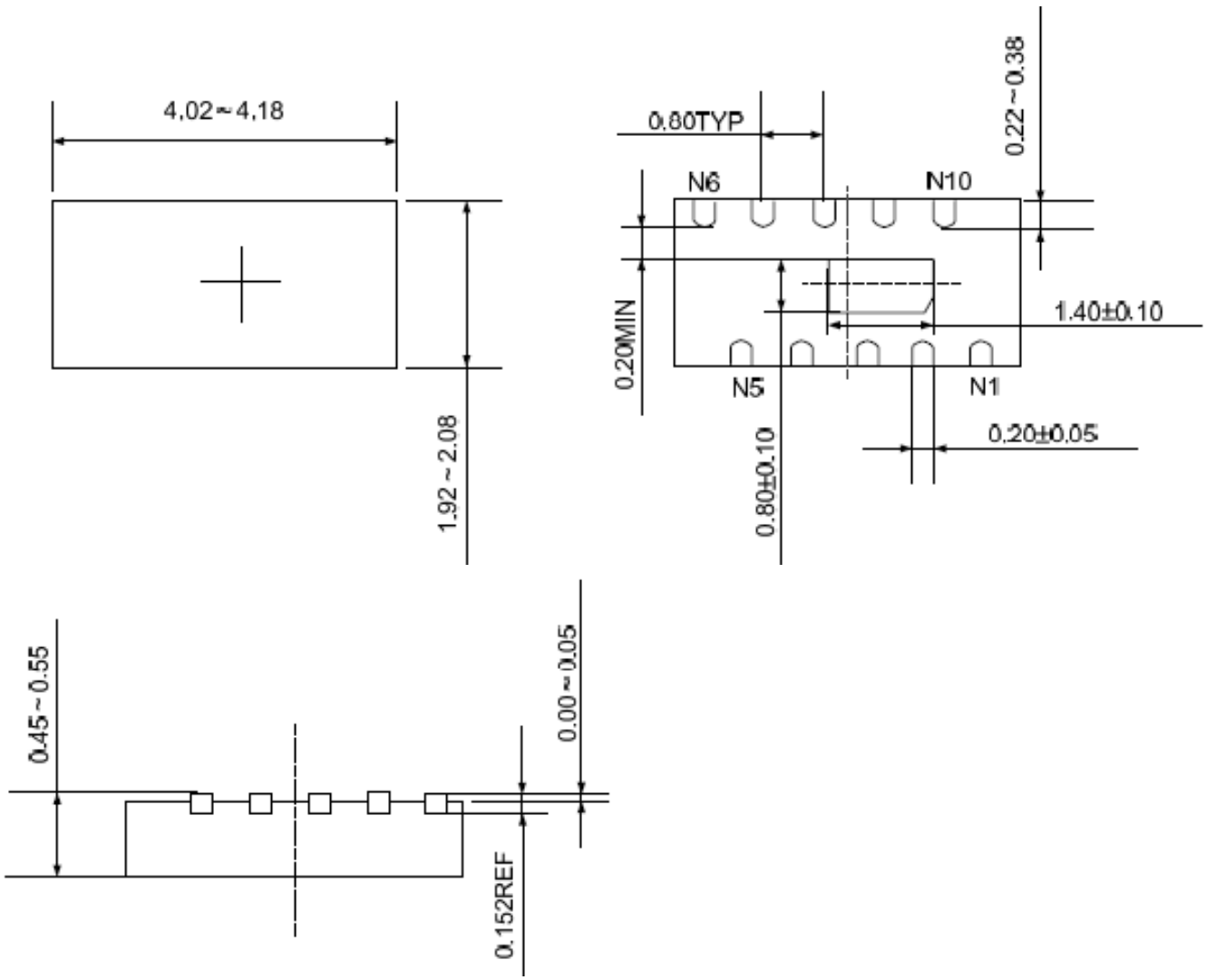

Disclaimer

Specifications are subject to change without notice.

The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time.

Users should verify actual device performance in their specific applications.