ALPHA & OMEGA SEMICONDUCTOR

AON6932A

30V Dual Asymmetric N-Channel AlphaMOS

General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Very Low RDS(on) at 4.5V_{GS}
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Application

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

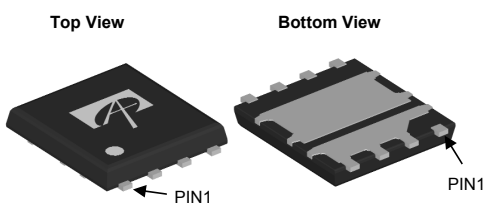
Product Summary

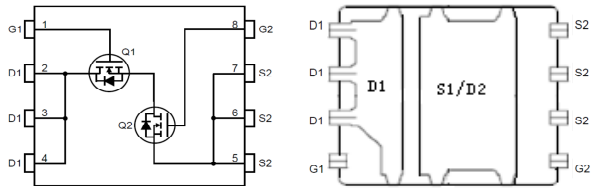
	Q1	Q2
V_{DS}	30V	30V
I_D (at V_{GS}=10V)	28A	42A
$R_{DS(ON)}$ (at V_{GS}=10V)	<5mΩ	<2.5mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	<8.5mΩ	<3.2mΩ

100% UIS Tested
100% Rg Tested

Green Product

DFN5X6B





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current[G]	T_C=25°C	I_D	28	42	A
	T_C=100°C		22	33	
Pulsed Drain Current [C]		I_{DM}	112	168	
Continuous Drain Current	T_A=25°C	I_{DSM}	22	36	A
	T_A=70°C		17	29	
Avalanche Current [C]		I_{AS}	32	70	A
Avalanche Energy L=0.05mH [C]		E_{AS}	26	123	mJ
V_{DS} Spike	100ns	V_{SPIKE}	36	36	V
Power Dissipation [B]	T_C=25°C	P_D	31	78	W
	T_C=100°C		12	31	
Power Dissipation [A]	T_A=25°C	P_{DSM}	3.6	4.3	W
	T_A=70°C		2.3	2.7	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	29	24	35	29	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		56	50	67	60	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	3.3	1.2	4	1.6	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.4	1.8	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		4.1	5	mΩ
		T_J=125°C		5.6	6.8	
		V_{GS}=4.5V, I_D=20A		6.7	8.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		91		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current[G]				28	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1037		pF
C_{oss}	Output Capacitance			441		pF
C_{rss}	Reverse Transfer Capacitance			61		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.7	1.5	2.3	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A		15.5	22	nC
Q_g(4.5V)	Total Gate Charge			6.8	10	nC
Q_{gs}	Gate Source Charge			3.0		nC
Q_{gd}	Gate Drain Charge			3.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		5.5		ns
t_r	Turn-On Rise Time			3.3		ns
$t_{D(off)}$	Turn-Off DelayTime			18		ns
t_f	Turn-Off Fall Time			4.3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs		12.7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs		17.2		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with TA=25° C.

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

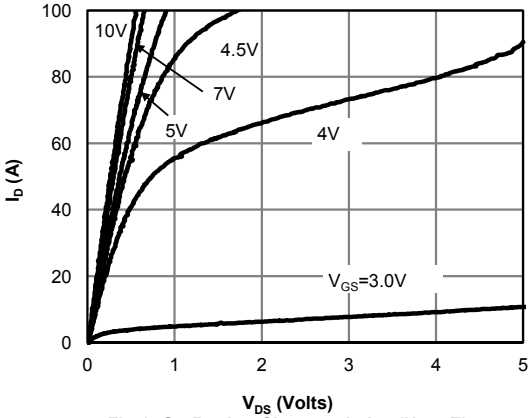


Fig 1: On-Region Characteristics (Note E)

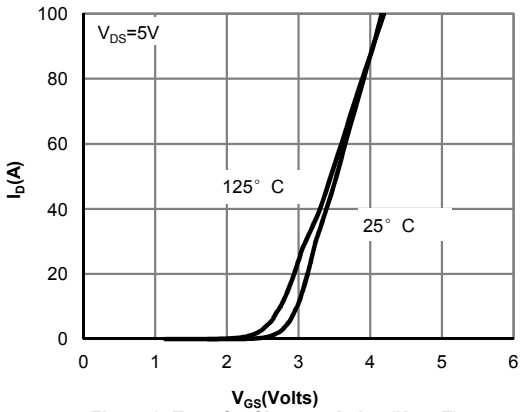


Figure 2: Transfer Characteristics (Note E)

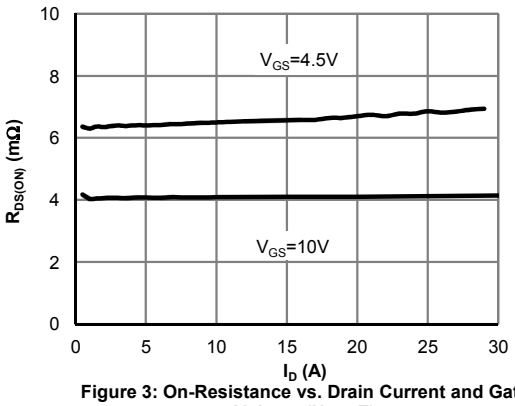


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

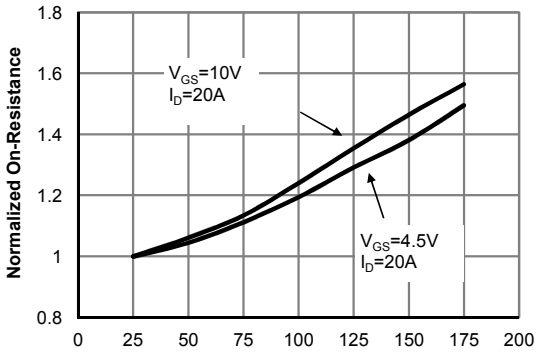


Figure 4: On-Resistance vs. Junction Temperature (Note E)

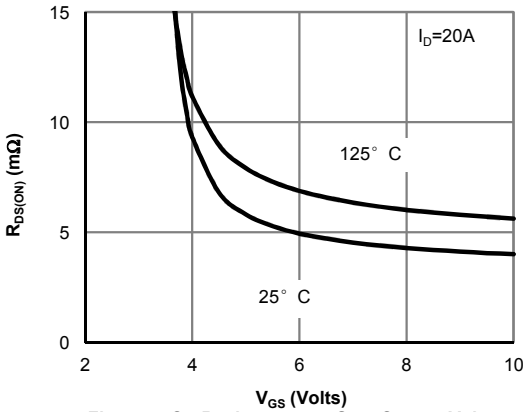


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

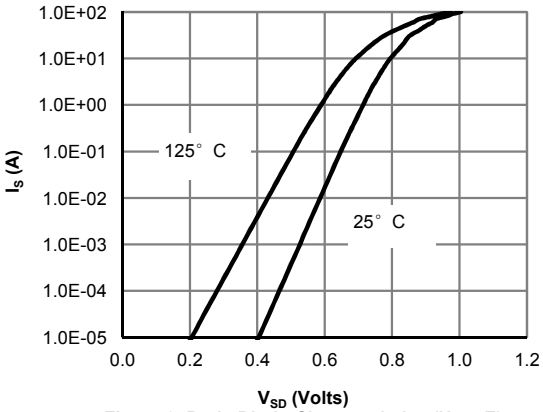


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

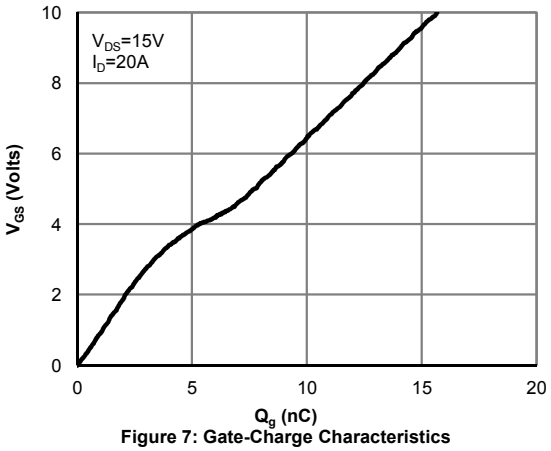


Figure 7: Gate-Charge Characteristics

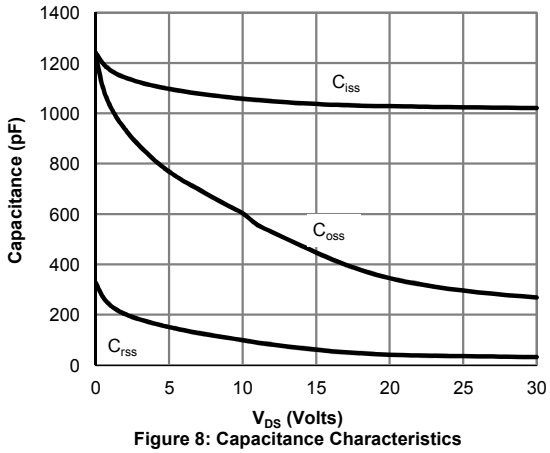


Figure 8: Capacitance Characteristics

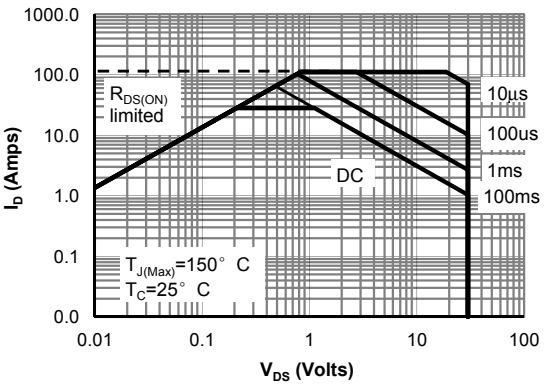


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

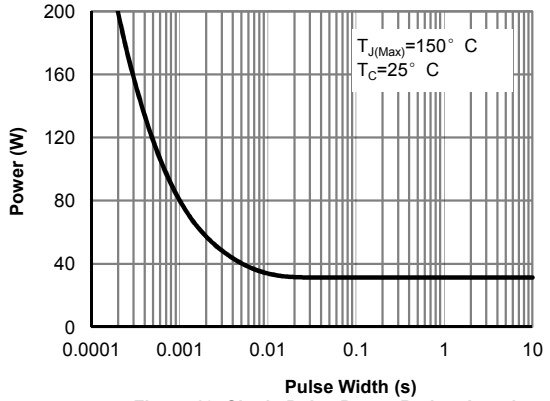


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

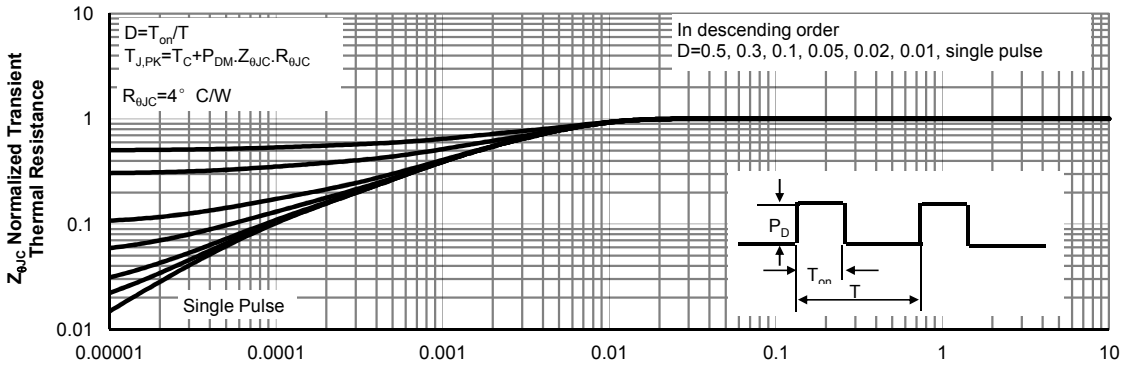


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

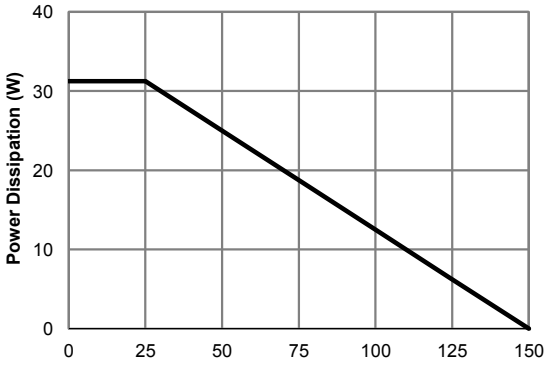


Figure 12: Power De-rating (Note F)

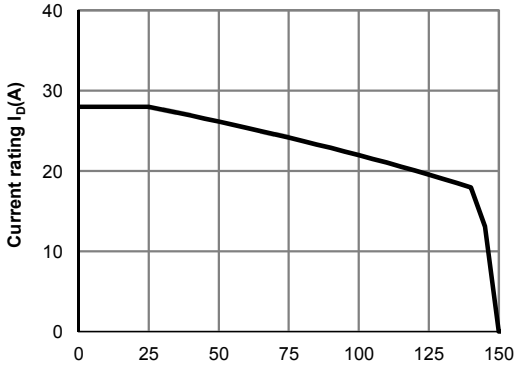


Figure 13: Current De-rating (Note F)

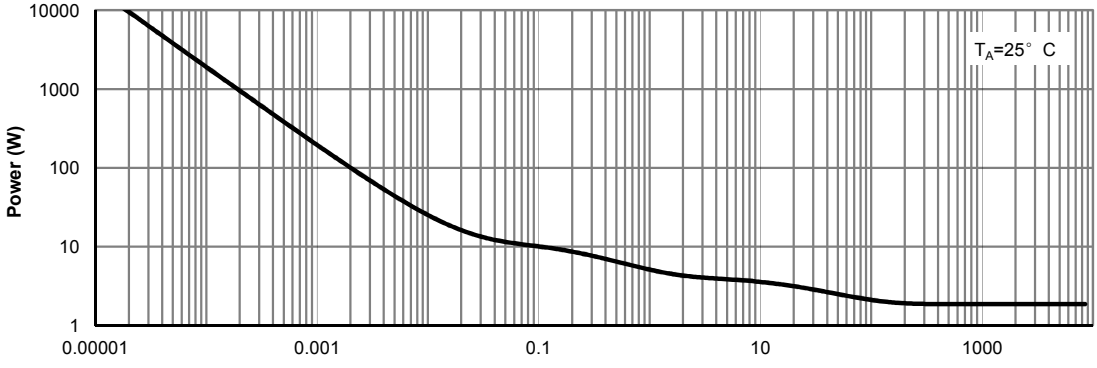


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

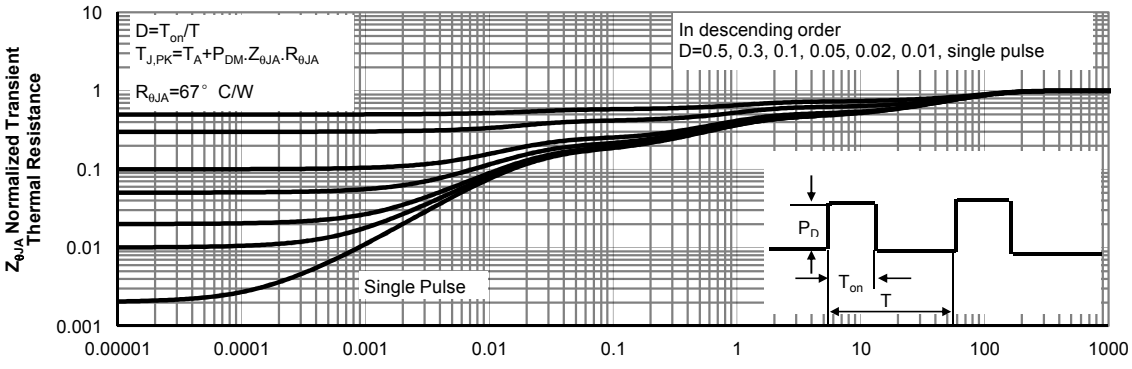


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.1	1.5	1.9	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		1.8	2.5	mΩ
		T_J=125°C		2.3	3.2	
		V_{GS}=4.5V, I_D=20A		2.4	3.2	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		85		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current[G]				42	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		3430		pF
C_{oss}	Output Capacitance			1327		pF
C_{rss}	Reverse Transfer Capacitance			175		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.3	0.7	1.1	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A		53	64	nC
Q_g(4.5V)	Total Gate Charge			25	30	nC
Q_{gs}	Gate Source Charge			7.8		nC
Q_{gd}	Gate Drain Charge			10.3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		7.5		ns
t_r	Turn-On Rise Time			5.0		ns
$t_{D(off)}$	Turn-Off DelayTime			33.8		ns
t_f	Turn-Off Fall Time			9.8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs		22		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs		58		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is limited by package.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with TA=25° C.

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

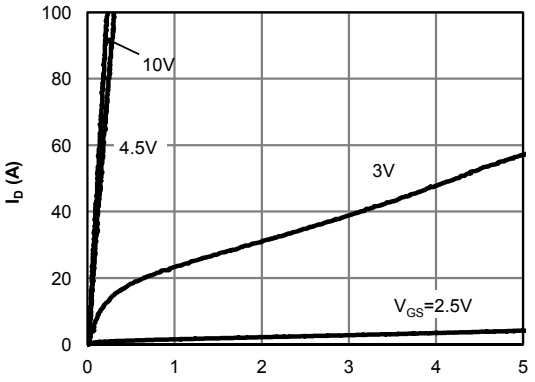


Fig 1: On-Region Characteristics (Note E)

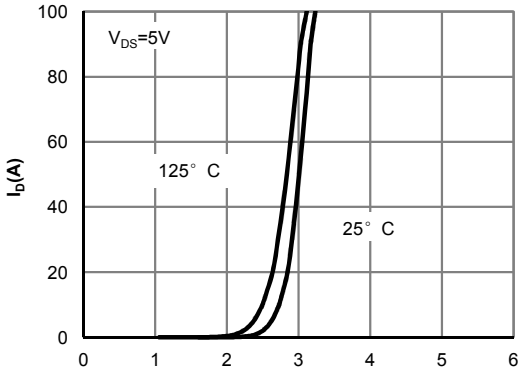


Figure 2: Transfer Characteristics (Note E)

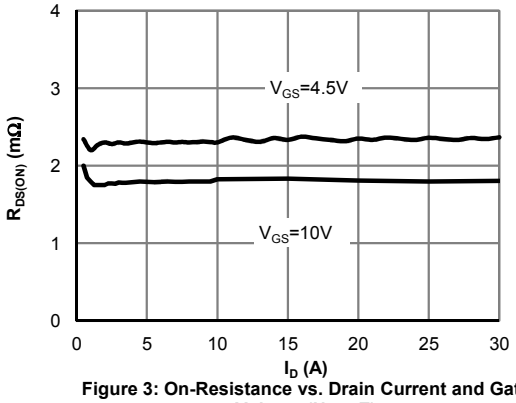


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

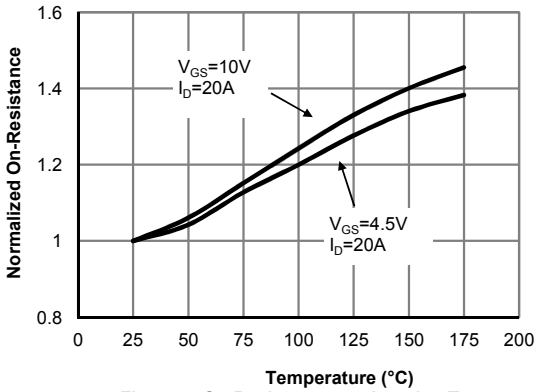


Figure 4: On-Resistance vs. Junction Temperature (Note E)

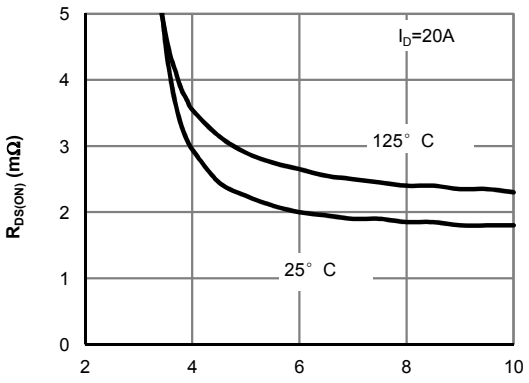


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

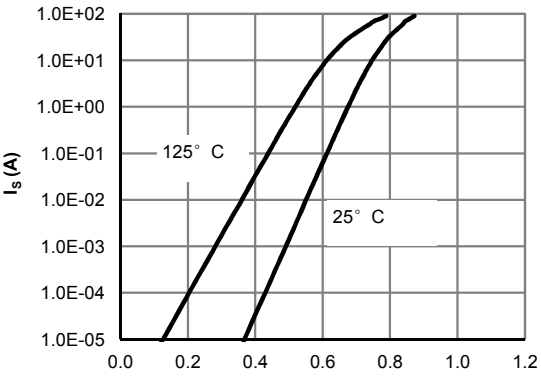


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

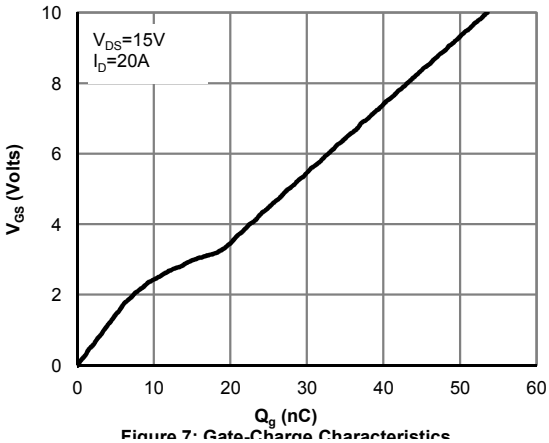


Figure 7: Gate-Charge Characteristics

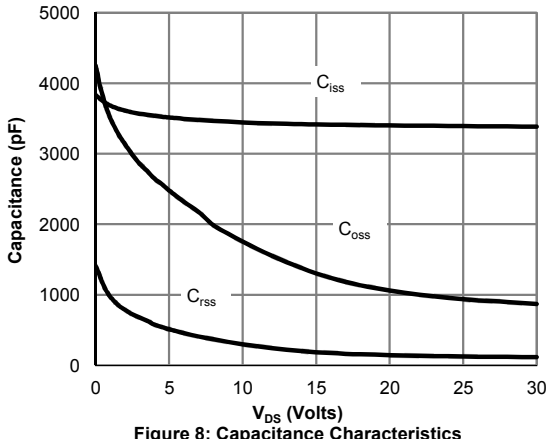


Figure 8: Capacitance Characteristics

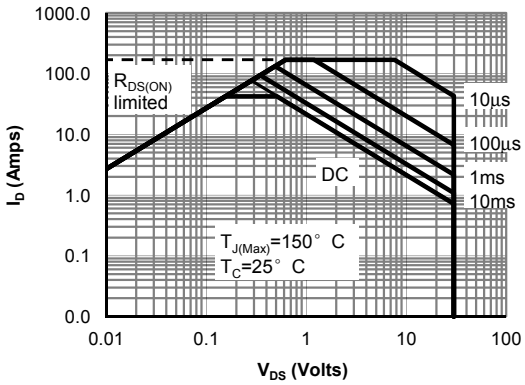


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

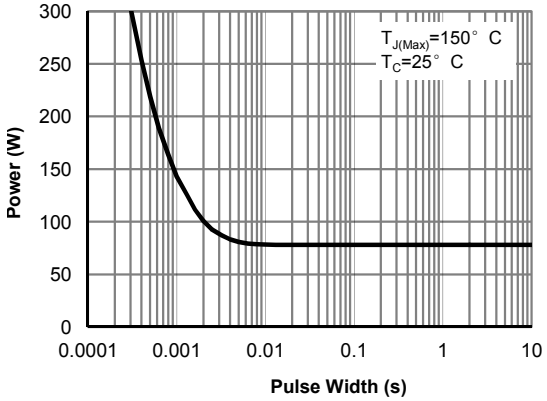


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

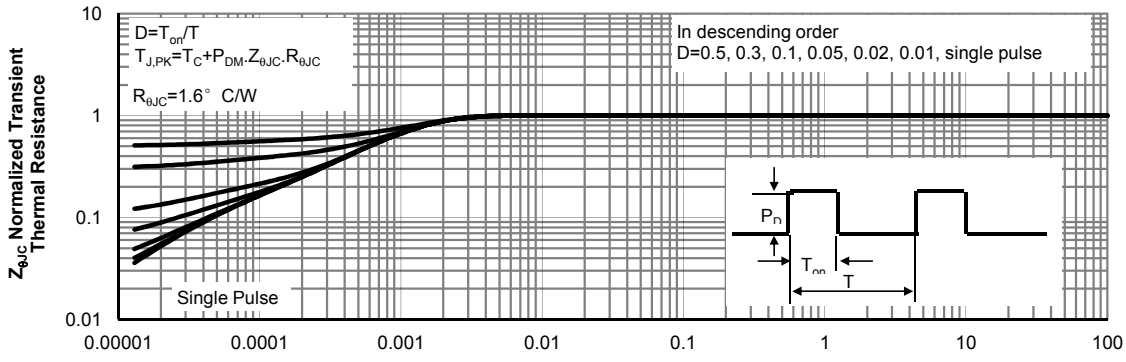


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

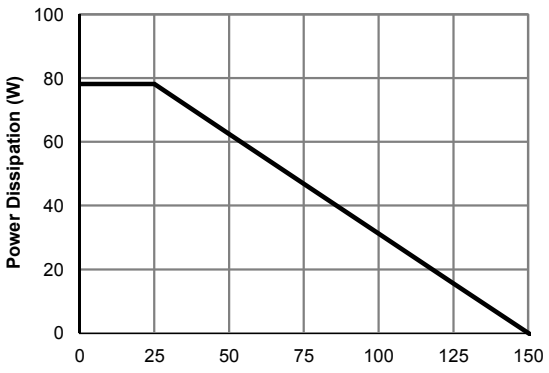


Figure 12: Power De-rating (Note F)

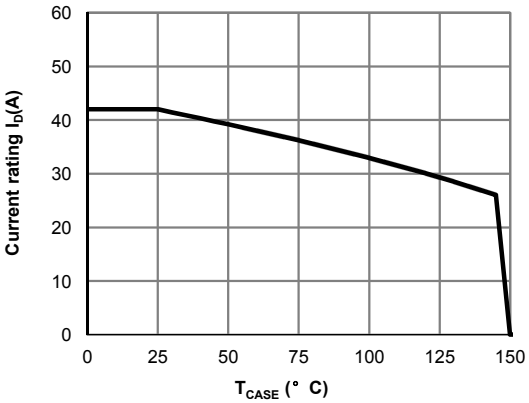


Figure 13: Current De-rating (Note F)

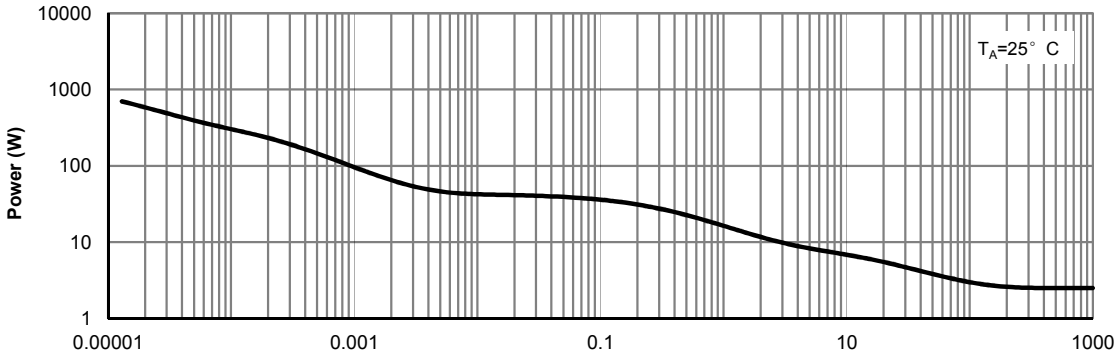


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

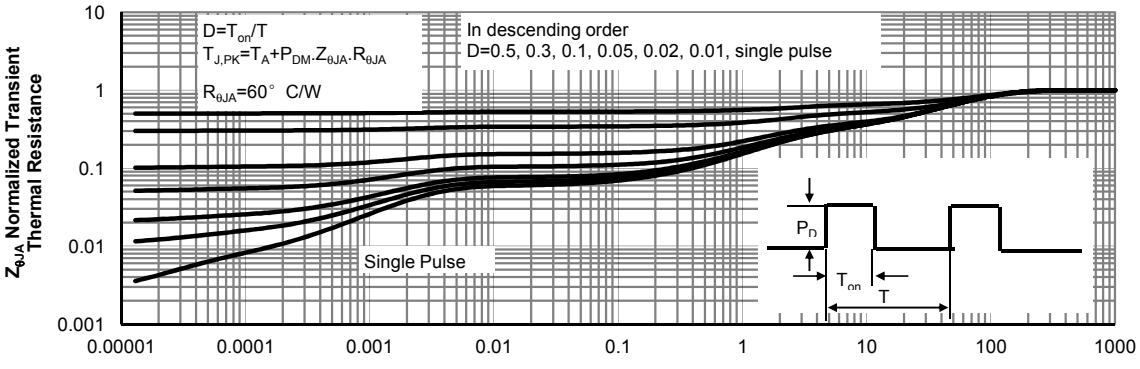
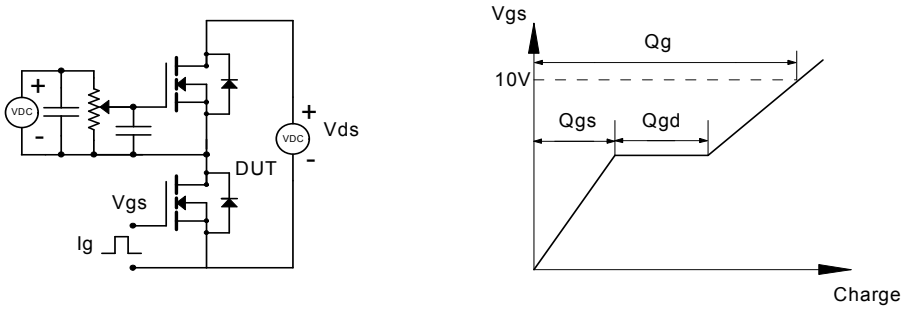
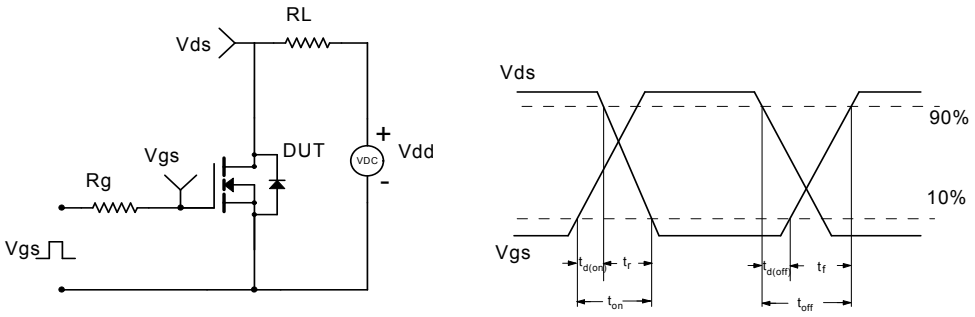


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

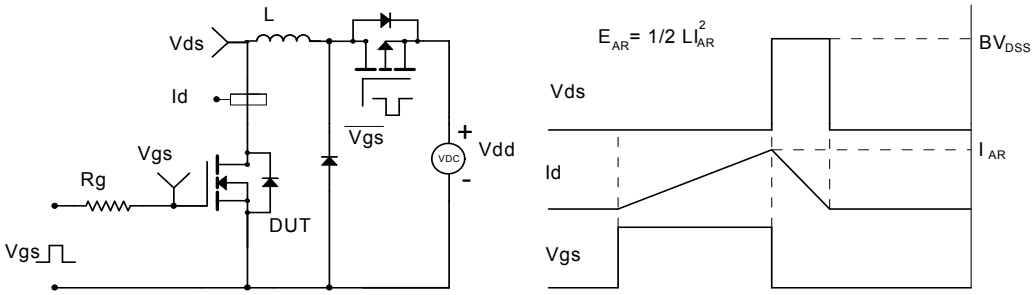
Gate Charge Test Circuit & Waveform



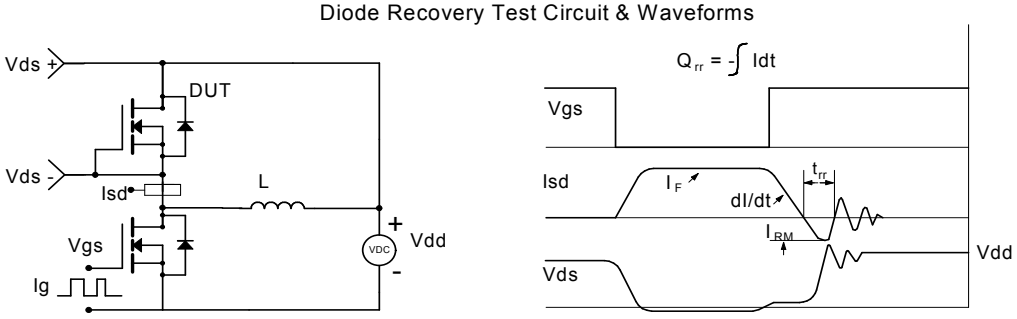
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



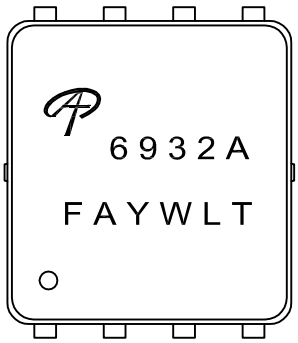
Diode Recovery Test Circuit & Waveforms



ALPHA & OMEGA SEMICONDUCTOR

Document No.	PD-01957
Version	A
Title	AON6932A Marking Description

DFN5X6 PACKAGE MARKING DESCRIPTION



Green product

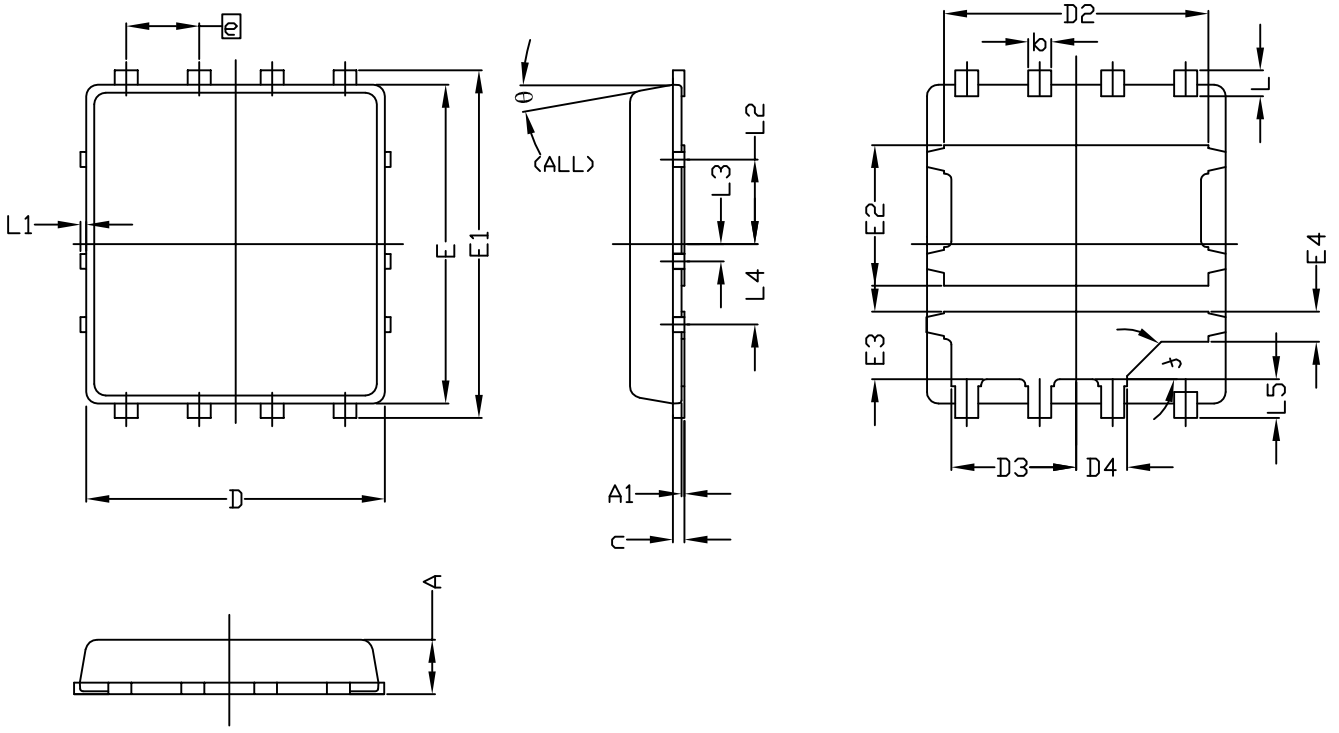
NOTE:
LOGO - AOS Logo
6932A - Part number code
F - Fab code
A - Assembly location code
Y - Year code
W - Week code
L&T - Assembly lot code

PART NO.	DESCRIPTION	CODE
AON6932A	Green product	6932A
AON6932AL	Green product	6932A

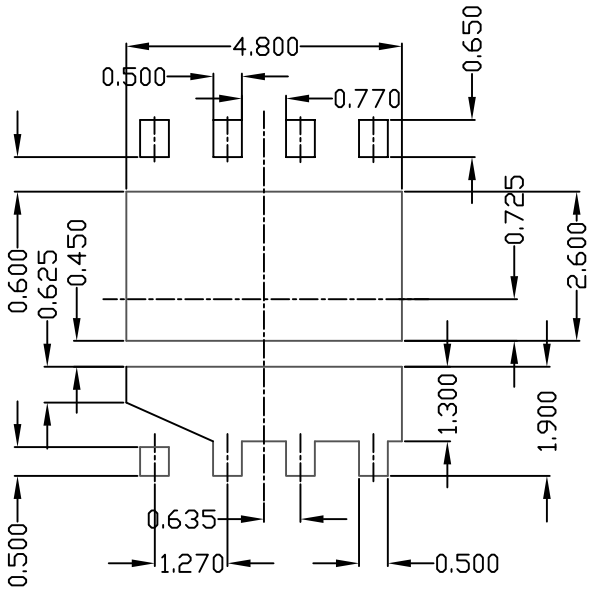
ALPHA & OMEGA SEMICONDUCTOR

Document No.	PO-00122
Version	C

DFN5x6B_8L_EP2_P PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.90	1.00	0.033	0.035	0.039
A1	0.00	——	0.05	0.000	——	0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.20 BSC			0.205 BSC		
D2	4.50	4.60	4.70	0.177	0.181	0.185
D3	2.125	2.175	2.225	0.084	0.086	0.088
D4	0.835	0.885	0.935	0.033	0.035	0.037
E	5.55 BSC			0.219 BSC		
E1	6.05 BSC			0.238 BSC		
E2	2.10	——	2.50	0.083	——	0.098
E3	1.10	——	1.225	0.043	——	0.048
E4	0.45	——	0.575	0.018	——	0.023
e	1.27 BSC			0.050 BSC		
L	0.35	0.45	0.55	0.014	0.018	0.022
L1	0	——	0.10	0	——	0.004
L2	1.375	1.475	1.575	0.054	0.058	0.062
L3	0.20	0.30	0.40	0.008	0.012	0.016
L4	1.30	1.40	1.50	0.051	0.055	0.059
L5	0.575	0.675	0.775	0.023	0.027	0.031
f	45°			45°		
θ	0°	——	10°	0°	——	10°

UNIT: mm

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

AOS Semiconductor
Product Reliability Report

AON6932A, rev A

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

This AOS product reliability report summarizes the qualification result for AON6932A. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AON6932A passes AOS quality and reliability requirements. The released product will be categorized by the process family and be monitored on a quarterly basis for continuously improving the product quality.

Table of Contents:

I. Product Description:

General description:
• Latest Trench Power AlphaMOS (αMOS LV) technology
• Very Low RDS(on) at 4.5VGS
• Low Gate Charge
• High Current Capability
• RoHS and Halogen-Free Compliant

Application:
• DC/DC Converters in Computing, Servers, and POL
• Isolated DC/DC Converters in Telecom and Industrial

Detailed information refers to datasheet.

II. Die / Package Information:

	AON6932A
Process	Standard sub-micron 30V Dual N channel
Package Type	DFN 5x6B
Lead Frame	Cu
Die Attach	Ag epoxy
Bonding	Cu & Au wire
Mold Material	Epoxy resin with silica filler
MSL (moisture sensitive level)	Level 1 based on J-STD-020

Note * based on information provided by assembler and mold compound supplier

ALPHA & OMEGA SEMICONDUCTOR

III. Result of Reliability Stress for AON6932A

Test Item	Test Condition	Time Point	Lot Attribution	Total Sample size	Number of Failures	Standard
MSL Precondition	**168hr 85℃ /85%RH +3 cycle reflow@260℃**	**-**	**11 lots**	**2299pcs**	**0**	**JESD22-A113**
HTGB	**Temp = 150 °c, Vgs=100% of Vgsmax**	**168hrs 500 hrs 1000 hrs**	**1 lot 3 lots (Note A*)**	**308pcs 77pcs / lot**	**0**	**JESD22-A108**
HTRB	**Temp = 150 °c, Vds=80% of Vdsmax**	**168hrs 500 hrs 1000 hrs**	**1 l ot 3 lots (Note A*)**	**308pcs 77pcs / lot**	**0**	**JESD22-A108**
HAST	**130 °c, 85%RH, 33.3 psi, Vgs = 100% of Vgs max**	**100 hrs**	**11 lots (Note A*)**	**605pcs 55pcs / lot**	**0**	**JESD22-A110**
Pressure Pot	**121°c, 29.7psi, RH=100%**	**96 hrs**	**11 lots (Note A*)**	**847pcs 77pcs / lot**	**0**	**JESD22-A102**
Temperature Cycle	**-65°c to 150°c, air to air**	**250 / 500 cycles**	**11 lots (Note A*)**	**847pcs 77pcs / lot**	**0**	**JESD22-A104**

Note A: The reliability data presents total of available generic data up to the published date.

IV. Reliability Evaluation

FIT rate (per billion): 7
MTTF = 15704 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the selected product (AON6932A). Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 \times 10^9$ **/ [**2 (N) (H) (Af)**]**
= 1.83×10^9 **/ [**2x (2x77x168+6x77x1000) x258**]** = 7
MTTF = 10^9 / FIT = 1.38×10^8hrs = 15704 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from HTRB and HTGB tests
H = Duration of HTRB/HTGB testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55℃)
Acceleration Factor [Af**]** = **Exp** [Ea / **k** (1/Tj u – 1/Tj s)]
Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	**258**	**87**	**32**	**13**	**5.64**	**2.59**	**1**

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16
Tj u = The use junction temperature in degree (Kelvin), K = C+273.16
K = Boltzmann's constant, 8.617164×10^{-5}eV / K