



ALGOLTEK

AG6201

HDMI1.4 to VGA

Converter

with Embedded Audio DAC

Data Sheet

Preliminary Version

V0.9

July, 2018

Revision History

Version	Date	Notes
0.9	2018/7/13	Preliminary release

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I. General Description

ALGOLTEK AG6201 is a high-performance, cost effective single-chip solution to implement HDMI1.4 high resolution video to VGA converter. With embedded audio DAC, customers can save the BOM cost and reduce the PCB size. The internal audio DAC can be turned off via the external circuits if it is not required. With **ALGOLTEK**'s ultra-low power design, AG6201 can perform stand-alone operation without external power source.

II. Features

- Video resolution support up to 1920x1200@60Hz
- Support Hot Plug Detection
- Embedded Crystal, Crystal-less in components
- Embedded 8-bit audio DAC
- Built-in 3.3V and 1.2V voltage regulators
- On-chip HDCP Engine which is compliant with HDCP 1.4 specification
- Integrated on-chip HDCP1.4 Keys
- 1.2V Core power and 3.3V I/O power
- 2KV ESD performance
- Operating temperature range: 0°C to +70°C

III. Device Information

Part Number	Package	Body Size
AG6201-MAQ	QFN-48	6x6 mm ²

IV. Application

- HDMI to VGA dongle
- Docking stations

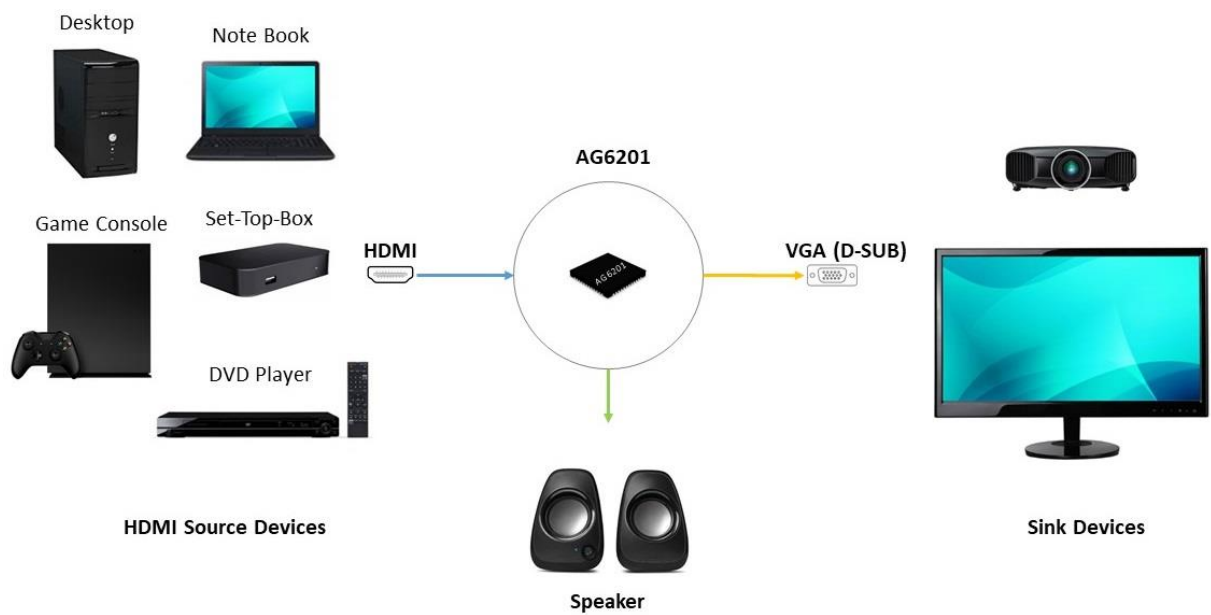


Figure 1 Application for HDMI to VGA Dongle

V. System Block Diagram

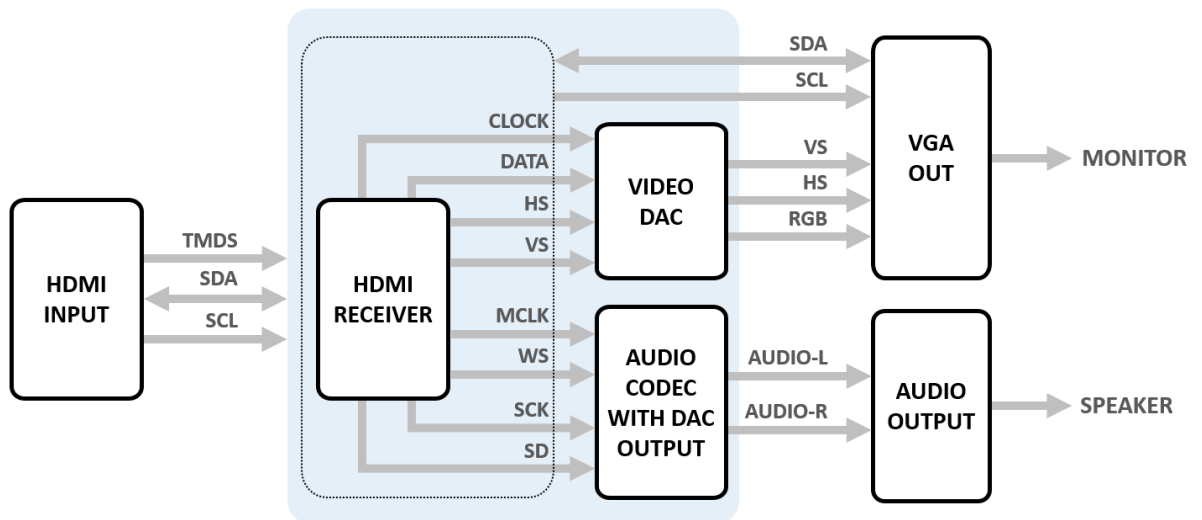


Figure 2 System Block Diagram

VI. Pin Definition and Functions

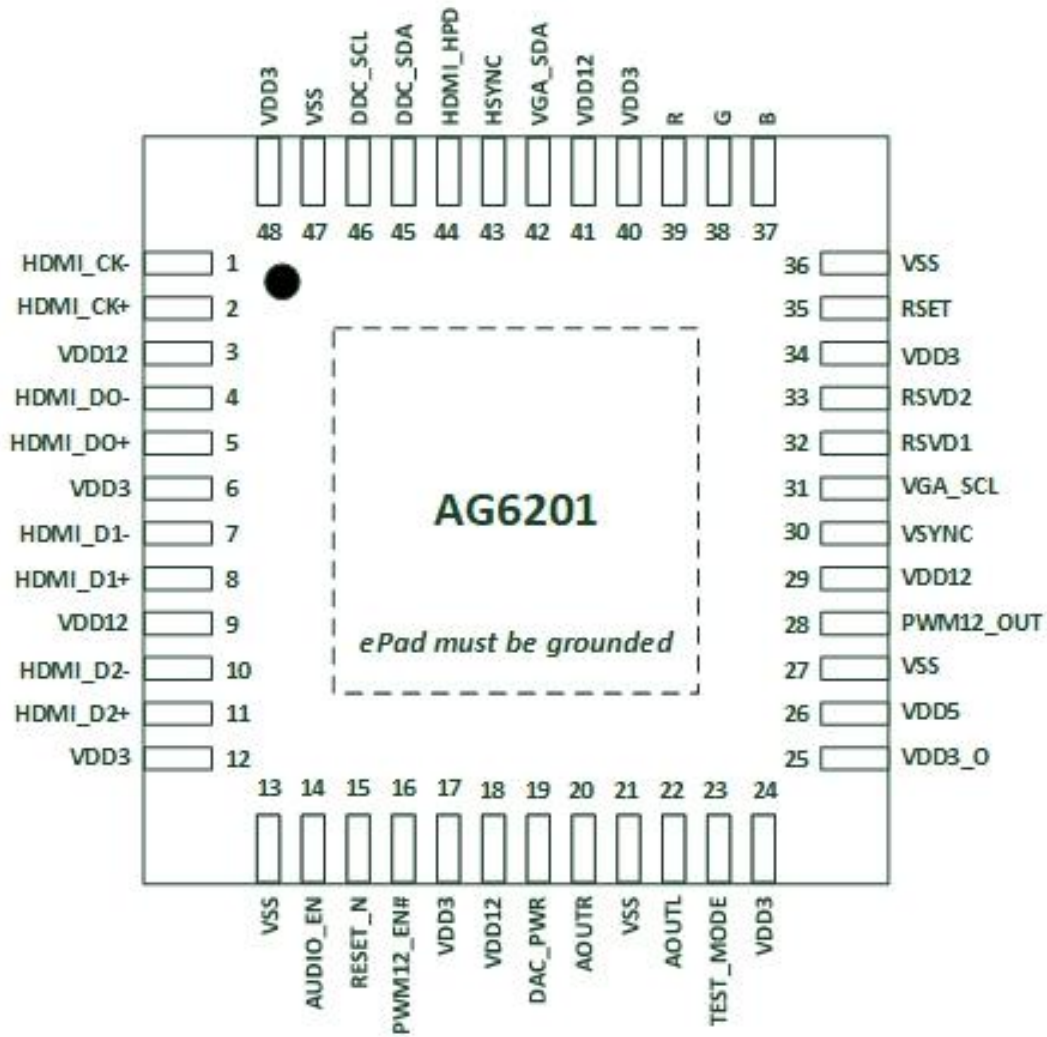


Figure 3 PIN Definition

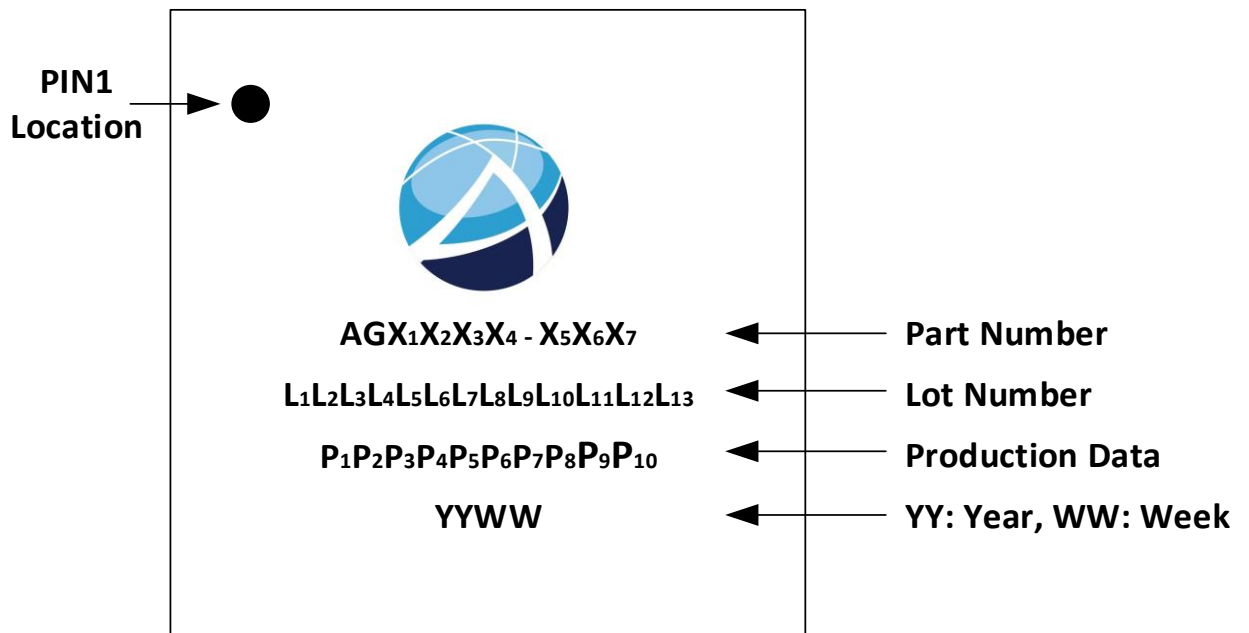
Table 1 Pin Description

PIN NAME	PIN	TYPE	DESCRIPTION
POWER SUPPLY			
VDD5	26	Power	5V Power input
VDD3	6, 12, 17, 24, 34, 40, 48	Power	3.3V Power input
VDD12	3, 9, 18, 29, 41	Power	1.2V power input
VDD3_OUT	25	Power	On-chip 3.3V regulator power output
PWM12_OUT	28	Power	On-chip PWM 1.2V regulator power output
VSS	13, 21, 27, 36, 47, EPAD	Power	Ground
DIFFERENTIAL HIGH-SPEED IO			
HDMI_CK-	1	Input	HDMI RX clock channel negative
HDMI_CK+	2	Input	HDMI RX clock channel positive
HDMI_D0-	4	Input	HDMI RX data channel 0 negative
HDMI_D0+	5	Input	HDMI RX data channel 0 positive
HDMI_D1-	7	Input	HDMI RX data channel 1 negative
HDMI_D1+	8	Input	HDMI RX data channel 1 positive
HDMI_D2-	10	Input	HDMI RX data channel 2 negative
HDMI_D2+	11	Input	HDMI RX data channel 2 positive
Digital IO			
AUDIO_EN	14	Input	Audio DAC control, Internal had a weakness pull-up resistor. NC = enable L = disable (pull-down a 1K ohm resistor to GND)
RESET_N	15	Input	An available external Reset signal for system implementation. Active LOW reset signal to the device Note: On-chip POR reset is available and this pin ONLY reserved for system HOST adjust reset timing in case any unexpected state.
PWM12_EN#	16	Input	1.2V internal regulator control NC = enable H = disable (pull up a 1.8K ohm resistor to 3.3V)

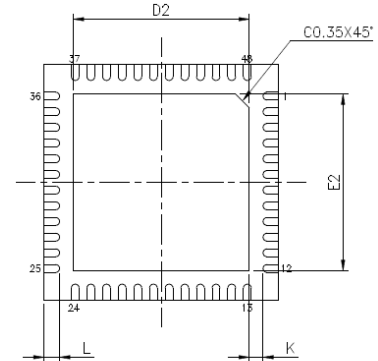
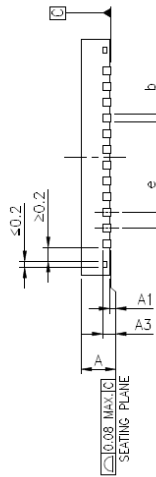
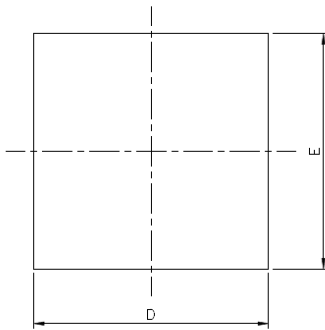
PIN NAME	PIN	TYPE	DESCRIPTION
TEST_MODE	23	Bidirectional	Factory test only Connect this signal to VDD3 through a 0Ω resistor
VSYNC	30	Output	Vertical sync signal
VGA_SCL	31	Bidirectional	VGA I2C Clock
RSVD1	32	Bidirectional	Reserved. Default NC. Reserved pull- down 1K ohm resistor is highly recommend.
RSVD2	33	Bidirectional	Reserved. Default NC. Reserved pull- down 1K ohm resistor is highly recommend.
VGA_SDA	42	Bidirectional	VGA I2C Data
HSYNC	43	Output	Horizontal sync signal
HDMI_HPD	44	Output	HDMI RX Hot-Plug Detect output
DDC_SDA	45	Bidirectional	DDC I2C Data for HDMI Port
DDC_SCL	46	Bidirectional	DDC I2C Clock for HDMI Port
Analog IO			
DAC_PWR	19	Output	On-chip Power domain for embedded Audio DAC
AOUTR	20	Output	Audio Right Channel Output
AOUTL	22	Output	Audio Left Channel Output
RSET	35	Input	Adjust voltage swing of R/G/B signals. Pull-down 4.7K ohm resistor to ground by default. Note: Increasing resistance is degrade voltage swing, versus decreasing resistance will upgrade voltage swing.
B	37	Output	Blue channel output Pull down to ground by an 75 ohm resistor
G	38	Output	Green channel output Pull down to ground by an 75 ohm resistor
R	39	Output	Red channel output Pull down to ground by an 75 ohm resistor

VII. Package Outline

VII.1 Marking



VII.2 Package Dimension



JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X648)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	6.00 BSC		
E	6.00 BSC		
e	0.40 BSC		
K	0.20	—	—

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE	WQFN	WQFN	UQFN	TQFN OPTION 1	TQFN OPTION 2
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF						
185X18* MIL	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45	√	X	(W)VJJE-1	√	√	—	—	—

VIII. Contact Information

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