4V3422 Data Sheets

(Vision 1.1)

4V3422 2M-Bits FIFO Field Memory

Contents:

1.0 Description

The 4V3422 is a general purpose FIFO (First-In-First-Out) memory. The product consists of 2M-bits of memory cell, and is configured as 262,144 words x 8 bit allowing sequentially buffer data without sending address for data read or write. The chip embeds complicated DRAM controller so that its bus interface is very user-friendly.

2M-bits size of memory capacity can hold not only for one TV field, but also enough to hold a whole PC video frame which normally contains 640x480 or 720x480 bytes. The 4V3422 device is available in 28-pin SOP package and is pin/function compatible to industrial standard, such as AL422B FIFO (of AverLogic).

2.0 Features

- 256K (262,144) x 8 bits FIFO organization
- Support VGA, NTSC or PAL resolutions
- Independent read/write operations (different I/O data rates acceptable)
- High speed asynchronous serial access
- Read/write cycle time: 20ns
- Access time: 15ns
- Output enable control (data skipping)
- Self refresh
- 5V or 3.3V power supply
- Standard 28-pin SOP package
- (option) 28-pin SOP Pb-free package

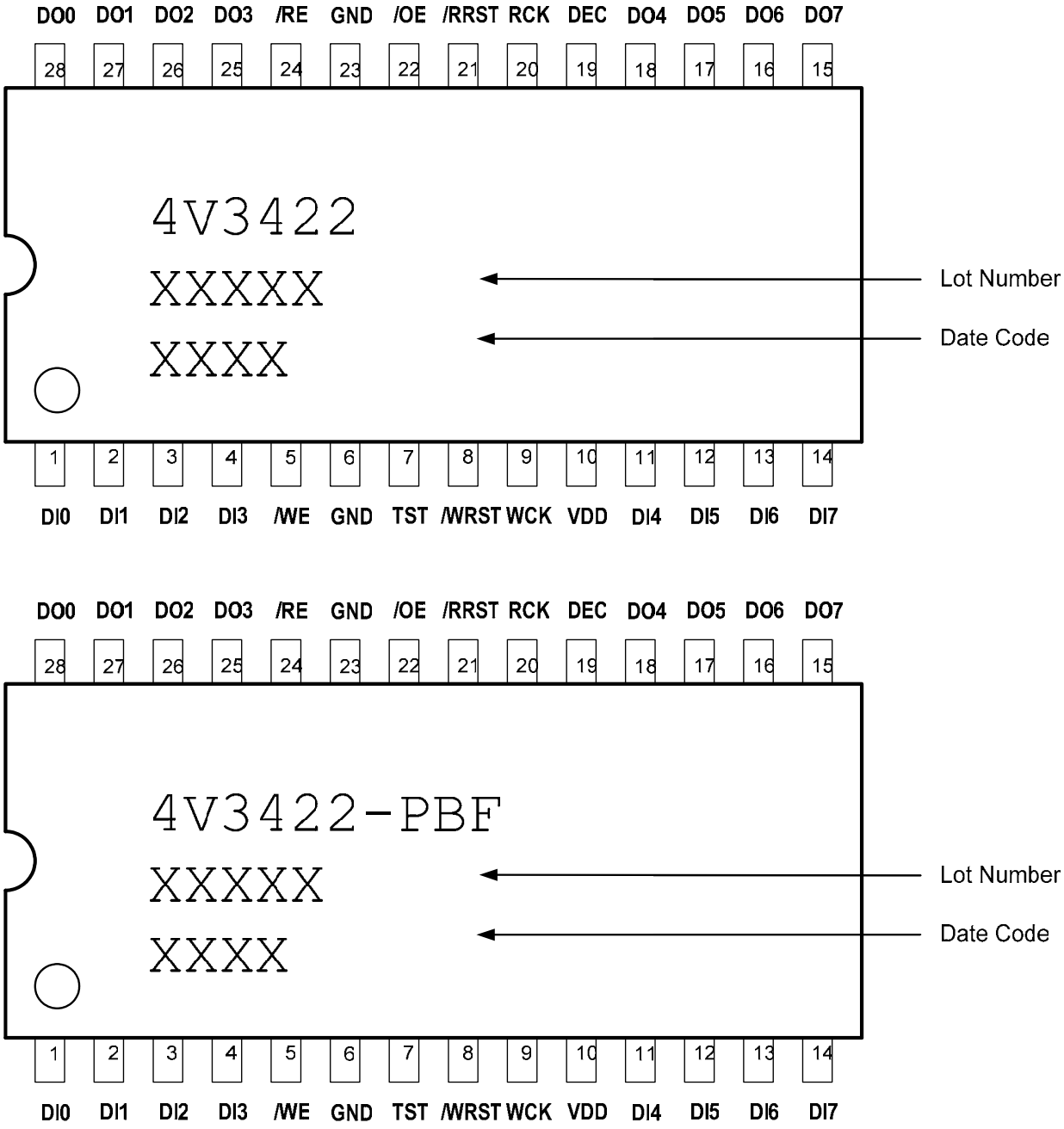
3.0 Applications

- Multimedia systems
- Video capture systems
- Video editing systems
- Scan rate converters
- TV's picture in picture feature
- Time base correction (TBC)
- Frame synchronizer
- Digital video camera
- Buffer for communications systems

4.0 Ordering Information

Part number	Package	Power Supply	Status
4V3422	28-pin plastic SOP	+3.3 volt	Shipping
4V3422-PBF	28-pin plastic SOP	+3.3 volt	Sample 2006

5.0 Pin-out Diagram



Note: “PBF” to indicate it is Pb free package.

6.0 Pin Description

Pin name	Pin #	I/O type	Function
DI0~DI7	1~4, 11~14	input	Data input
WCK	9	Input	Write clock
/WE	5	Input (active low)	Write enable
/WRST	8	Input (active low)	Write reset
DO0~DO7	15~18, 25~28	Output (tristate)	Data output
RCK	20	Input	Read clock
/RE	24	Input (active low)	Read enable
/RRST	21	Input (active low)	Read reset
/OE	22	Input (active low)	Output enable
TST	7	Input	Test pin (pulled-down)*
VDD	10		5V or 3.3V
DEC/VDD	19		Decoupling cap input
GND	6, 23		Ground

7.0 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter		Ratings		Unit
		3.3V application	5V application	
V_{DD}	Supply Voltage	-1.0 ~ +4.5	-1.0 ~ +7.0	V
V_P	Pin Voltage	-1.0 ~ +5.5	-1.0 ~ V_{DD} +0.5	V
I_O	Output Current	-20 ~ +20	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +70	0 ~ +70	°C
T_{stg}	Storage temperature	-55 ~ +125	-55 ~ +125	°C

7.2 Recommended Operating Conditions

Parameter		3.3V application		5V application		Unit
		Min	Max	Min	Max	
V_{DD}	Supply Voltage	+3.0	+3.6	+4.5	+5.25	V
V_{IH}	High Level Input Voltage	+2.0	+5.5	+3.0	V_{DD} +0.5	V
V_{IL}	Low Level Input Voltage	-1.0	+0.8	-1.0	+0.8	V

7.3 DC Characteristics

(V_{DD} =5V or 3.3V, Vss=0V. T_{AMB} = 0 to 70°C)

Parameter		3.3V application			5V application			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{DD}	Operating Current @20MHz	-	33	-	-	50	-	mA
I_{DD}	Operating Current @30MHz	-	45	-	-	66	-	mA
I_{DD}	Operating Current @40MHz	-	57	-	-	82	-	mA
I_{DD}	Operating Current @50MHz	-	68	-	-	97	-	mA
I_{DDS}	Standby Current	-	7	-	-	12	-	mA
V_{OH}	Hi-level Output Voltage	$0.7V_{DD}$	-	V_{DD}	+3.0	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	-	-	+0.4	V
I_{LI}	Input Leakage Current	-10	-	+10	-10	-	+10	μA
I_{LO}	Output Leakage Current	-10	-	+10	-10	-	+10	μA

7.4 AC Characteristics

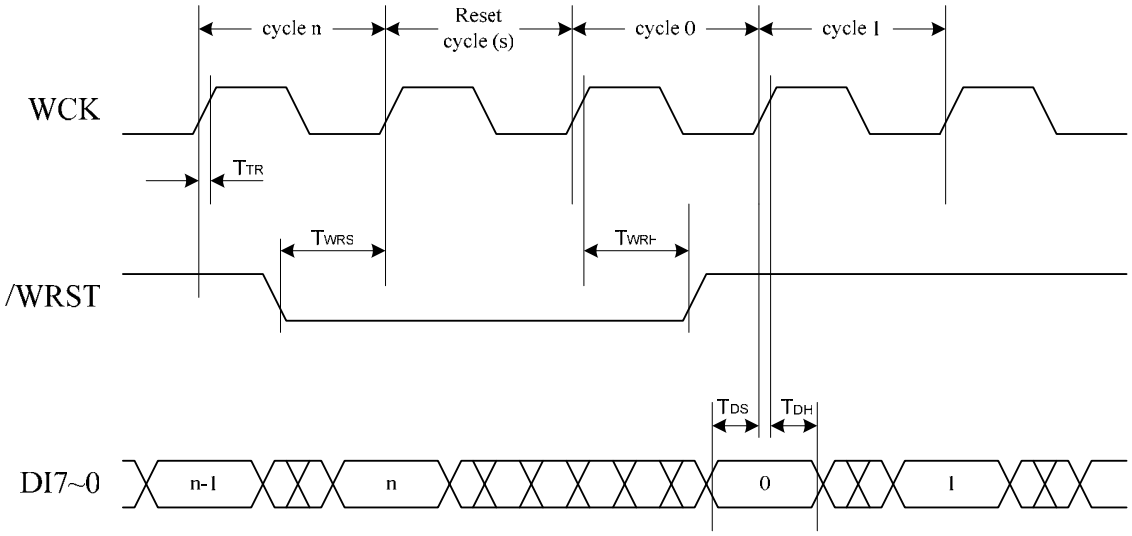
(V_{DD} =5V or 3.3V, Vss=0V, T_{AMB} = 0 to 70°C)

Parameter		3.3V application		5V application		Unit
		Min	Max	Min	Max	
T_{WC}	WCK Cycle Time	20	1000	20	1000	ns
T_{WPH}	WCK High Pulse Width	7	-	7	-	ns
T_{WPL}	WCK Low Pulse Width	7	-	7	-	ns
T_{RC}	RCK Cycle Time	20	1000	20	1000	ns
T_{RPH}	RCK High Pulse Width	7	-	7	-	ns
T_{RPL}	RCK Low Pulse Width	7	-	7	-	ns

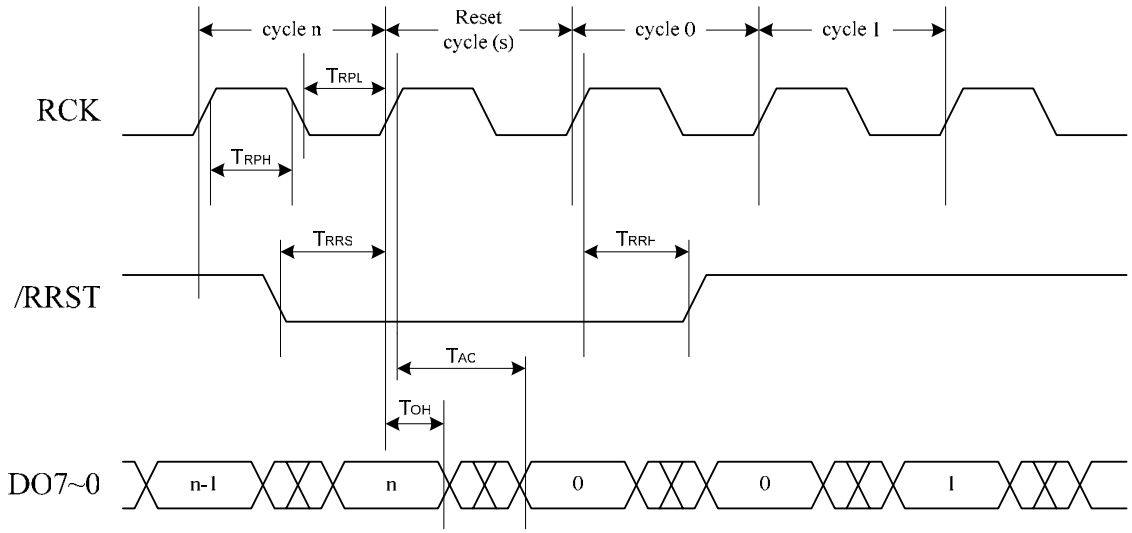
T_{AC}	Access Time	-	15	-	15	ns
T_{OH}	Output Hold Time	4	-	4	-	ns
T_{HZ}	Output High-Z Setup Time	3	15	4	15	ns
T_{LZ}	Output Low-Z Setup Time	3	15	4	15	ns
T_{WRS}	/WRST Setup Time	5	-	6	-	ns
T_{WRH}	/WRST Hold Time	2	-	3	-	ns
T_{RRS}	/RRST Setup Time	5	-	6	-	ns
T_{RRH}	/RRST Hold Time	2	-	3	-	ns
T_{DS}	Input Data Setup Time	5	-	6	-	ns
T_{DH}	Input Data Hold Time	2	-	3	-	ns
T_{WES}	/WE Setup Time	5	-	6	-	ns
T_{WEH}	/WE Hold Time	2	-	3	-	ns
T_{WPW}	/WE Pulse Width	10	-	10	-	ns
T_{RES}	/RE Setup Time	5	-	6	-	ns
T_{REH}	/RE Hold Time	2	-	3	-	ns
T_{RPW}	/RE Pulse Width	10	-	10	-	ns
T_{OES}	/OE Setup Time	5	-	6	-	ns
T_{OEH}	/OE Hold Time	2	-	3	-	ns
T_{OPW}	/OE Pulse Width	10	-	10	-	ns
T_{TR}	Transition Time	2	20	3	20	ns
C_I	Input Capacitance	-	7	-	7	pF
C_O	Output Capacitance	-	7	-	7	pF

- Input voltage levels are defined as VIH=3.0V and VIL=0.4V.
- The read address needs to be at least 128 cycles after the write address.

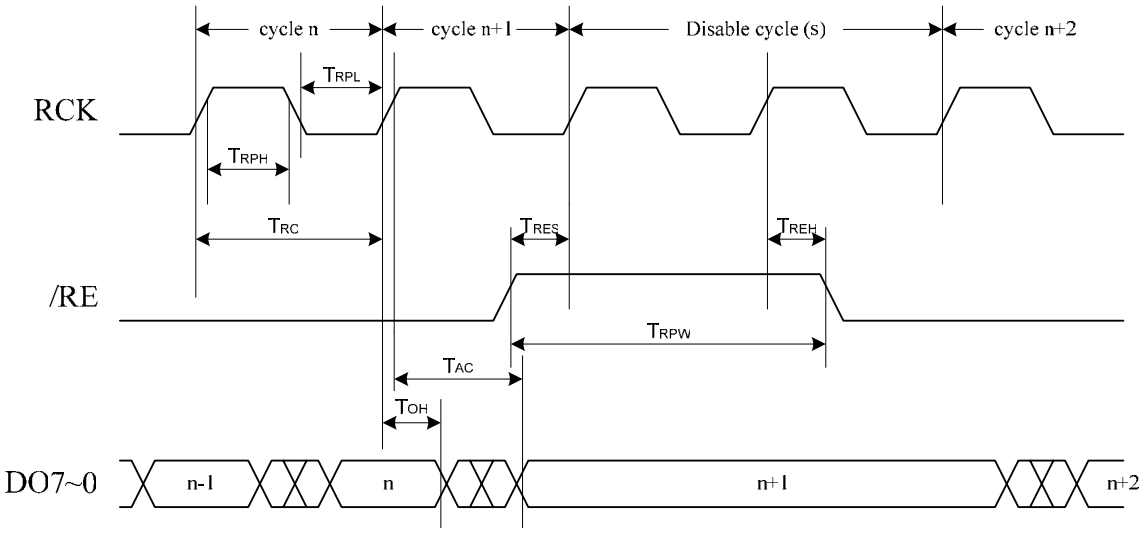
7.5 Timing Diagrams



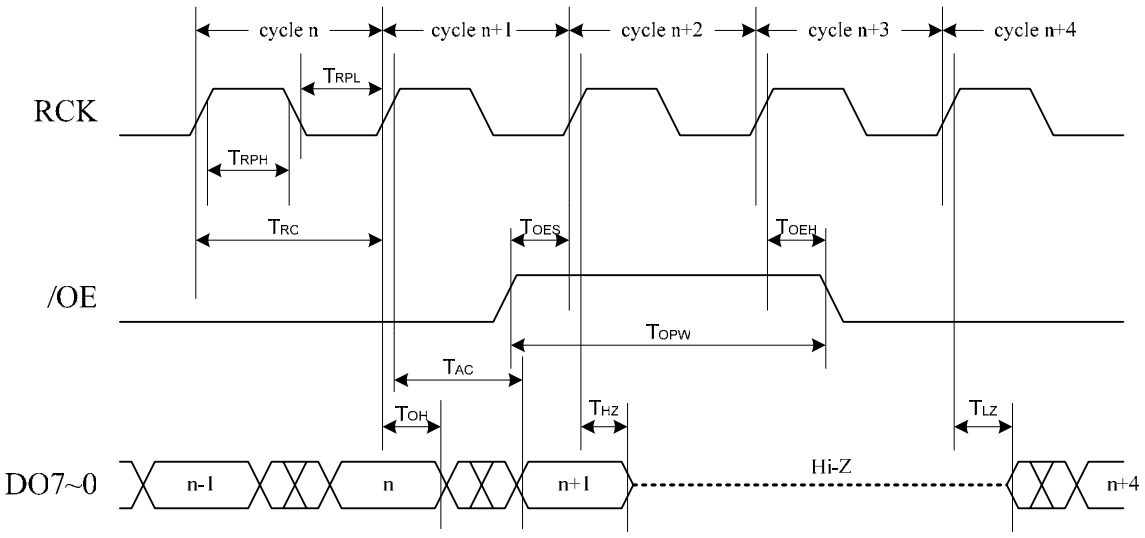
Write Cycle Timing (Write Reset)



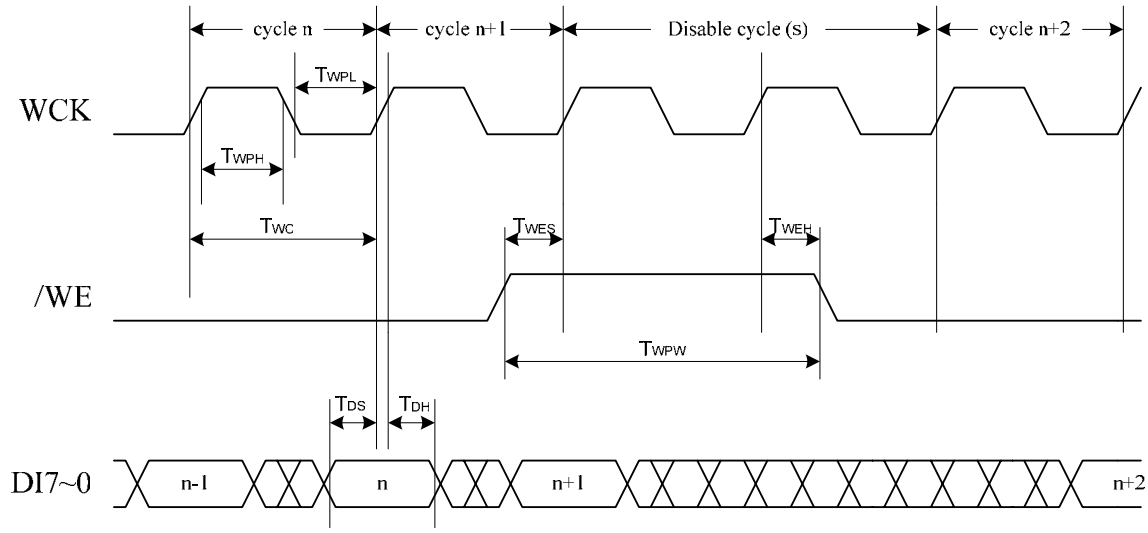
Read Cycle Timing (Read Reset)



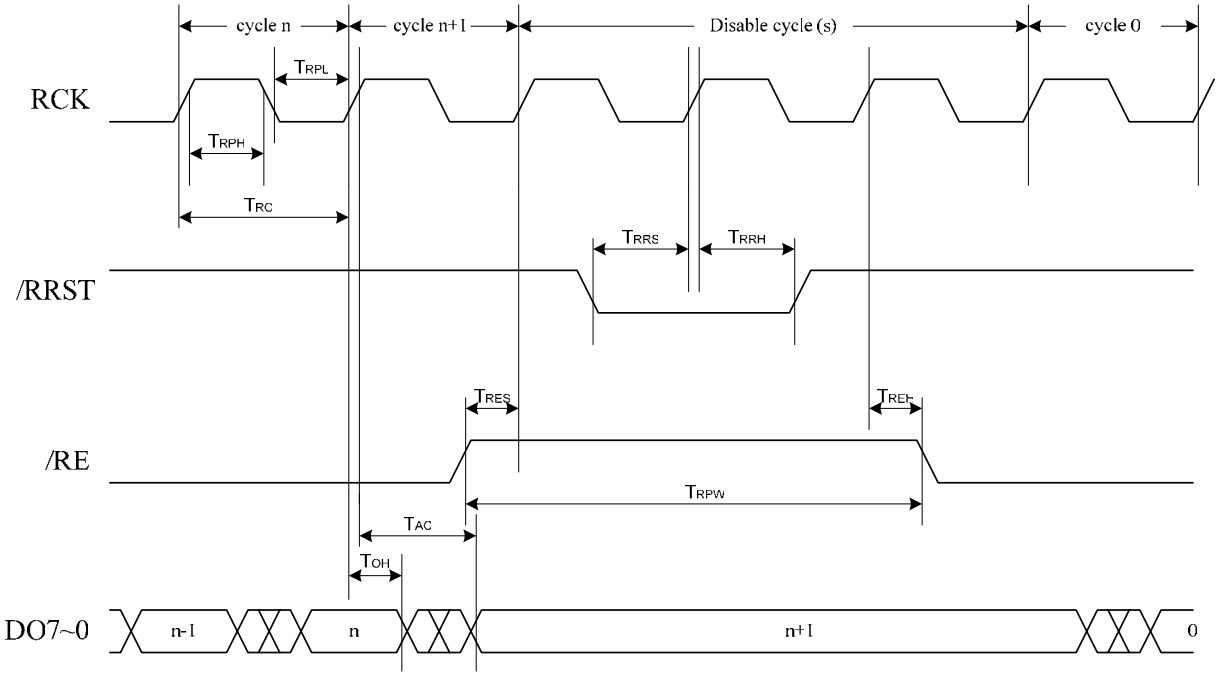
Read Cycle Timing (Read Enable)



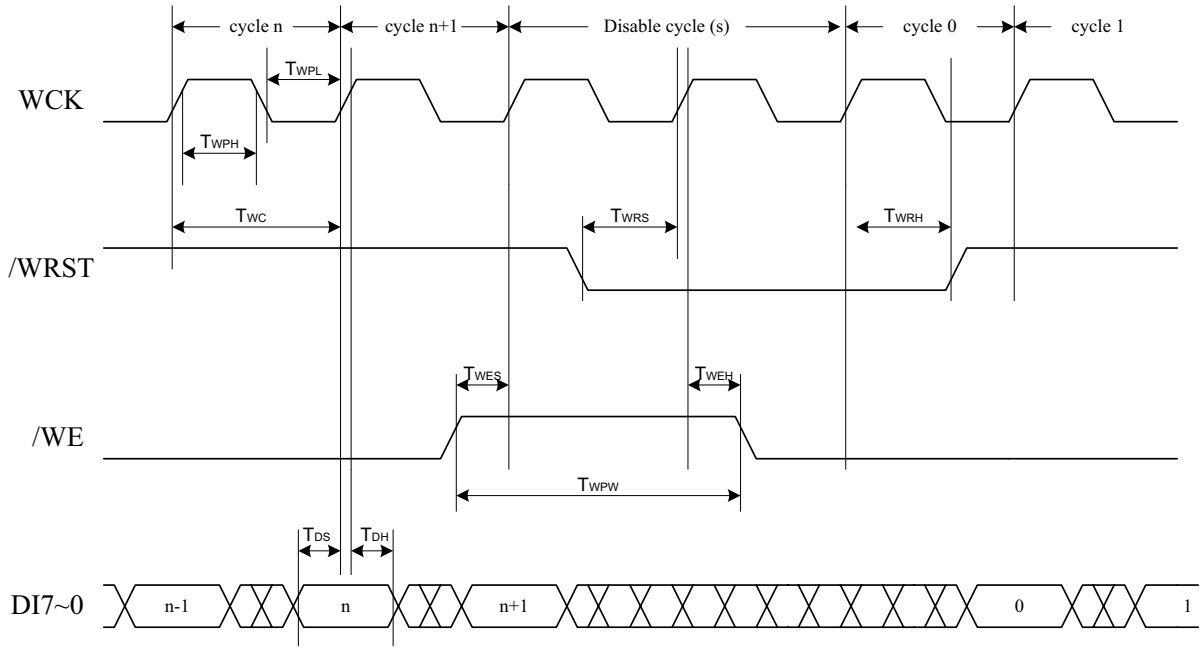
Read Cycle Timing (Output Enable)



Write Cycle Timing (Write Enable)



Read Cycle Timing (RE, RRST)



Write Cycle Timing (WE, WRST)

8 Functional Description

The I/O pin-outs and functions are described as follows:

DI7~DI0 Data Input: Data is input on the rising edge of the cycle of WCK when /WE is pulled low (enabled).

DO7~DO0 Data Output: Data output is synchronized with the RCK clock. Data is obtained at the rising edge of the RCK clock when /RE is pulled low. The access time is defined from the rising edge of the RCK cycle.

WCK Write Clock Input: The write data input is synchronized with this clock. Write data is input at the rising edge of the WCK cycle when /WE is pulled low (enabled). The internal write address pointer is incremented automatically with this clock input.

RCK Read Clock Input: The read data output is synchronized with this clock. Read data output at the rising edge of the RCK cycle when /OE is pulled low (enabled). The internal read address pointer is incremented with this clock input.

/WE Write Enable Input: /WE controls the enabling/disabling of the data input. When /WE is pulled low, input data is acquired at the rising edge of the WCK cycle. When /WE is pulled high, the memory does not accept data input. The write address pointer is stopped at the current position. /WE signal is fetched at the rising edge of the WCK cycle.

/RE Read Enable Input: /RE controls the operation of the data output. When /RE is pulled low, output data is provided at the rising edge of the RCK cycle and the internal read address is incremented automatically. /RE signal is fetched at the rising edge of the RCK cycle.

/OE Output Enable Input: /OE controls the enabling/disabling of the data output. When /OE is pulled low, output data is provided at the rising edge of the RCK cycle. When /OE is pulled high, data output is disabled and the output pins remain at high impedance status. /OE signal is fetched at the rising edge of RCK cycle.

/WRST Write Reset Input: This reset signal initializes the write address to 0, and is fetched at the rising edge of the WCK input cycle.

/RRST Write Reset Input: This reset signal initializes the read address to 0, and is fetched at the rising edge of the RCK input cycle.

TST Test Pin: For testing purpose only. It should be pulled low for normal applications.

DEC: Decoupling cap pin should be connected to the 3.3V power with 0.1μF bypass capacitor.

8.1 Operation

Initialization

Apply /WRST and /RRST 0.1ms after power on, then follow the following instructions for normal operation.

Reset Operation

The reset signal can be given at any time regardless of the /WE, /RE and /OE status, however, they still need to meet the setup time and hold time requirements with reference to the clock input. When the reset signal is provided during disabled cycles, the reset operation is not executed until cycles are enabled again. After WRST and RRST signals are pulled low, the data output and input start from address 0.

Write Operation

Data input DI7~DI0 is written into the write register at the WCK input when /WE is pulled low. The write data should meet the setup time and hold time requirements with reference to the WCK input cycle.

Write operation is prohibited when /WE is pulled high, and the write address pointer is stopped at the current position. The write address starts from there when the /WE is pulled low again. The /WE signal needs to meet the setup time and hold time requirements with reference to the WCK input cycle.

Read Operation

Data output DO7~DO0 is written into the read register at the RCK input when both /RE and /OE are pulled low. The output data is ready after T_{AC} (access time) from the rising edge of the RCK input cycle.

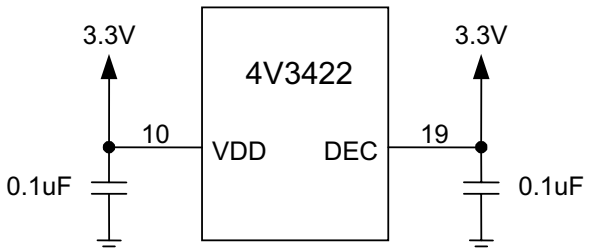
The read address pointer is stopped at the current position when /RE is pulled high, and starts there when /RE is pulled low again.

/OE needs to be pulled low for read operations. When /OE is pulled high, the data outputs will be at high impedance stage. The read address pointer still increases synchronously with RCK regardless of the /OE status. The /RE and /OE signals need to meet the setup time and hold time requirements with reference to the RCK input cycle.

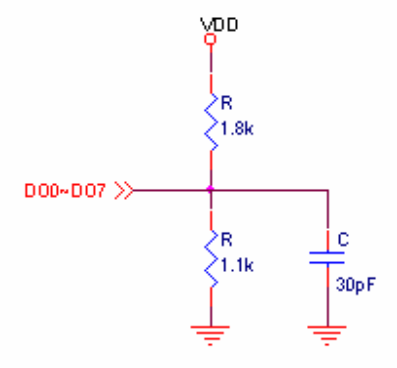
When the new data is read, the read address should be between 128 to 393,247 cycles after the write address, otherwise the output may not be new data.

8.2 Application Note

Power Supply

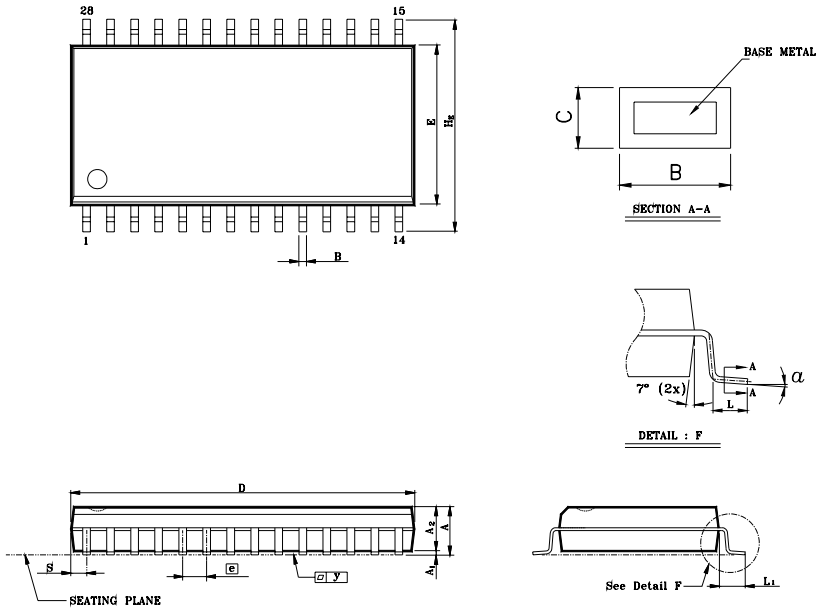


DO External Load



9.0 Mechanical Drawing

28 PIN PLASTIC SOP:



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.112	—	—	2.85
A_1	0.004	—	—	0.10	—	—
A_2	0.093	0.098	0.103	2.36	2.49	2.62
B	0.014	0.016	0.020	0.36	0.41	0.51
C	0.008	0.010	0.012	0.20	0.25	0.30
D	—	0.713	0.728	—	18.11	18.49
E	0.326	0.331	0.336	8.28	8.41	8.53
e	0.044	0.050	0.056	1.12	1.27	1.42
H	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L_1	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
α	0°	—	8°	0°	—	8°

Note:
1. Dimension D Max. & s include mold flash or tie bar burrs
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and determined at the mold parting line
4. Controlling dimension: Inch
5. General appearance spec should be based on final visual inspection spec.

REV NO	DESCRIPTION	DATE
B	1.Revise symbol letter per JEDEC definition. 2.Tighten tolerance of followine dimensions. Dimension / Was / Now C / 0.014" / 0.012" D / 0.733" / 0.728" α / 10° / 8°	Apr,07
B	1.Update form. 2.The effective decimal 0.xx instead of 0.xxx in the metric system.	Mar,22

TITLE: 28LD SOP (330 mil BODY) PACKAGE OUTLINE			
L/F MATERIAL: A194 F.H.		JEDEC CODE NO	MO-059
		ELAJ CODE NO	———
APPR.		DWG NO.	S028-SW2
R&D		REV NO.	C
Q.M		SCALE	
CHK.		DATE	June, 30, 98
DEN.		SHT NO.	1/1
AVERLOGIC TECHNOLOGIES, INC.			

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