PCF8563

Real-time clock/calendar

1. General description

The PCF8563 is a CMOS real-time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage-low detector are also provided. All address and data are transferred serially via a two-line bidirectional I^2C-bus. Maximum bus speed is 400 kbits/s. The built-in word address register is incremented automatically after each written or read data byte.

2. Features

- Provides year, month, day, weekday, hours, minutes and seconds based on 32.768 kHz quartz crystal
- Century flag
- Wide operating supply voltage range: 1.0 to 5.5 V
- Low back-up current; typical 0.25 µA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 400 kHz two-wire I^2C-bus interface (at V_{DD} = 1.8 to 5.5 V)
- Programmable clock output for peripheral devices: 32.768 kHz, 1024 Hz, 32 Hz and 1 Hz
- Alarm and timer functions
- Voltage-low detector
- Integrated oscillator capacitor
- Internal power-on reset
- I^2C-bus slave address: read A3H; write A2H
- Open drain interrupt pin.

3. Applications

- Mobile telephones
- Portable instruments
- Fax machines
- Battery powered products.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage operating mode	I^2C-bus inactive; T_{amb} = 25 °C	1.0	5.5	V
		I^2C-bus active; f_{SCL} = 400 kHz; T_{amb} = −40 to +85 °C	1.8	5.5	V
I_{DD}	supply current; timer and CLKOUT disabled	f_{SCL} = 400 kHz	-	800	µA
		f_{SCL} = 100 kHz	-	200	µA
		f_{SCL} = 0 Hz; T_{amb} = 25 °C			
		V_{DD} = 5 V	-	550	nA
		V_{DD} = 2 V	-	450	nA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PCF8563P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8563T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCF8563TS	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3.0 mm	SOT505-1

6. Block diagram

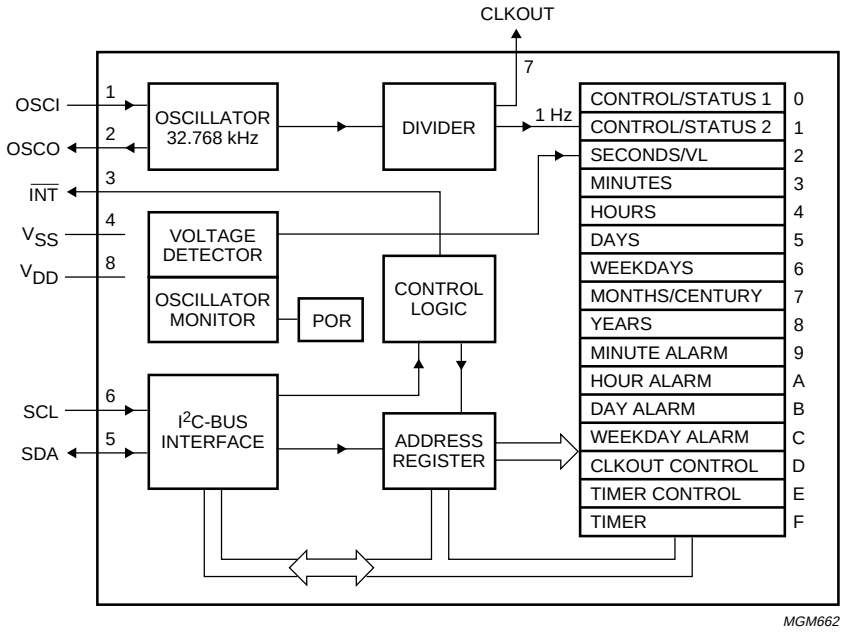


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

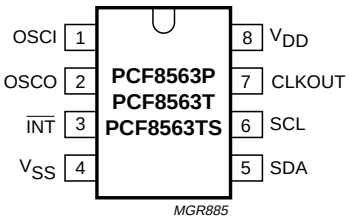


Fig 2. Pin configuration.

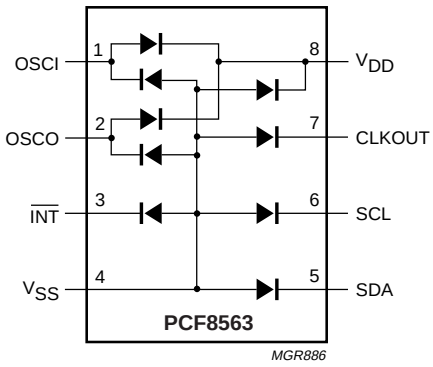


Fig 3. Device diode protection diagram.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
$\overline{INT}$	3	interrupt output (open-drain; active LOW)
V_{SS}	4	ground
SDA	5	serial data I/O
SCL	6	serial clock input
CLKOUT	7	clock output (open-drain)
V_{DD}	8	positive supply

8. Functional description

The PCF8563 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with an integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I^2C-bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00H and 01H) are used as control and/or status registers. The memory addresses 02H through 08H are used as counters for the clock function (seconds up to year counters). Address locations 09H through 0CH contain alarm registers which define the conditions for an alarm. Address 0DH controls the CLKOUT output frequency. 0EH and 0FH are the timer control and timer registers, respectively.

The Seconds, Minutes, Hours, Days, Months, Years as well as the Minute alarm, Hour alarm and Day alarm registers are all coded in BCD format. The Weekdays and Weekday alarm register are not coded in BCD format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

8.1 Alarm function modes

By clearing the MSB (bit AE = Alarm Enable) of one or more of the alarm registers, the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the alarm flag, AF (bit 3 of Control/Status 2 register). The asserted AF can be used to generate an interrupt ($\overline{INT}$). Bit AF can only be cleared by software.

8.2 Timer

The 8-bit countdown timer (address 0FH) is controlled by the Timer Control register (address 0EH; see Table 25). The Timer Control register selects one of 4 source clock frequencies for the timer (4096, 64, 1, or $1/60$ Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF (see Table 7). The timer flag TF can only be cleared by software. The asserted timer flag TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. TI/TP (see Table 7) is used to control this mode selection. When reading the timer, the current countdown value is returned.

8.3 CLKOUT output

A programmable square wave is available at the CLKOUT pin. Operation is controlled by the CLKOUT frequency register (address 0DH; see Table 23). Frequencies of 32.768 kHz (default), 1024, 32 and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is an open-drain output and enabled at power-on. If disabled it becomes high-impedance.

8.4 Reset

The PCF8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C-bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE which are set to logic 1.

8.5 Voltage-low detector and clock monitor

The PCF8563 has an on-chip voltage-low detector. When V_{DD} drops below V_{low} the VL bit (Voltage Low, bit 7 in the Seconds register) is set to indicate that reliable clock/calendar information is no longer guaranteed. The VL flag can only be cleared by software.

The VL bit is intended to detect the situation when V_{DD} is decreasing slowly for example under battery operation. Should V_{DD} reach V_{low} before power is re-asserted then the VL bit will be set. This will indicate that the time may be corrupted.

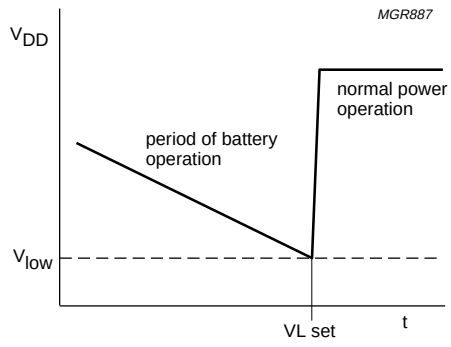


Fig 4. Voltage-low detection.

8.6 Register organization

Table 4: Registers overview

Bit positions labelled as '–' are not implemented; those labelled with '0' should always be written with logic 0.

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	Control/Status 1	TEST1	0	STOP	0	TESTC	0	0	0
01H	Control/Status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
0DH	CLKOUT frequency	FE	–	–	–	–	–	FD1	FD0
0EH	Timer control	TE	–	–	–	–	–	TD1	TD0
0FH	Timer countdown value	<timer countdown value>							

Table 5: BCD formatted registers overview

Bit positions labelled as '–' are not implemented.

Address	Register name	BCD format tens nibble				BCD format units nibble			
		Bit 7 2^3	Bit 6 2^2	Bit 5 2^1	Bit 4 2^0	Bit 3 2^3	Bit 2 2^2	Bit 1 2^1	Bit 0 2^0
02H	Seconds	VL	<seconds 00 to 59 coded in BCD>						
03H	Minutes	–	<minutes 00 to 59 coded in BCD>						
04H	Hours	–	–	<hours 00 to 23 coded in BCD>					
05H	Days	–	–	<days 01 to 31 coded in BCD>					
06H	Weekdays	–	–	–	–	–	<weekdays 0 to 6 > [1]		
07H	Months/Century	C	–	–	<months 01 to 12 coded in BCD>				
08H	Years	<years 00 to 99 coded in BCD>							
09H	Minute alarm	AE	<minute alarm 00 to 59 coded in BCD>						
0AH	Hour alarm	AE	–	<hour alarm 00 to 23 coded in BCD>					
0BH	Day alarm	AE	–	<day alarm 01 to 31 coded in BCD>					
0CH	Weekday alarm	AE	–	–	–	–	<weekday alarm 0 to 6 > [1]		

[1] Not coded in BCD.

8.6.1 Control/Status 1 register

Table 6: Control/Status 1 register bits description (address 00H)

Bit	Symbol	Description
7	TEST1	TEST1 = 0; normal mode. TEST1 = 1; EXT_CLK test mode; see Section 8.7.
5	STOP	STOP = 0; RTC source clock runs. STOP = 1; all RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available).
3	TESTC	TESTC = 0; power-on reset override facility is disabled (set to logic 0 for normal operation). TESTC = 1; power-on reset override is enabled.
6, 4, 2 to 0	0	By default set to logic 0.

8.6.2 Control/Status 2 register

Table 7: Description of Control/Status 2 register bits description (address 01H)

Bit	Symbol	Description
7 to 5	0	By default set to logic 0.
4	TI/TP	TI/TP = 0: INT is active when TF is active (subject to the status of TIE).
		TI/TP = 1: INT pulses active according to Table 8 (subject to the status of TIE). Note that if AF and AIE are active then INT will be permanently active.
3	AF	When an alarm occurs, AF is set to logic 1. Similarly, at the end of a timer countdown, TF is set to logic 1. These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access. See Table 9 for the value descriptions of bits AF and TF.
2	TF	
1	AIE	Bits AIE and TIE activate or deactivate the generation of an interrupt when AF or TF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.
0	TIE	AIE = 0: alarm interrupt disabled; AIE = 1: alarm interrupt enabled.
		TIE = 0: timer interrupt disabled; TIE = 1: timer interrupt enabled.

Table 8: $\overline{INT}$ operation (bit TI/TP = 1)

Source clock (Hz)	$\overline{INT}$ [1] period (s)	
	n [2] = 1	n > 1
4 096	$1/8192$	$1/4096$
64	$1/128$	$1/64$
1	$1/64$	$1/64$
$1/60$	$1/64$	$1/64$

[1] TF and $\overline{INT}$ become active simultaneously.

[2] n = loaded countdown timer value. Timer stopped when n = 0.

Table 9: Value descriptions for bits AF and TF

R/W	Bit: AF		Bit: TF	
	Value	Description	Value	Description
Read	0	alarm flag inactive	0	timer flag inactive
	1	alarm flag active	1	timer flag active
Write	0	alarm flag is cleared	0	timer flag is cleared
	1	alarm flag remains unchanged	1	timer flag remains unchanged

8.6.3 Seconds, Minutes and Hours registers

Table 10: Seconds/VL register bits description (address 02H)

Bit	Symbol	Description
7	VL	VL = 0: reliable clock/calendar information is guaranteed; VL = 1: reliable clock/calendar information is no longer guaranteed.
6 to 0	<seconds>	These bits represent the current seconds value coded in BCD format; value = 00 to 59. Example: <seconds> = 101 1001, represents the value 59 s.

Table 11: Minutes register bits description (address 03H)

Bit	Symbol	Description
7	–	not implemented
6 to 0	<minutes>	These bits represent the current minutes value coded in BCD format; value = 00 to 59.

Table 12: Hours register bits description (address 04H)

Bit	Symbol	Description
7 to 6	–	not implemented
5 to 0	<hours>	These bits represent the current hours value coded in BCD format; value = 00 to 23.

8.6.4 Days, Weekdays, Months/Century and Years registers

Table 13: Days register bits description (address 05H)

Bit	Symbol	Description
7 to 6	–	not implemented
5 to 0	<days>	These bits represent the current day value coded in BCD format; value = 01 to 31. The PCF8563 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year ‘00’.

Table 14: Weekdays register bits description (address 06H)

Bit	Symbol	Description
7 to 3	–	not implemented
2 to 0	<weekdays>	These bits represent the current weekday value 0 to 6; see Table 15. These bits may be re-assigned by the user.

Table 15: Weekday assignments

Day	Bit 2	Bit 1	Bit 0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

Table 16: Months/Century register bits description (address 07H)

Bit	Symbol	Description
7	C	Century bit. C = 0; indicates the century is 20xx. C = 1; indicates the century is 19xx. 'xx' indicates the value held in the Years register; see Table 18. This bit is toggled when the Years register overflows from 99 to 00. These bits may be re-assigned by the user.
6 to 5	–	not implemented
4 to 0	<months>	These bits represents the current month value coded in BCD format; value = 01 to 12; see Table 17.

Table 17: Month assignments

Month	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

Table 18: Years register bits description (address 08H)

Bit	Symbol	Description
7 to 0	<years>	This register represents the current year value coded in BCD format; value = 00 to 99.

8.6.5 Alarm registers

When one or more of the alarm registers are loaded with a valid minute, hour, day or weekday and its corresponding AE (Alarm Enable) bit is a logic 0, then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the bit AF (Alarm Flag) is set.

AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE bit set at logic 1 will be ignored.

Table 19: Minute alarm register bits description (address 09H)

Bit	Symbol	Description
7	AE	AE = 0; minute alarm is enabled. AE = 1; minute alarm is disabled.
6 to 0	<minute alarm>	These bits represents the minute alarm information coded in BCD format; value = 00 to 59.

Table 20: Hour alarm register bits description (address 0AH)

Bit	Symbol	Description
7	AE	AE = 0; hour alarm is enabled. AE = 1; hour alarm is disabled.
6 to 0	<hour alarm>	These bits represents the hour alarm information coded in BCD format; value = 00 to 23.

Table 21: Day alarm register bits description (address 0BH)

Bit	Symbol	Description
7	AE	AE = 0; day alarm is enabled. AE = 1; day alarm is disabled.
6 to 0	<day alarm>	These bits represents the day alarm information coded in BCD format; value = 01 to 31.

Table 22: Weekday alarm register bits description (address 0CH)

Bit	Symbol	Description
7	AE	AE = 0; weekday alarm is enabled. AE = 1; weekday alarm is disabled.
6 to 0	<weekday alarm>	These bits represents the weekday alarm information value 0 to 6.

8.6.6 CLKOUT frequency register

Table 23: CLKOUT frequency register bits description (address 0DH)

Bit	Symbol	Description
7	FE	FE = 0; the CLKOUT output is inhibited and the CLKOUT output is set to high-impedance. FE = 1; the CLKOUT output is activated.
6 to 2	–	not implemented
1	FD1	These bits control the frequency output (f_{CLKOUT}) on the CLKOUT pin; see Table 24.
0	FD0	

Table 24: CLKOUT frequency selection

FD1	FD0	f_{CLKOUT}
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

8.6.7 Countdown timer registers

The Timer register is an 8-bit binary countdown timer. It is enabled and disabled via the Timer control register bit TE. The source clock for the timer is also selected by the Timer control register. Other timer properties, e.g. interrupt generation, are controlled via the Control/status 2 register. For accurate read back of the countdown value, the I^2C-bus clock SCL must be operating at a frequency of at least twice the selected timer clock.

Table 25: Timer control register bits description (address 0EH)

Bit	Symbol	Description
7	TE	TE = 0; timer is disabled. TE = 1; timer is enabled.
6 to 2	–	not implemented
1	TD1	Timer source clock frequency selection bits. These bits determine the source clock for the countdown timer, see Table 26. When not in use, TD1 and TD0 should be set to ‘11’ ($1/60$ Hz) for power saving.
0	TD0	

Table 26: Timer source clock frequency selection

TD1	TD0	Timer source clock frequency (Hz)
0	0	4096
0	1	64
1	0	1
1	1	$1/60$

Table 27: Timer countdown value register bits description (address 0FH)

Bit	Symbol	Description
7 to 0	<timer countdown value>	This register holds the loaded countdown value ‘n’. $\text{Countdown period} = \frac{n}{\text{Source clock frequency}}$

8.7 EXT_CLK test mode

A test mode is available which allows for on-board testing. In this mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit TEST1 in the Control/Status1 register. The CLKOUT pin then becomes an input. The test mode replaces the internal 64 Hz signal with the signal that is applied to the CLKOUT pin. Every 64 positive edges applied to CLKOUT will then generate an increment of one second.

The signal applied to the CLKOUT pin should have a minimum pulse width of 300 ns and a minimum period of 1000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using the STOP bit. When the STOP bit is set, the pre-scaler is reset to 0. STOP must be cleared before the pre-scaler can operate again. From a STOP condition, the first 1 s increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 s increment.

Remark: Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

8.7.1 Operation example

1. Enter the EXT_CLK test mode; set bit 7 of Control/Status 1 register (TEST = 1)
2. Set bit 5 of Control/Status 1 register (STOP = 1)
3. Clear bit 5 of Control/Status 1 register (STOP = 0)
4. Set time registers (Seconds, Minutes, Hours, Days, Weekdays, Months/Century and Years) to desired value
5. Apply 32 clock pulses to CLKOUT
6. Read time registers to see the first change
7. Apply 64 clock pulses to CLKOUT
8. Read time registers to see the second change.

Repeat steps 7 and 8 for additional increments.

8.8 Power-On Reset (POR) override mode

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the I^2C-bus pins, SDA and SCL, be toggled in a specific order as shown in Figure 5. All timing values are required minimum.

Once the override mode has been entered, the chip immediately stops being reset and normal operation starts i.e. entry into the EXT_CLK test mode via I^2C-bus access. The override mode is cleared by writing a logic 0 to bit TESTC. Re-entry into the override mode is only possible after TESTC is set to logic 1. Setting TESTC to logic 0 during normal operation has no effect except to prevent entry into the POR override mode.

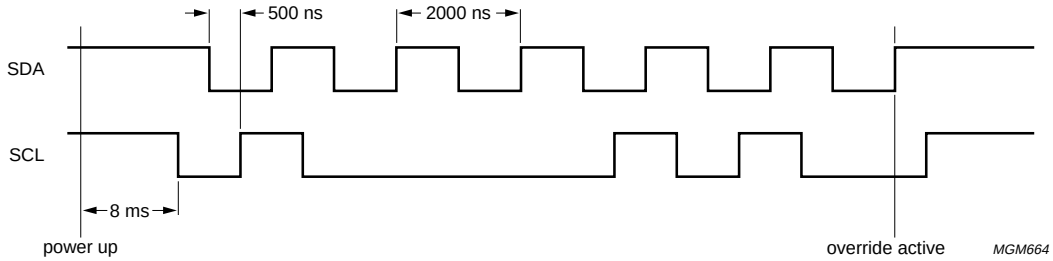


Fig 5. POR override sequence.

8.9 Serial interface

The serial interface of the PCF8563 is the I²C-bus. A detailed description of the I²C-bus specification, including applications, is given in the brochure: *The I²C-bus and how to use it*, order no. 9398 393 40011 or *I²C Peripherals Data Handbook IC12.*

8.9.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

The I²C-bus system configuration is shown in Figure 6. A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

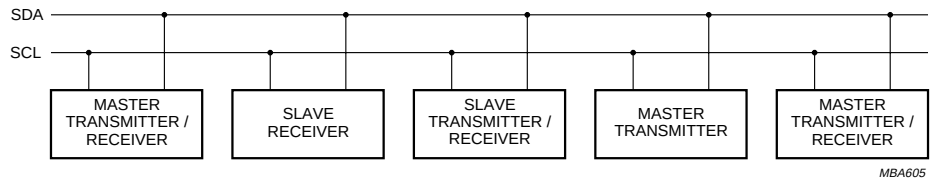


Fig 6. I²C-bus system configuration.

8.9.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P); see Figure 7.

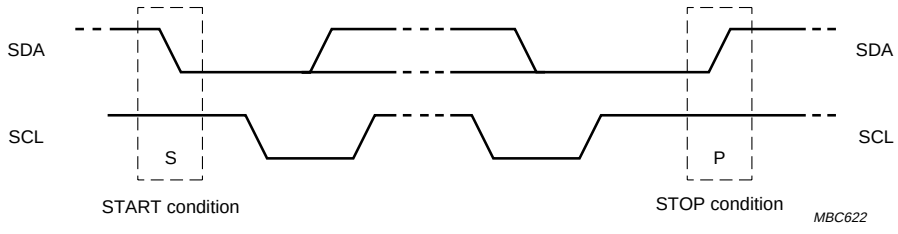


Fig 7. START and STOP conditions on the I²C-bus.

8.9.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal; see Figure 8.

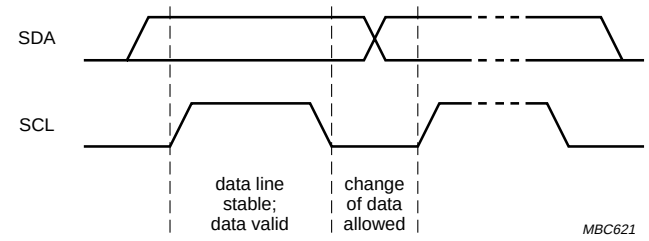


Fig 8. Bit transfer on the I²C-bus.

8.9.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

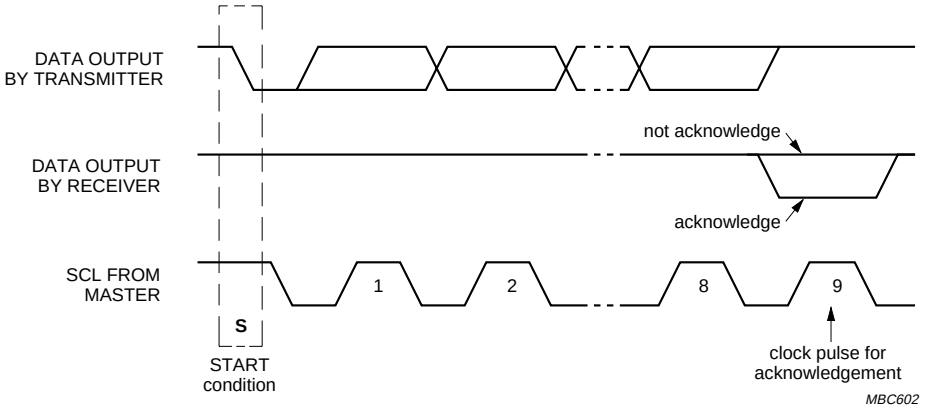


Fig 9. Acknowledge on the I²C-bus.

8.9.5 I²C-bus protocol

Addressing: Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The PCF8563 slave address is shown in Figure 10.

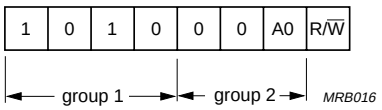


Fig 10. Slave address.

Clock/calendar read/write cycles: The I²C-bus configuration for the different PCF8563 read and write cycles are shown in Figure 11, 12 and 13. The word address is a four bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

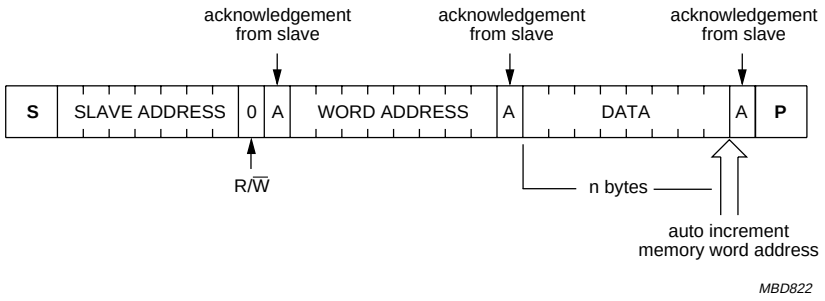


Fig 11. Master transmits to slave receiver (write mode).

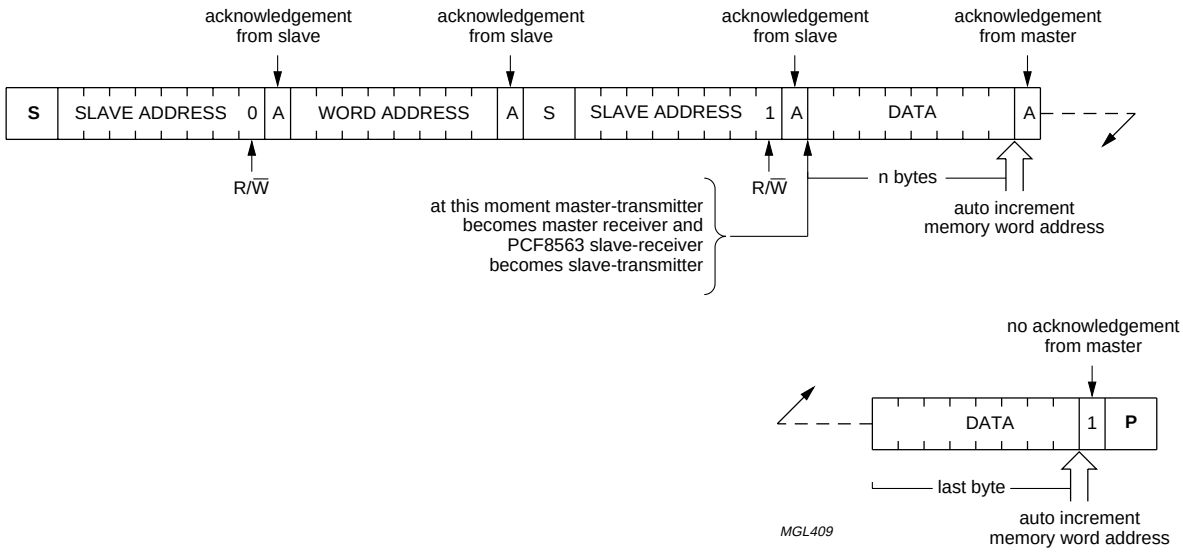


Fig 12. Master reads after setting word address (write word address; read data).

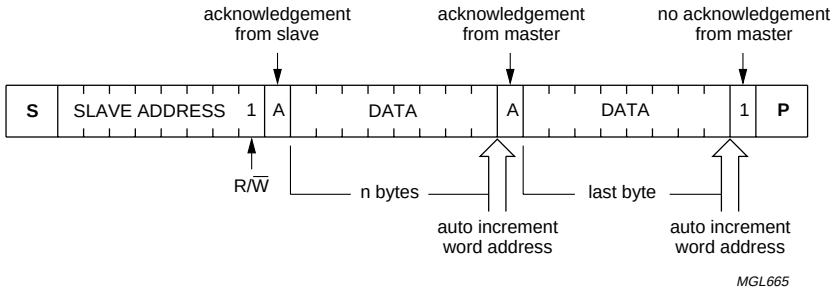


Fig 13. Master reads slave immediately after first byte (read mode).

9. Limiting values

Table 28: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.5	V
I_{DD}	supply current		–50	+50	mA
V_I	input voltage on inputs SCL and SDA		–0.5	6.5	V
	input voltage on input OSCI		–0.5	V_{DD} + 0.5	V
V_O	output voltage on outputs CLKOUT and $\overline{INT}$		–0.5	6.5	V
I_I	DC input current at any input		–10	+10	mA
I_O	DC output current at any output		–10	+10	mA
P_{tot}	total power dissipation		–	300	mW
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C

10. Static characteristics

Table 29: Static characteristics

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C; f_{OSC} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage	I^2C-bus inactive; T_{amb} = 25 °C		1.0 [1]	–	5.5	V
		I^2C-bus active; f_{SCL} = 400 kHz		1.8 [1]	–	5.5	V
	supply voltage for reliable clock/calendar information	T_{amb} = 25 °C		V_{low}	–	5.5	V
I_{DD1}	supply current; CLKOUT disabled (FE = 0)	f_{SCL} = 400 kHz	[2]	–	–	800	µA
		f_{SCL} = 100 kHz		–	–	200	µA
		f_{SCL} = 0 Hz; T_{amb} = 25 °C	[2]				
		V_{DD} = 5 V		–	275	550	nA
		V_{DD} = 3 V		–	250	500	nA
		V_{DD} = 2 V		–	225	450	nA
		f_{SCL} = 0 Hz	[2]				
		V_{DD} = 5 V		–	500	750	nA
		V_{DD} = 3 V		–	400	650	nA
		V_{DD} = 2 V		–	400	600	nA
I_{DD2}	supply current; CLKOUT enabled (f_{CLKOUT} = 32 kHz; FE = 1)	f_{SCL} = 0 Hz; T_{amb} = 25 °C	[2]				
		V_{DD} = 5 V		–	825	1600	nA
		V_{DD} = 3 V		–	550	1000	nA
		V_{DD} = 2 V		–	425	800	nA
		f_{SCL} = 0 Hz	[2]				
		V_{DD} = 5 V		–	950	1700	nA
		V_{DD} = 3 V		–	650	1100	nA
		V_{DD} = 2 V		–	500	900	nA
Inputs							
V_{IL}	LOW-level input voltage			V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}		−1	–	+1	µA
C_i	input capacitance		[3]	–	–	7	pF
Outputs							
$I_{OL(SDA)}$	LOW-level output current; pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V		−3	–	–	mA
$I_{OL(\overline{INT})}$	LOW-level output current; pin $\overline{INT}$			−1	–	–	mA
$I_{OL(CLKOUT)}$	LOW-level output current; pin CLKOUT			−1	–	–	mA

Table 29: Static characteristics *...continued*

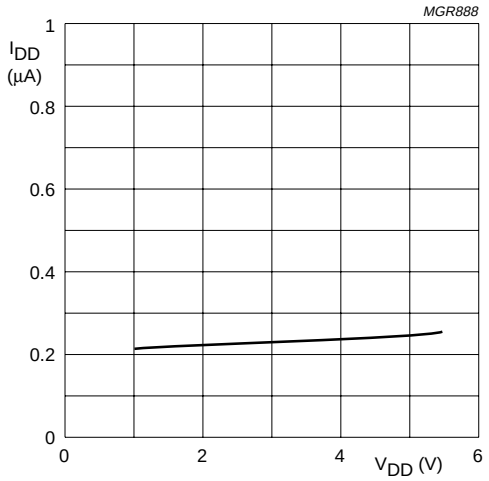
V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C; f_{OSC} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OH(CLKOUT)}$	HIGH-level output current; pin CLKOUT	V_{OH} = 4.6 V; V_{DD} = 5 V	1	–	–	mA
I_{LO}	output leakage current	V_O = V_{DD} or V_{SS}	−1	–	+1	µA
Voltage detector						
V_{low}	voltage-low detection level	T_{amb} = 25 °C	–	0.9	1.0	V

[1] For reliable oscillator start-up at power-up: $V_{DD(min)power\text{-}up}$ = $V_{DD(min)}$ + 0.3 V.

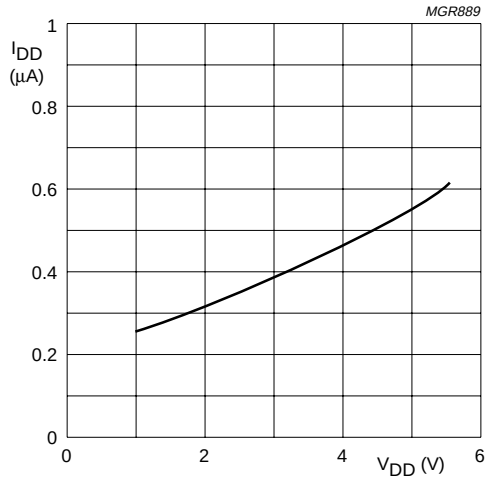
[2] Timer source clock = $\frac{1}{60}$ Hz; SCL and SDA = V_{DD}.

[3] Tested on sample basis.



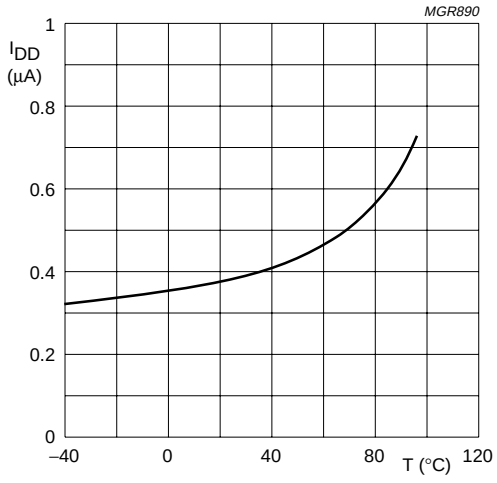
T_{amb} = 25 °C; Timer = 1 minute.

Fig 14. I_{DD} as a function of V_{DD}; CLKOUT disabled.



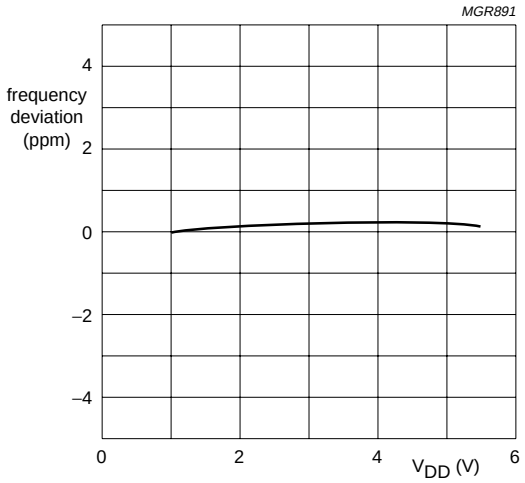
T_{amb} = 25 °C; Timer = 1 minute.

Fig 15. I_{DD} as a function of V_{DD}; CLKOUT = 32 kHz.



V_{DD} = 3 V; Timer = 1 minute.

Fig 16. I_{DD} as a function of T_{amb}; CLKOUT = 32 kHz.



T_{amb} = 25 °C; normalized to V_{DD} = 3 V.

Fig 17. Frequency deviation as function of V_{DD}.

11. Dynamic characteristics

Table 30: Dynamic characteristics

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_s = 40 kΩ; C_L = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
$C_{L(integrated)}$	integrated load capacitance		15	25	35	pF
$\Delta f_{OSC}/f_{OSC}$	oscillator stability	ΔV_{DD} = 200 mV; T_{amb} = 25 °C	–	2×10^{-7}	–	
Quartz crystal parameters (f_{OSC} = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
CLKOUT output						
δ_{CLKOUT}	CLKOUT duty factor	[1]	–	50	–	%
I^2C-bus timing characteristics [2]						
f_{SCL}	SCL clock frequency	[3]	–	–	400	kHz
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
t_r	SCL and SDA rise time		–	–	0.3	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_b	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

[1] Unspecified for f_{CLKOUT} = 32.768 kHz.

[2] All timing values are valid within the operating supply voltage range at T_{amb} and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[3] I^2C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

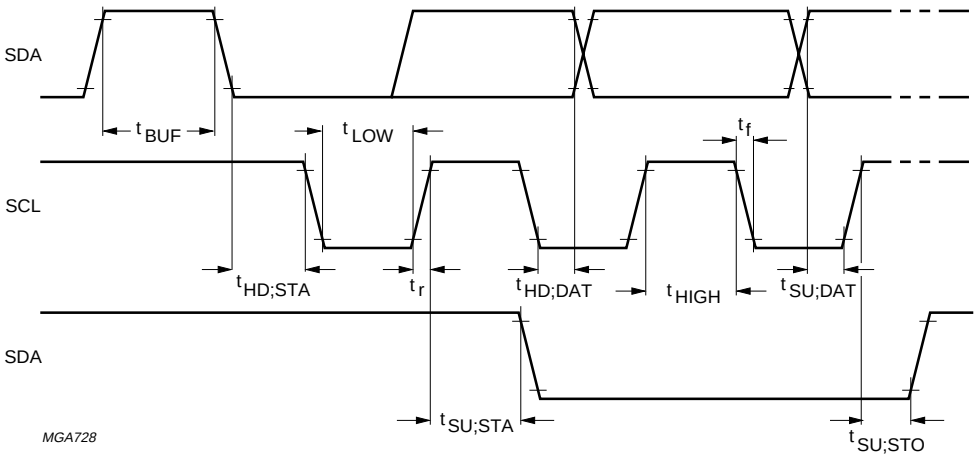


Fig 18. I²C-bus timing waveforms.

12. Application information

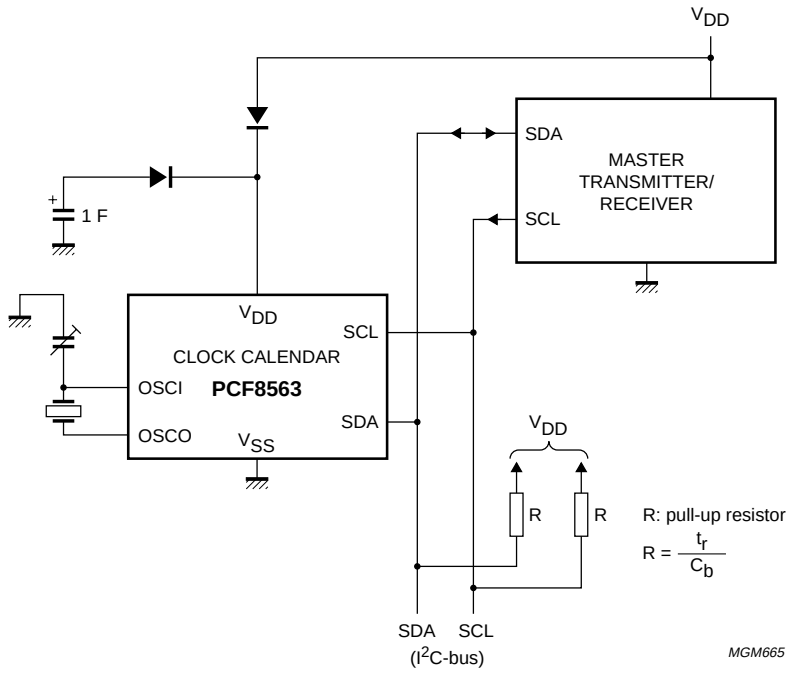


Fig 19. Application diagram.

12.1 Quartz crystal frequency adjustment

Method 1: Fixed OSCI capacitor — By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at the CLKOUT pin. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$).

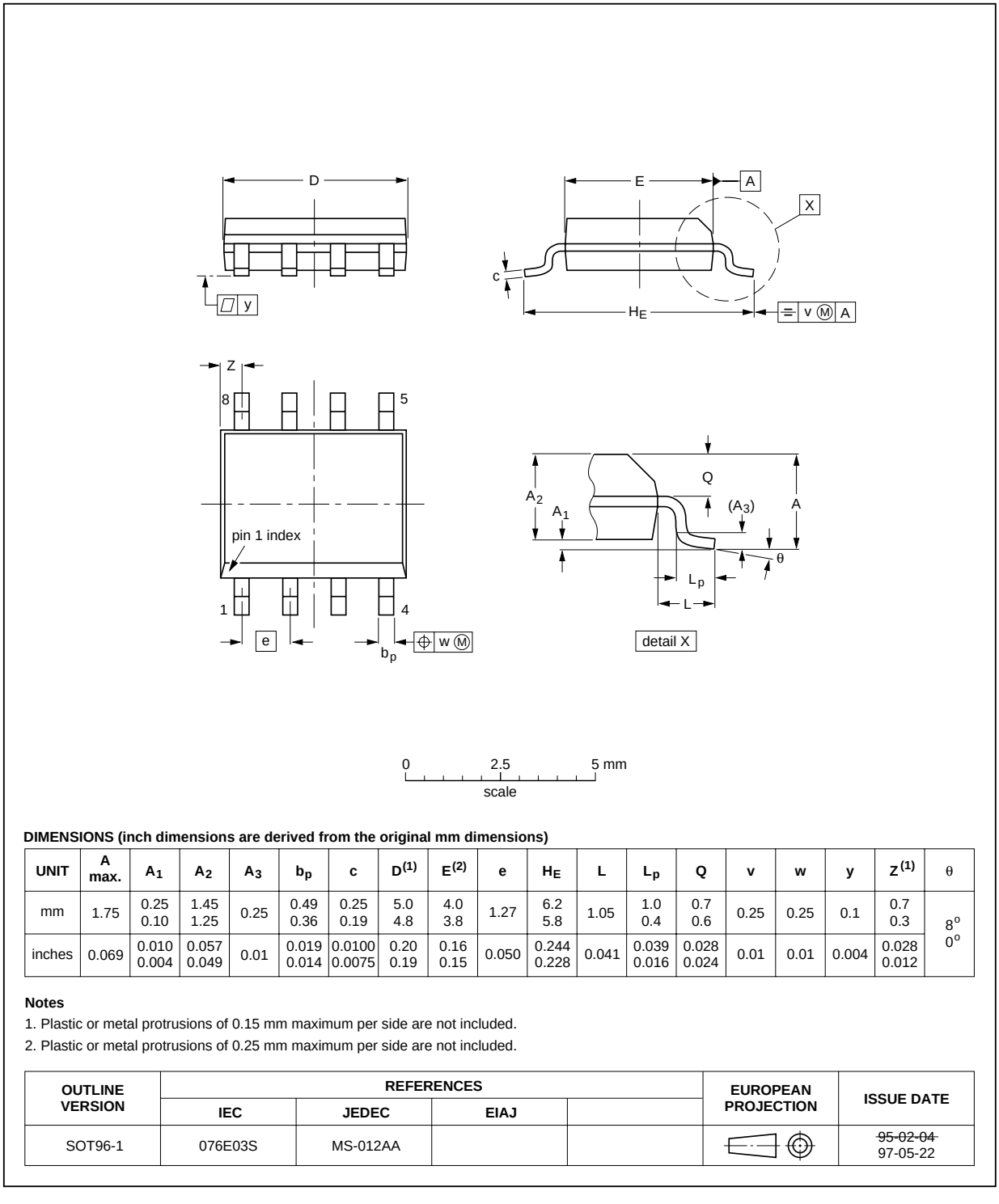
Average deviations of ±5 minutes per year can be easily achieved.

Method 2: OSCI trimmer — The oscillator is tuned to the required accuracy by adjusting a trimmer capacitor on pin OSCI and measuring the 32.768 kHz signal available after power-on at the CLKOUT pin.

Method 3: OSCO output — Direct output measurement on pin OSCO (accounting for test probe capacitance).

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

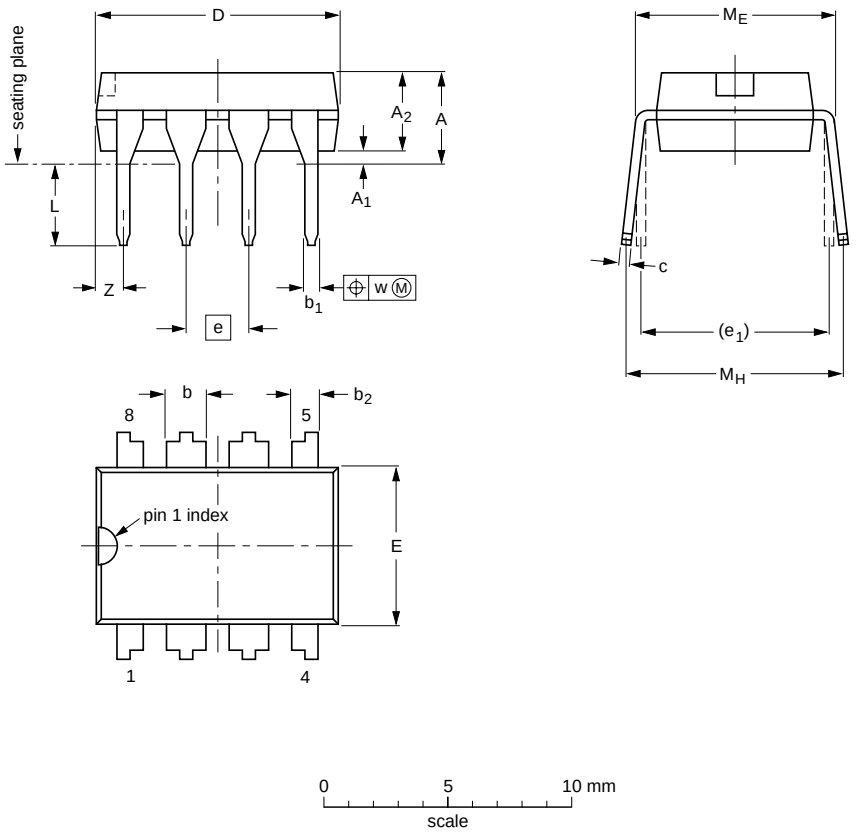
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Fig 20. SOT96-1.

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

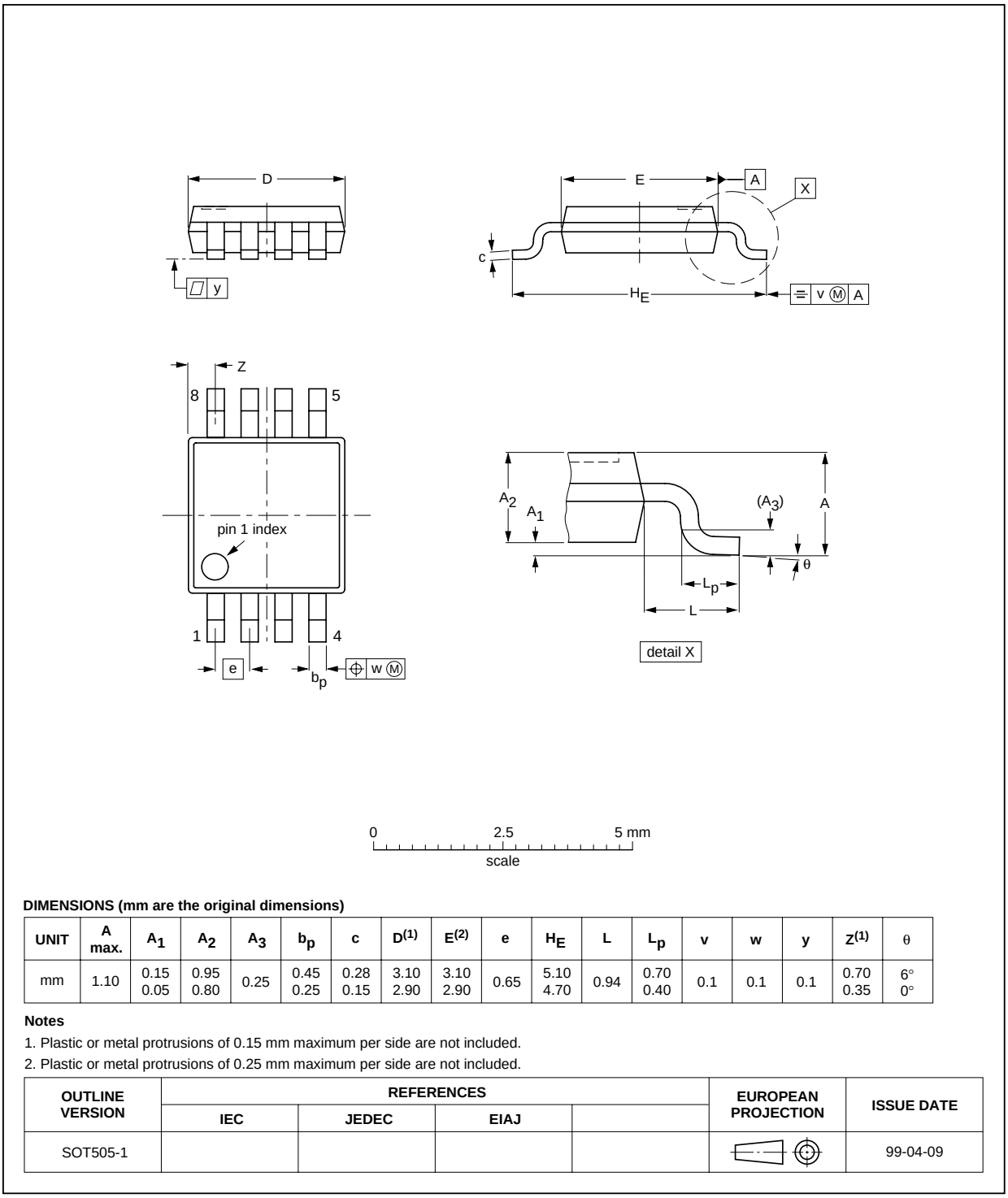
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

Fig 21. SOT97-1.

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

Fig 22. SOT505-1.