5.5”FHD Pixel Eye Solution

LCD MODULE

Preliminary

SPECIFICATION

Model:	TPM0551002P
TDI P/N.:	340S055004
Date:	2014.10.10
Version:	0.0

For Customer's Acceptance

Approved by	comment

Taiwan Display Inc.
JDI Japan Display Inc. Group

Record of Revision

Version	Revise Date	Page	Content	Owner
0.0	2014.10.10	32	Initial Release Draft Version	Rainbow Wang

Contents

1. General Specifications

1.1. Description

Product consists of a 5.46" diagonal 1080xRGBx1920 PE LTPS display with Drive IC R69338 and TP IC S3351. The driver IC is R69338. A backlight incorporating with 12 pcs white LED's is included to illuminate the display.

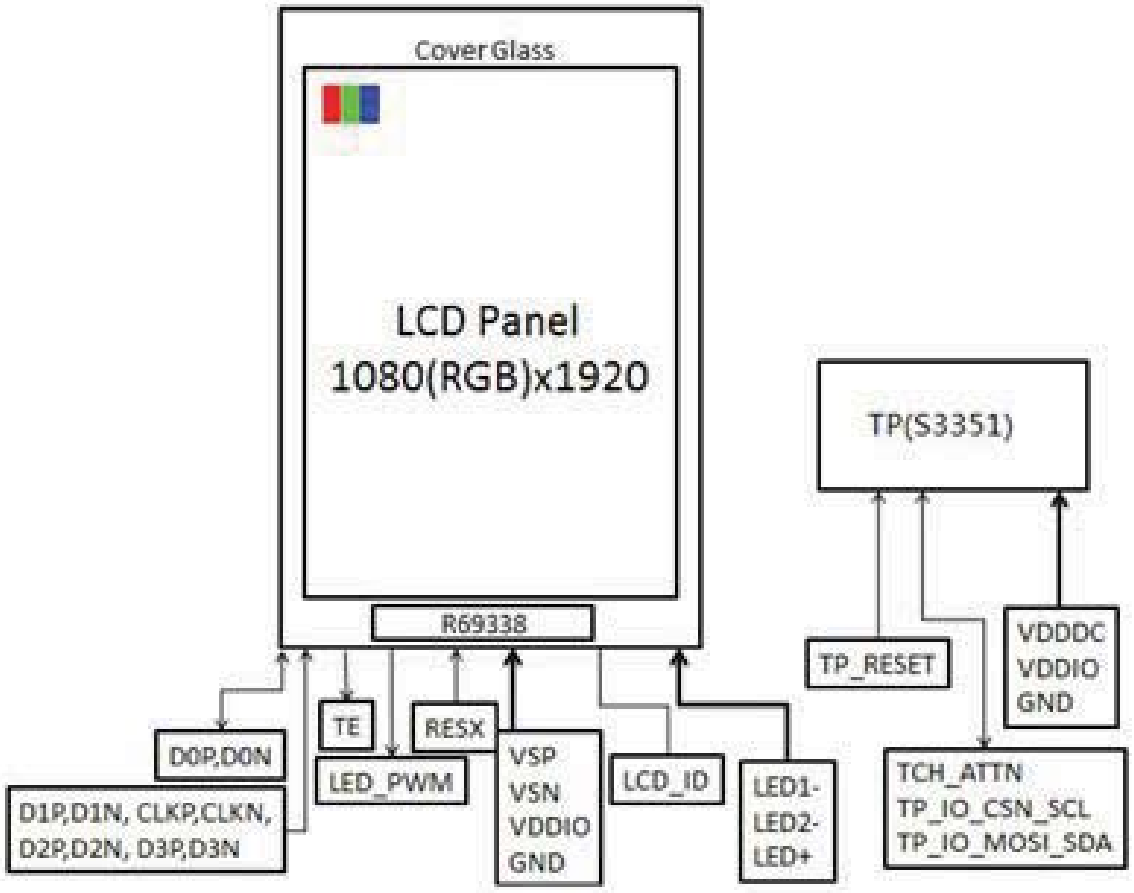
1.2. GENERAL SPECIFICATIONS

No.	Item	Specification	Unit	Remark
1	LCD Size	5.46	inch	-
2	Panel Type	Trans missive Type	-	-
3	Resolution	1080xRGB x1920	pixel	-
4	Display Mode	LTPS; Normally Black Mode, In-Plane Switching Mode, Pixel Eyes.	-	-
5	Display Number of Colors	16M (24bit)	-	-
6	Viewing Direction	-	-	Note 1
7	Viewing Angle	80/80/80/80		-
8	Contrast Ratio	1000(Typ)	-	-
9	Luminance	450 cd/m2 (Typ),400cd/m2(min) (Active Area Center)	cd/m2	-
10	Module Size	70.44(W) x 128.11(H) x 1.36(D)	mm	Note 1
11	Panel Active Area	68.04(W) × 120.96(H)	mm	Note 1
12	Pixel Pitch	63.0 x 63.0	um	-
13	Weight	TBD	g	Note 2
14	Driver IC	R69338	-	-
15	TP Driver IC	S3351		
16	Light Source	12 LEDs		-
17	Interface	MIPI 4Lane 39pin	-	-
18	Operating Temperature	-20℃~60℃	℃	-
19	Storage Temperature	-30℃~70℃	℃	-
20	Touch Feature	Multi-touch		

Note 1: Refer to mechanical drawing.

Note 2: Exclude protect sheet.

2. Block Diagram



3. Pin Assignment

3.1. Pin assignment for LCM

Recommend connector type: FH26-39S-0.3SHW(05), supplier: Hirose

Pin No.	Pin assignment	I/O	Description	Remark
1	TCH_ATTN/TP_INT	I/O	Attention Line	
2	TP_IO_CSN_SCL	I/O	TP I2C Clock	
3	TP_IO_MOSI_SDA	I/O	TP I2C Data	
4	GND	Power	Ground	
5	GND	Power	Ground	
6	TP_RESET	I	TP reset signal	
7	NC	-	No Connection	
8	NC	-	No Connection	
9	NC	-	No Connection	
10	NC	-	No Connection	
11	NC	-	No Connection	
12	VDDIO	Power	Digital Power Supply Voltage for LCD and TP	
13	VDDDC	Power	Analog Power Supply Voltage for TP	
14	AVDD/VSP	Power	Analog Power Supply Voltage for LCD	
15	AVEE/VSN	Power	Analog Power Supply Voltage for LCD	
16	RESX	I	LCD Reset Signal	
17	TE	O	TE signal output	
18	NC	-	No Connection	
19	LCD_ID	I	LCD ID Pin (connect 100Kohm resistor to GND in LCM)	GND
20	GND	Power	Ground	
21	D2P	I	MIPI Data2 Positive Signal	
22	D2N	I	MIPI Data2 Negtive Signal	
23	GND	Power	Ground	
24	D1P	I	MIPI Data1 Positive Signal	
25	D1N	I	MIPI Data1 Negative Signal	
26	GND	Power	Ground	
27	CLKP	I	MIPI Clock Positive Signal	
28	CLKN	I	MIPI Clock Negative Signal	
29	GND	Power	Ground	
30	D0P	I	MIPI Data0 Positive Signal	
31	D0N	I	MIPI Data0 Negative Signal	
32	GND	Power	Ground	
33	D3P	I	MIPI Data3 Positive Signal	
34	D3N	I	MIPI Data3 Negative Signal	

Pin No.	Pin assignment	I/O	Description	Remark
35	GND	Power	Ground	
36	LED_PWM	O	PWM output	
37	LED1-	Power	LED Power Supply Cathode1	
38	LED2-	Power	LED Power Supply Cathode2	
39	LED+	Power	LED Power Supply Anode	

4. Electrical Specifications

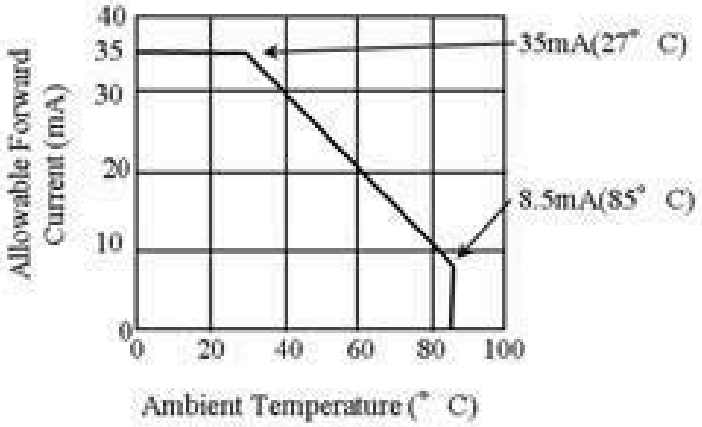
4.1. ABSOLUTE MAXIMUM RATINGS

GND = 0V, Ta = 25°C

Item	Symbol	Min.	Max.	Unit	Note
Supply voltage for LCD	VDDIO	-0.3	2.0	V	(1)
Supply voltage for LCD	VSP	-0.3	5.6	V	(1)
Supply voltage for LCD	VSN	-0.3	-5.6	V	(1)
Supply voltage for TP	VDDDC	-0.3	3.5	V	(1)
Input Voltage	Vt	-0.3	VDDIO +0.3	V	(2)
Input Voltage (TP)	Vtp	-0.3	VDDIO + 0.3	V	(3)
LED Reverse Voltage	V_R	-	5	V	
LED Forward Current	I_{LED}	-	Note (4)	mA	per LED

Notes

1) Keep all Voltages no lower than GND, When absolute maximum rating is exceeded, it may become permanent destruction of LCM. Moreover, if the conditions of 4.3 Electrical characteristics are exceeded even if it is in absolute maximum rating, it may have malfunction and the influence on reliability
2) Applies to the RESET pins
3) The input terminal of TP (DATA0P/DATA0N/DATA1P/DATA1N/STB_CLKP/STB_CLKN)
4) Ambient Temperature vs. Allowable Forward Current



4.2. Typical Operation Conditions

DC Characteristics

GND = 0V, Ambient temperature = 25°C unless otherwise specified

Item	Symbol	Condition	Values			Unit	Note
			Min	Typ.	Max		
Digital Power Supply Voltage for LCD	VDDIO		1.65	1.8	1.95	V	
Analog Power Supply Voltage for LCD	VSP		5.4	5.5	5.6	V	
Analog Power Supply Voltage for LCD	VSN		-5.4	-5.5	-5.6	V	
Analog Power Supply Voltage for TP	VDDDC		3.1	3.3	3.5	V	
Low-level input voltage	VIL		0.0	-	0.3 x VDDIO	V	
High-level input voltage	VIH		0.7 x VDDIO	-	VDDIO	V	
Low-level output voltage	VOL	IOL=+1mA	-	-	0.2 x VDDIO	V	
High-level output voltage	VOH	IOH=-1mA	0.8 x VDDIO	-	-	V	
Input high level leakage current	IIH	VIH=VDDIO	-	-	10	μA	
Input low level leakage current	IIL	VIL= 0V	-10	-	-	μA	
Power supply current(Display on)	I_{VDDIO}		-	(19.3)	TBD	mA	NOTE1,2,3
Power supply current(Display on)	I_{VSP}			(15.3)	TBD	mA	NOTE1,2,3
Power supply current(Display on)	I_{VSN}		-	(-10.4)	TBD	mA	NOTE1,2,3
Power supply current(Display on)	I_{VDDDC}		-	(25.8)	TBD	mA	NOTE1,2,3
Power supply current(Sleep in)	I_{VDDIO}		-	(160)	TBD	uA	NOTE1,3

Power supply current(Sleep in)	I_{VSP}		-	0.7	TBD	uA	NOTE1,3
Power supply current(Sleep in)	I_{VSN}		-	0.7	TBD	uA	NOTE1,3
Power supply current(Sleep in)	I_{VDDDC}		-	TBD	TBD	uA	NOTE1,3
Frame rate	f_{frame}			60		Hz	

NOTE1: When it is the power supply voltage Typ. and the temperature of 25 °C.

NOTE2: Display image is "White Pattern" (Still image)

NOTE3: Touch Panel operation is Active and No finger.

4.3. Backlight Unit

Test Condition: I_{LED}=20mA

Worning: LCM Brightness must match Optical Spec requirement when I_{LED}=20mA

Backlight Unit Schematic: (6serials&2parallel)

Item	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Forward Voltage	V_{BL}	TBD	(3.1)	TBD	V	Note 4
BL current	I_{BL}	TBD	(40)	TBD	mA	Note 5

Note 4 : When I_{LED}=20mA，the V_{BL} must be in the range of above table specified.

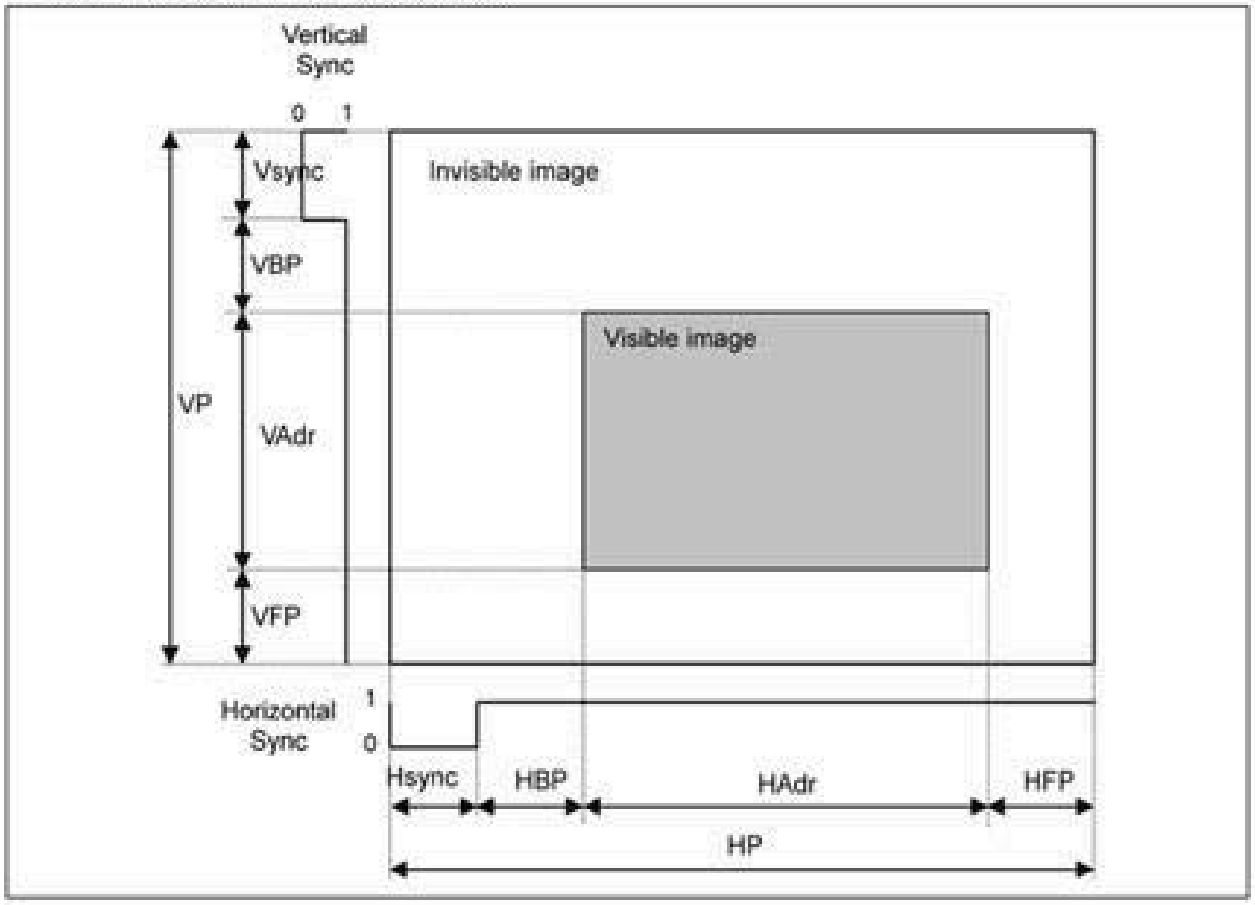
Note 5 : $I_{BL} = I_{LED} * 2$

4.4. Driver and Interface Characteristics

4.4.1 LCD Video Mode sequence

R69338 Video mode support (Burst mode, Non-Burst mode with sync events).

4.4.1.1 Display Timing(Video Mode)



Vertical Display Timing(Video Through Mode)

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Vertical cycle	VP		Line		1928		
vertical low pulse width	VS		Line		1		
Vertical front porch	VFP		Line		4		
Vertical back porch	VBP		Line		3		
Vertical data start point	-	BP	Line		-		
Vertical blanking period	VBL	VFP+BP	Line		-		
Vertical active area	Vadr		Line		1920		

Horizontal Display Timing(Video Through Mode)

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Horizontal front porch	HFP		ByteClock		96		
Horizontal sync pulse width	HPW				-		
Horizontal Back Porch	HBP				-		
Horizontal data start point	-	HS+HBP	ByteClock		45		
Horizontal active area	Hadr		Pixel		1080		

4.4.1.2 Video mode interface timing

DSI supports several formats, or packet sequences, for Video mode data transmission. The peripheral's timing requirements dictate which format is appropriate.

• Non-burst mode with sync events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single sync event is substituted.

• Burst mode – Burst mode refers to time-compression of the RGB pixel (active video) portion of the transmission. RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

Vertical Display Timing (Video Mode)

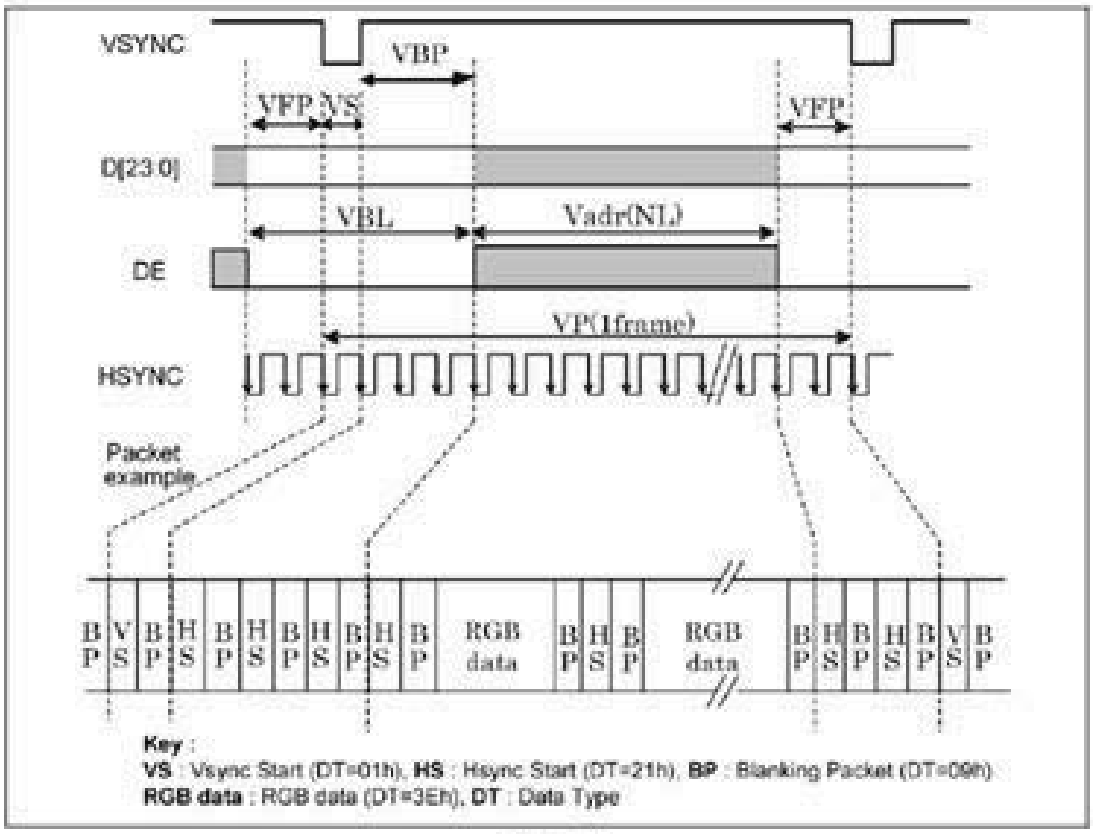


Figure 33

Horizontal Display Timing (Video Mode)

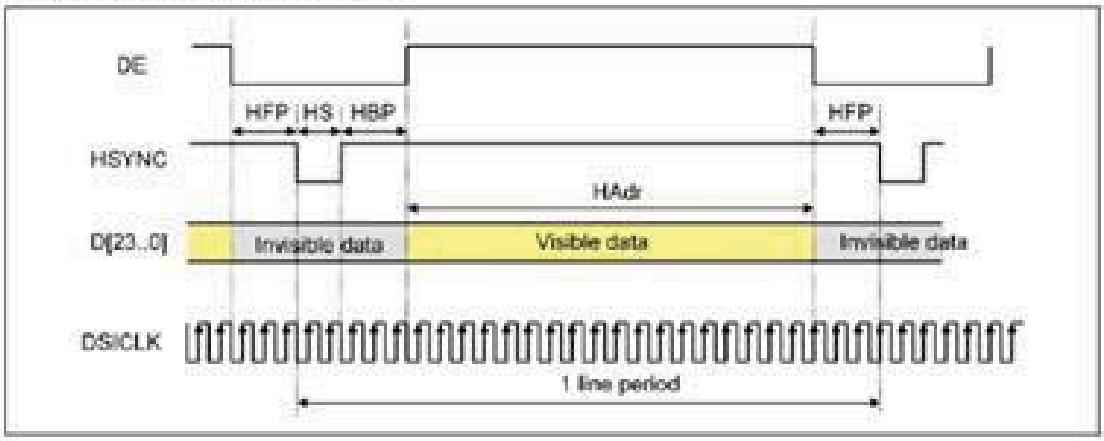


Figure 34

4.4.1.3 Data to clock channel timing

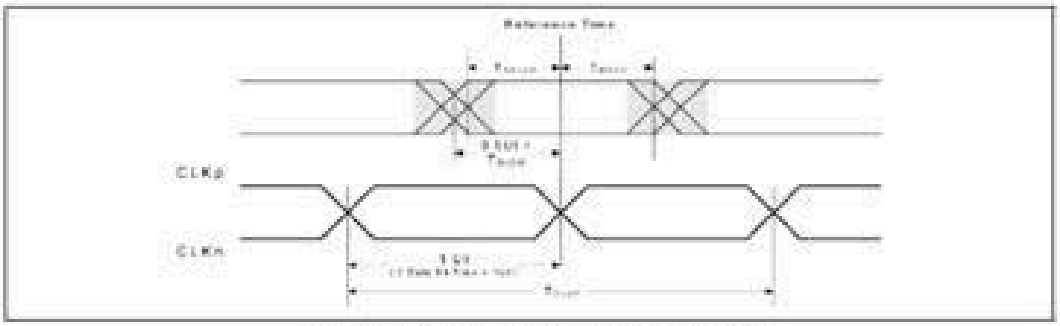
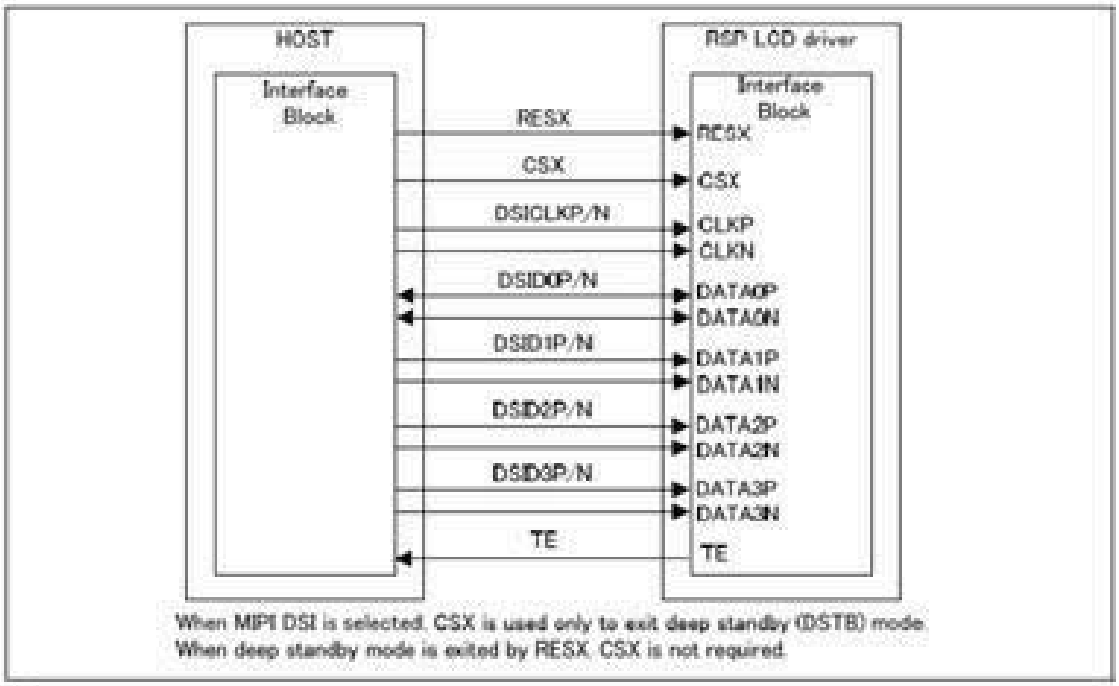


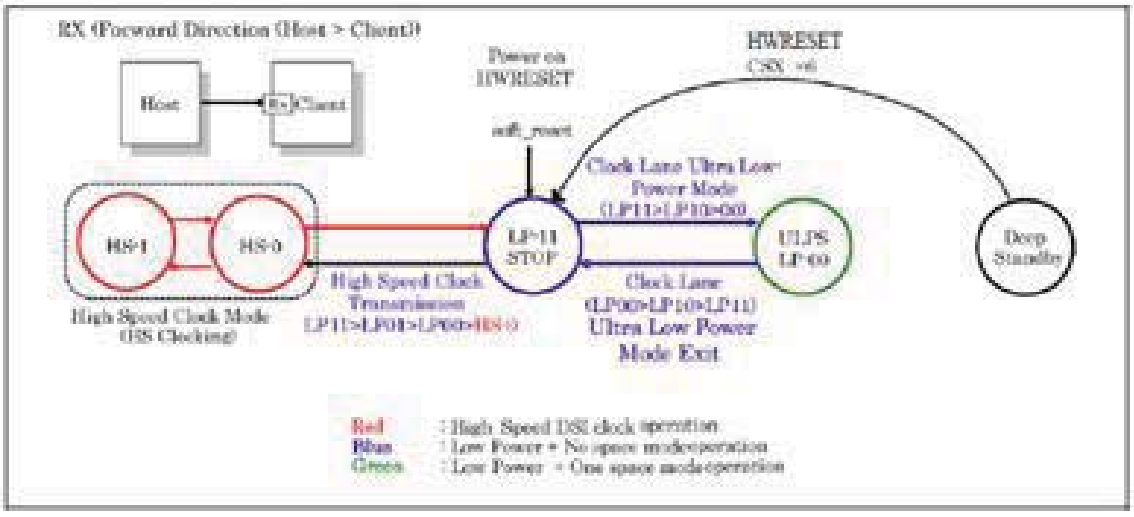
Figure 14 Data to Clock Timing Definitions

4.4.1.4System Interface Configuration (MIPI DSI)

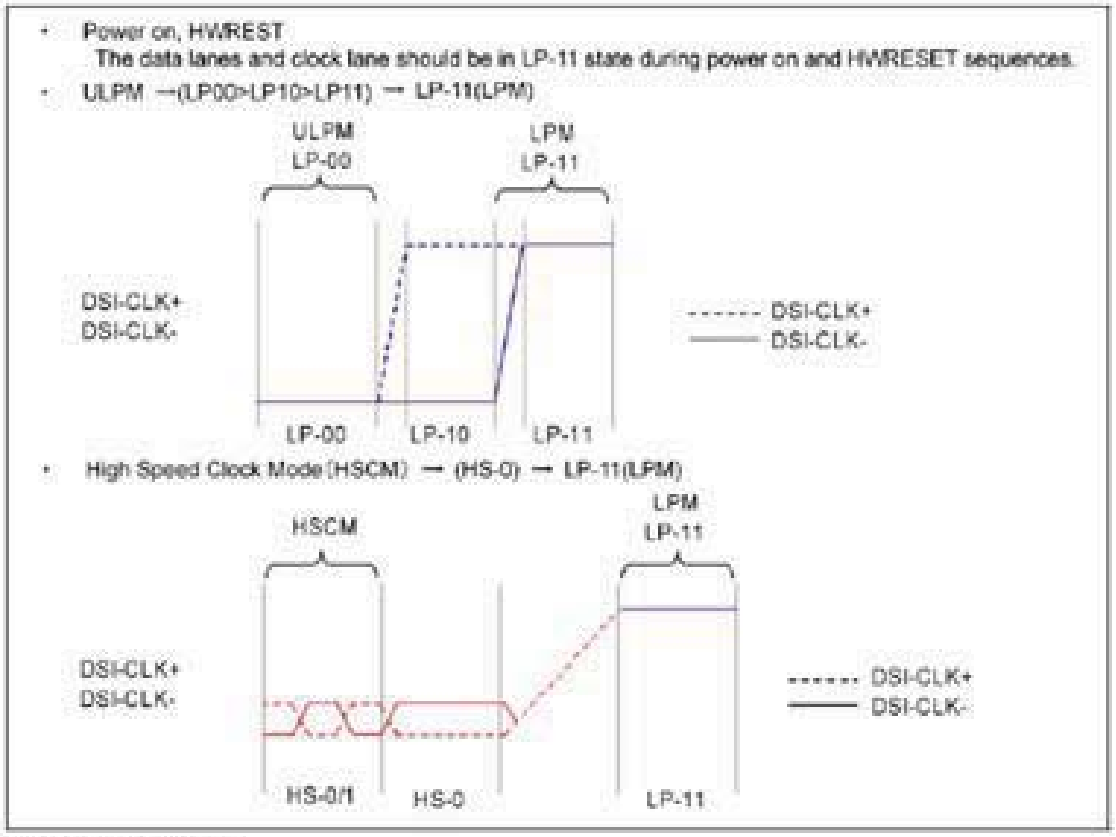
DSI System Configuration



DSI-CLK Lane



Low Power Mode (LP-11: STOP)



High Speed Clock Mode

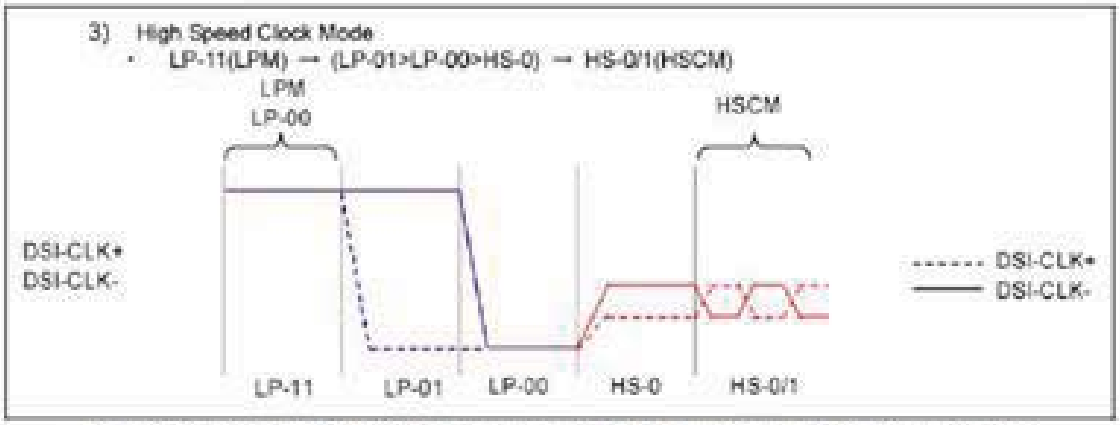


Figure 23 Switching the Clock Lane between Clock Transmission and Low Power Mode 3

High Speed Clock Burst

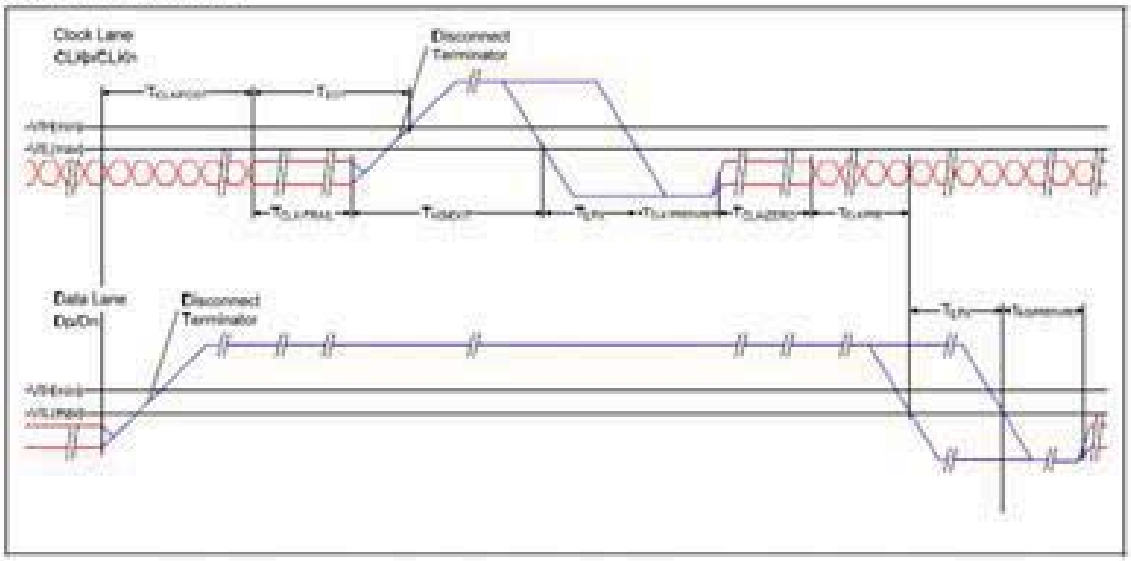


Figure 24 Switching the Clock Lane between Clock Transmission and Low Power Mode 4

4.4.1.5 MIPI DSI Characteristics

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	-	-	70	3
	Differential input low threshold	VIDTL	mV	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	-70	-	-	3
	Single-ended input low voltage	VILHS	mV	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	80	100	125	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.65V~ 3.60V v	880	-	1350	
	I/O leakage current	ILEAK	µA	Vin = -50mV ~ 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVCC=DPHYVCC= 1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	450	-	-	

Notes: 1. VCMRX (DC) = (VP+VDN)/2

2. Excluding COG resistance (contact resistance and ITO wiring resistance). The values are tentative.

3. Minimum 110mV/-110mV HS differential swing is required for display data transfer.

MIPI DSI HS-RX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	100	-	500	4
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	1	-	10	
DSI Data Transfer Rate	fDSIR	Mbps	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V DSI 4 lanes	200	-	1000	4
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	0.15	-	-	6
		ns	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	0.15	-	-	5,6
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	0.15	-	-	6
		ns	IOVCC=1.65V~ 3.60V DPHYVCC=1.65V~ 3.60V	0.15	-	-	5,6

Notes: 4. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.
5. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.
6. tSETUP/tHOLD Time are measured without HS-TX Jitter.

MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Item	Symbol	Unit	Test condition	Min	Typ	Max	Notes
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$			40 ns + 4*UI	-	85ns + 6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$			145ns + 10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$			max (n*8*UI, 60 ns + n*4*UI)	-	-	1,2
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	ns		100	-	-	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}			$4*T_{LPTX}$			
Time-out before new TX side starts driving	$T_{TA-SURE}$			$1*T_{LPTX}$	-	$2*T_{LPTX}$	
Time to drive LP-00 by new TX	T_{TA-GET}			$5*T_{LPTX}$			
Length of any Low-Power state period	T_{LP}	ns		50	-	-	
Ratio of $T_{LPXMASTER}/T_{LPXSLAVE}$ between Master and Slave side	Ratio T_{LPX}			2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLKPOST}$			60 ns + 52UI	-	-	3
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	ns		300	-	-	
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	T_{CLKPRE}	UI		8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns		38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns		60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}			-	-	105 ns + n*12*UI	2
Length of Low-Power TX period in case of using DSI clock	T_{LPTX1}	UI		-	48	-	4
Length of Low-Power TX period in case of using Internal OSC clock	T_{LPTX2}	ns		-	1/fosc1	-	

Notes: 1. If a > b then max(a, b) = a, otherwise max(a, b) = b
2. Where n = 1 for Forward-direction HS mode.
3. The R69338 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R69338 can work without the remained process if tCLK-POST is more than 256 UI.
4. The R69338 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled. Here, "fosc1" is the frequency of oscillator clock, typical 28 MHz.

4.4.2 TP IIC interface

4.4.2.1 I²C Interface

Figure 6 shows an example of host connection using the S3351 I2C interface. The values of the pull-up resistors should be chosen to ensure that the rise times of the SDA and SCL signals are within the limits set by the I2C specification. This depends on what other slave devices, if any, are on the I2C bus but typically would fall within the range of 2.2 kΩ — 10 kΩ.

Refer to the *ClearPad Integration Guide* (PN: 511-000399-01) for additional information.

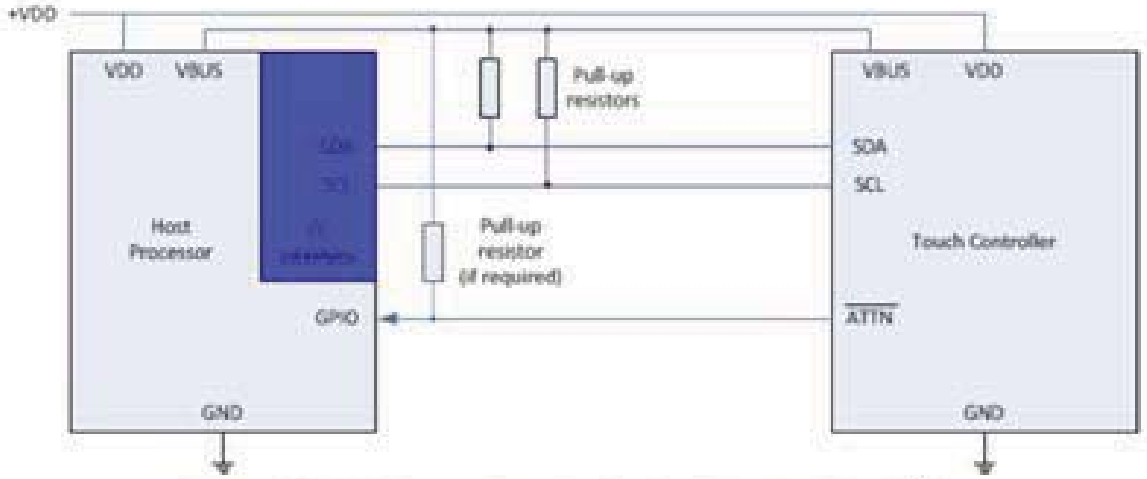


Figure 6. Typical connection of the Touch Controller to host (I²C)

I²C clock stretching

Special attention should be paid to clock stretching when interfacing with a Synaptics Touch Controller over I2C. The host processor must support clock stretching. The first byte of a transaction contains the slave address and read/write bit. At the end of the first byte, the sensor holds SCL low (clock stretches) and checks that the slave address matches its own. If the slave address does not match, the S3351 will not stretch the clock on subsequent byte transmissions until it detects the next start condition. If the slave address does match, the sensor acknowledges and may stretch the clock after some or all of the subsequent bytes within the same transaction (Figure 7).

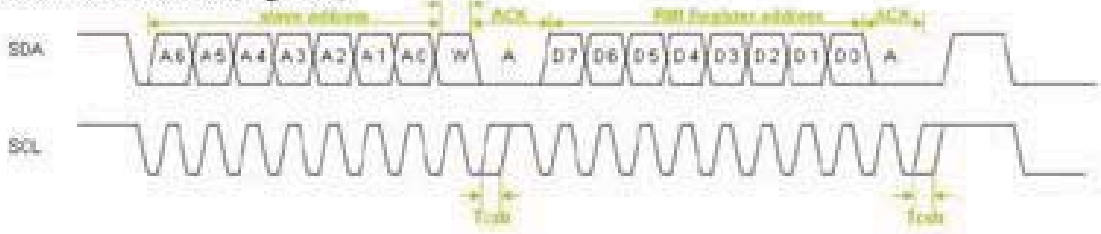
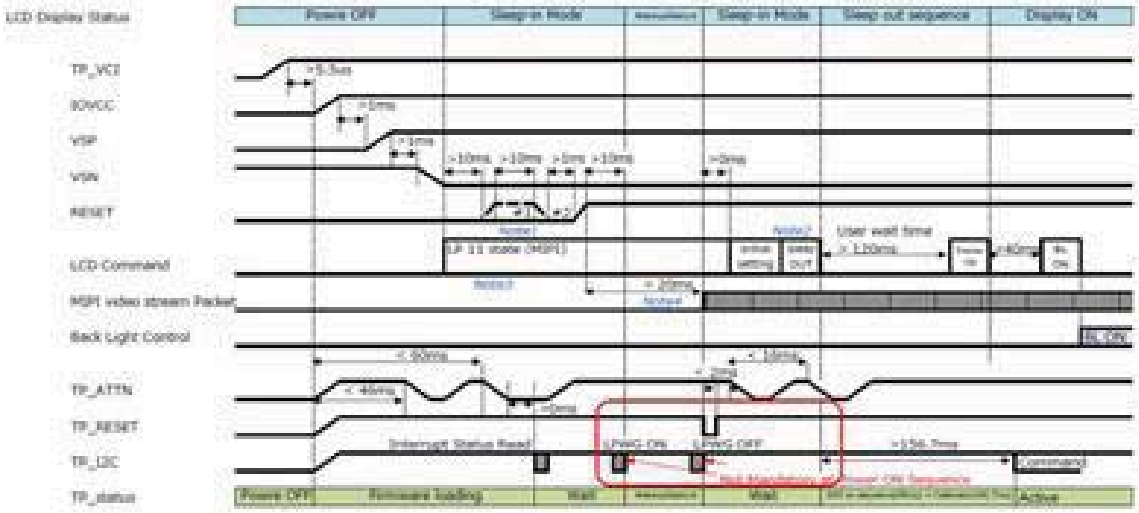


Figure 7. Clock stretching within an I²C transaction

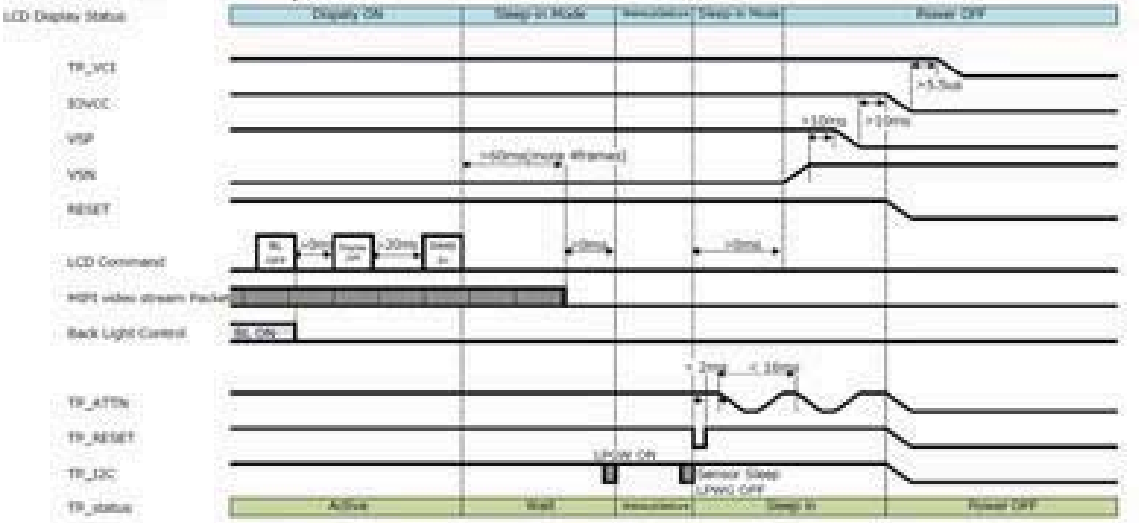
Typical clock stretch time (Tstr) is less than 25 us.

4.4.3 Power ON & Power OFF

LCD Power ON sequence



LCD Power OFF sequence



4.4.4 Initial code table

Power ON & Display ON

Step	Mode	Action/Command	DSI Data Type	Address	Para.	Data	Note
1	Initial Condition	RESX = L					
2		Power Supply IOVDD ON (Typ.1.8V)					
3		- wait Min. 1ms					wait for IOVDD=100% (depends on Power Supply Circuit)
4		Power Supply AVDD= ON (Typ.3.0V)					
5		- wait Min. 1ms					wait for VSP-->VSN ordering (depends on Power Supply Circuit)
6		Power Supply AVDD= ON (Typ.5.5V)					
7		- wait Min. 5ms					
8		RESX = H					
9		- wait Min. 10ms					wait to VSP/VSN=±90% and RESX=Low period (depends on Power Supply Circuit)
10		RESX = H					
11		- wait 10ms					wait min. 10ms
12	NVM Auto Load						
13	Sleep Mode In						
14		write_Display_Brightness	DCS	0x51	0x01	0xFF	0xFF=FFh : LED 100% Duty
15		write_CTRL_Display	DCS	0x53	0x01	0x0C	0x24 : LED ON 0x0C : Reserved ON
16		write_CABC	DCS	0x55	0x01	0x02	0x00 : CABC OFF 0x02 : CABC ON
17		set_sleep_mode	DCS	0x11	-	-	
18		- wait Min. 120ms					
19		set_display_on	DCS	0x29	-	-	
20	Sleep Mode Off Display On						

Display OFF & Power OFF

Step	State	Action/Command	DSI Data Type		Address	Para.	Data	Note
1	Sleep Mode Off Display On							
2		set_display_off	DCS	0x05	0x28	-	-	
3		+ wait min. 20ms						
4	Sleep Mode Off Display Off							
5		enter_sleep_mode	DCS	0x05	0x10	-	-	
6		+ wait min. 80ms						
7	Sleep Mode On							
8		Power Supply AVDD= OFF (Typ=6.6V)						
9		+ wait min. 10ms						Wait for VGH / VGP ramping (depends on Power Supply Circuit)
10		Power Supply AVEE= OFF (Typ=-5V)						
11		+ wait min. 10ms						Wait for VGP = 10%, VGN = 10% (depends on Power Supply Circuit)
12		RESX=L						
13		+ wait min. 5ms						
14		Power Supply IOVDD OFF (Typ=1.8V)						
15	Power Off							

5. OPTICAL CHARACTERISTICS

(T_a=+25℃)

Item		Symbol	Condition	Min	Typ	Max	Unit	Notes
Brightness		B	φ=0°, θ=0°	400	450	-	cd/m²	(1),(2)
Brightness Uniformity		-	φ=0°, θ=0°	80	-	-	%	(2),(3),(5)
Viewing Angle		φ1+φ2	θ=0°, CR>10		160	-	deg	(4),(6),(7)
			θ=90°, CR>10		160	-		
Color Tone (Primary Color)	Red	x	φ=0°, θ=0°	TBD	TBD	TBD	-	(9)
		y		TBD	TBD	TBD		
	Green	x		TBD	TBD	TBD		
		y		TBD	TBD	TBD		
	Blue	x		TBD	TBD	TBD		
		y		TBD	TBD	TBD		
	White	x		TBD	TBD	TBD		
		y		TBD	TBD	TBD		
Contrast Ratio		CR	φ=0°, θ=0°	(700)	(1000)	-	-	(6)
Response Time		tr+tf	φ=0°, θ=0°			(35)	ms	(8)
NTSC Ratio		-	φ=0°, θ=0°	(60)	(70)	-	%	-
Gamma		-		(1.9)	(2.2)	(2.5)		
Cross Talk		-		-	-	(4)	%	(10)
Flicker		-		-	-	(-25)	dB	(11)

Measurement Conditions

Measurement environment: Dark room

Ambient temperature: Ta=25°C

Power supply voltage: VDDIO=1.8V

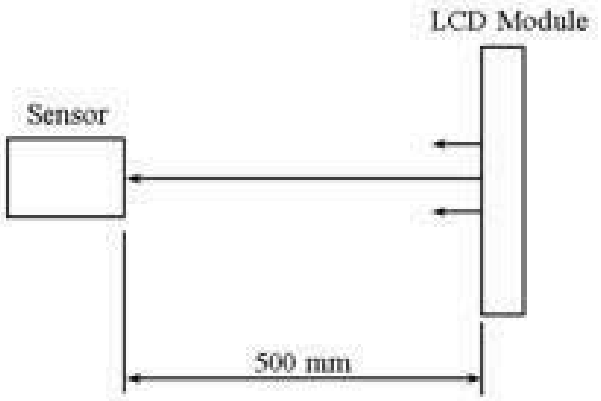
VSP=5.5V

VSN=-5.5V

Backlight current: IBL=40mA (ILED=20mA)

Notes

(1) Definition of Brightness "B"



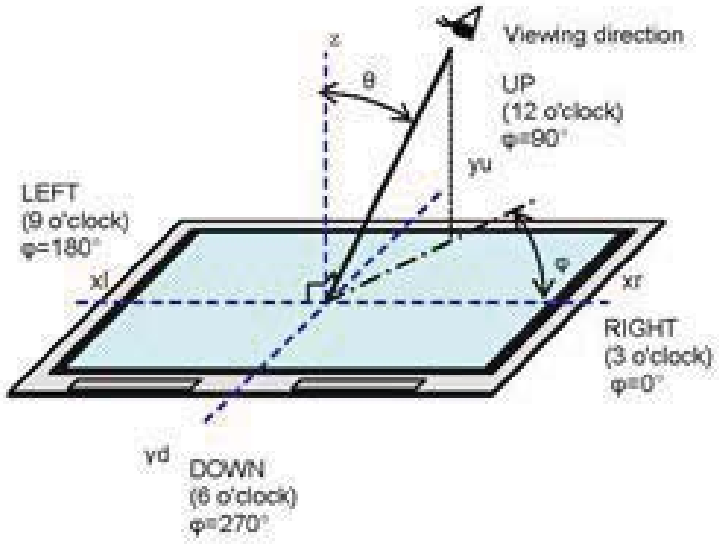
Sensor: KONICA MINOLTA CS-2000 or equivalent
Measurement point: Center of LCD's active area

(2) Display image for measurement: All White

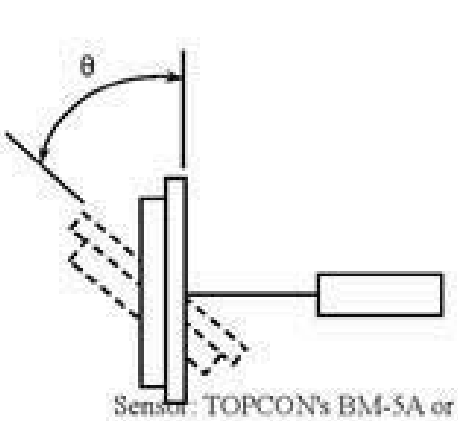
(3) Definition of brightness uniformity

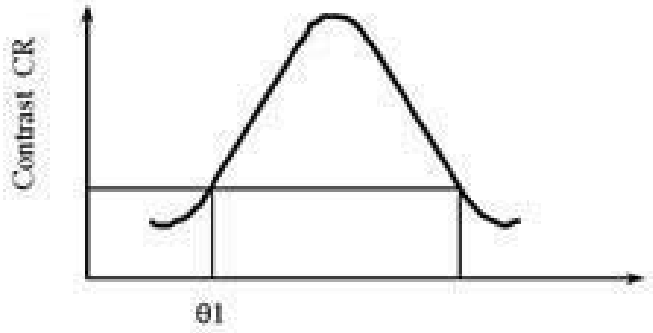
$$\text{Brightness uniformity} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\ (\%)$$

(4) Viewing Angel: Definition of θ and φ



Definition of Viewing Angle θ

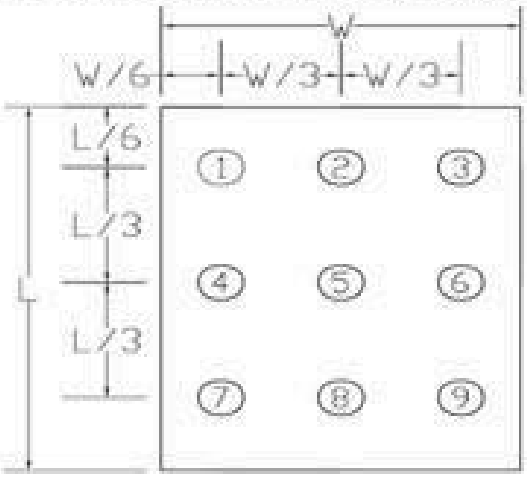




Sensor: TOPCON's BM-5A or equivalent

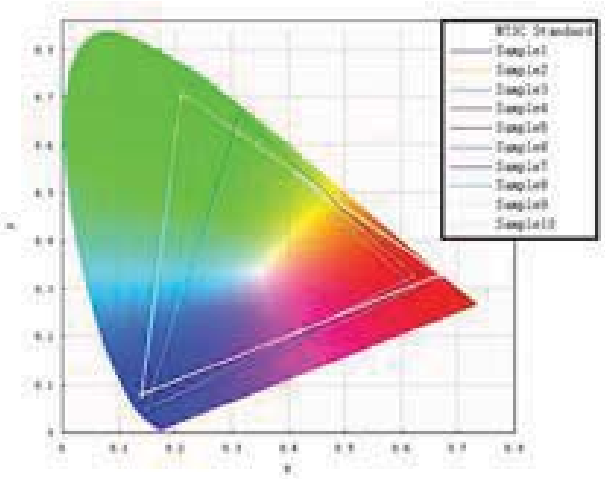
(5) Color Tone: Color coordinates of CIE 1931
The test condition is at I_{LED}=21mA and measured on the surface of LCD module at 25℃.
Measurement equipment: CA310

The Color Coordinate (CIE 1931) is center of active area of the module



Defintion of Color of CIE Coordinate and NTSC Ratio.

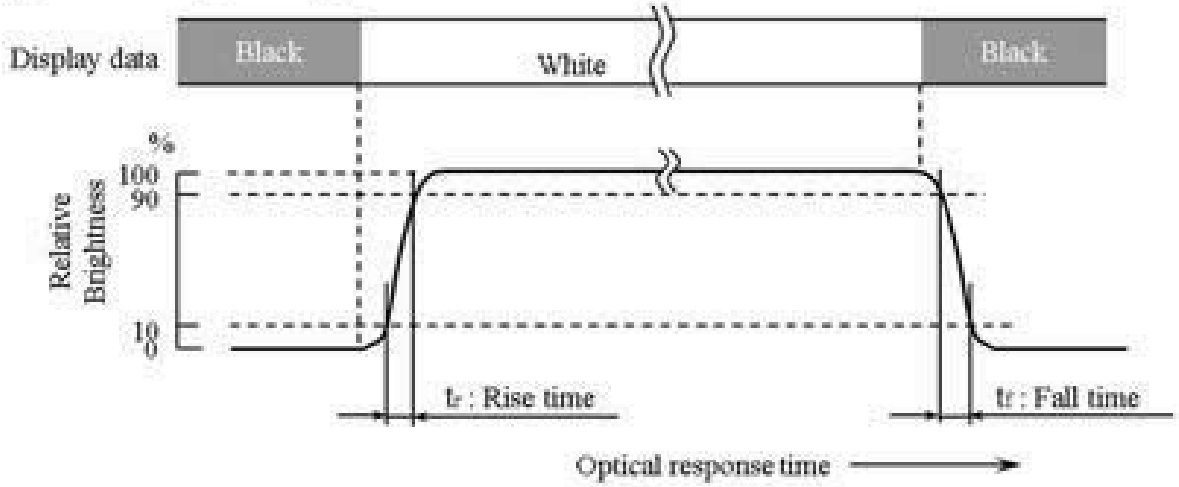
$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$



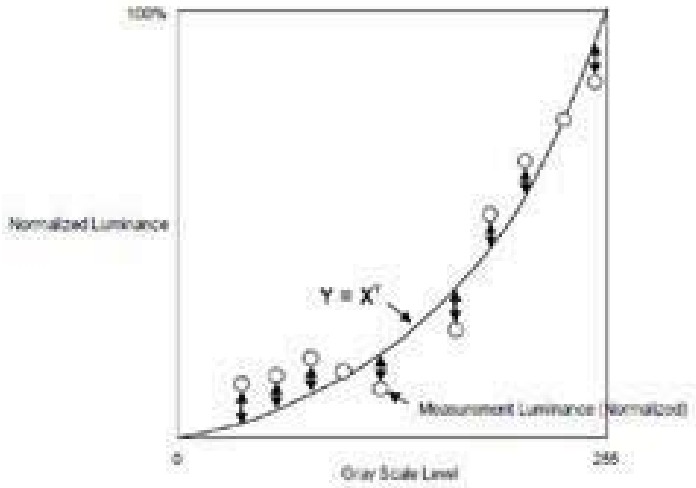
(6) Definition of Contrast "CR"

$$CR = \frac{\text{Brightness when displaying White raster}}{\text{Brightness when displaying Black raster}}$$

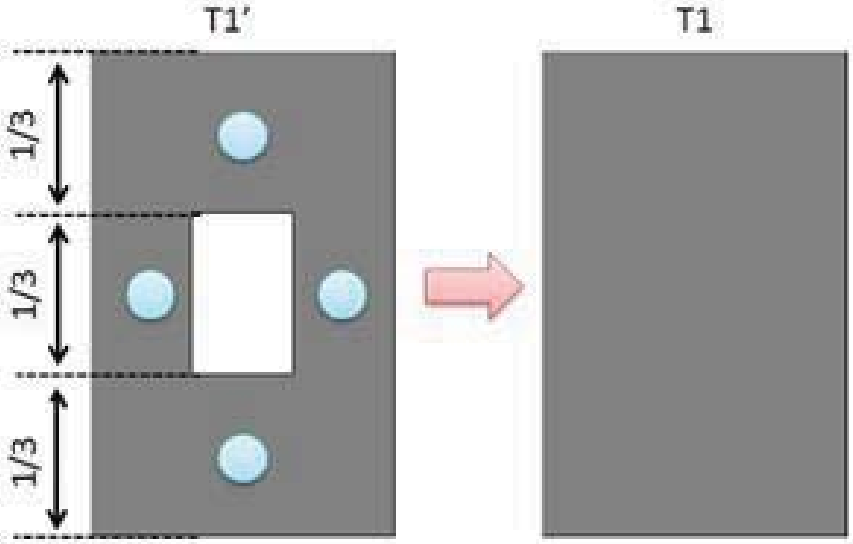
(7) Definition of Optical Response Time



(8) Gamma value is the exponent of power function which approximates the relation between gray scale level and its luminance normalized by maximum luminance.
Optimum exponent of approximate function is determined with the method of least square

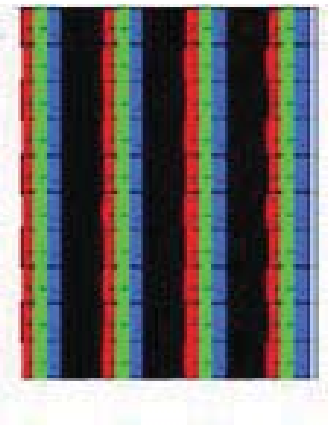


(9) Definition of Cross Talk
Measurement pattern: Gray by L128



Cross Talk Ratio(%) =(T1' – T1) / T1

(10) Definition of Flicker
Module should stay in standing for 60 hours, and then turn on display for 40 seconds before flicker measurement.
Measurement pattern:Pixel column pattern.



7. Handling Precautions

7.1. Safety

The liquid crystal in the LCD is poisonous. DO NOT put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

7.2. Handling

The LCD and touch panel is made of plate glass. DO NOT subject the panel to mechanical shock or to excessive force on its surface.
Do not handle the product by holding the flexible pattern portion in order to assure the reliability
Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
Provide a space so that the panel does not come into contact with other components.
To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

7.3. Static Electricity

Ground soldering iron tips, tools and testers when they are in operation.
Ground your body when handling the products.
Power on the LCD module BEFORE applying the voltage to the input terminals.
DO NOT apply voltage which exceeds the absolute maximum rating.
Store the products in an anti-electrostatic bag or container.

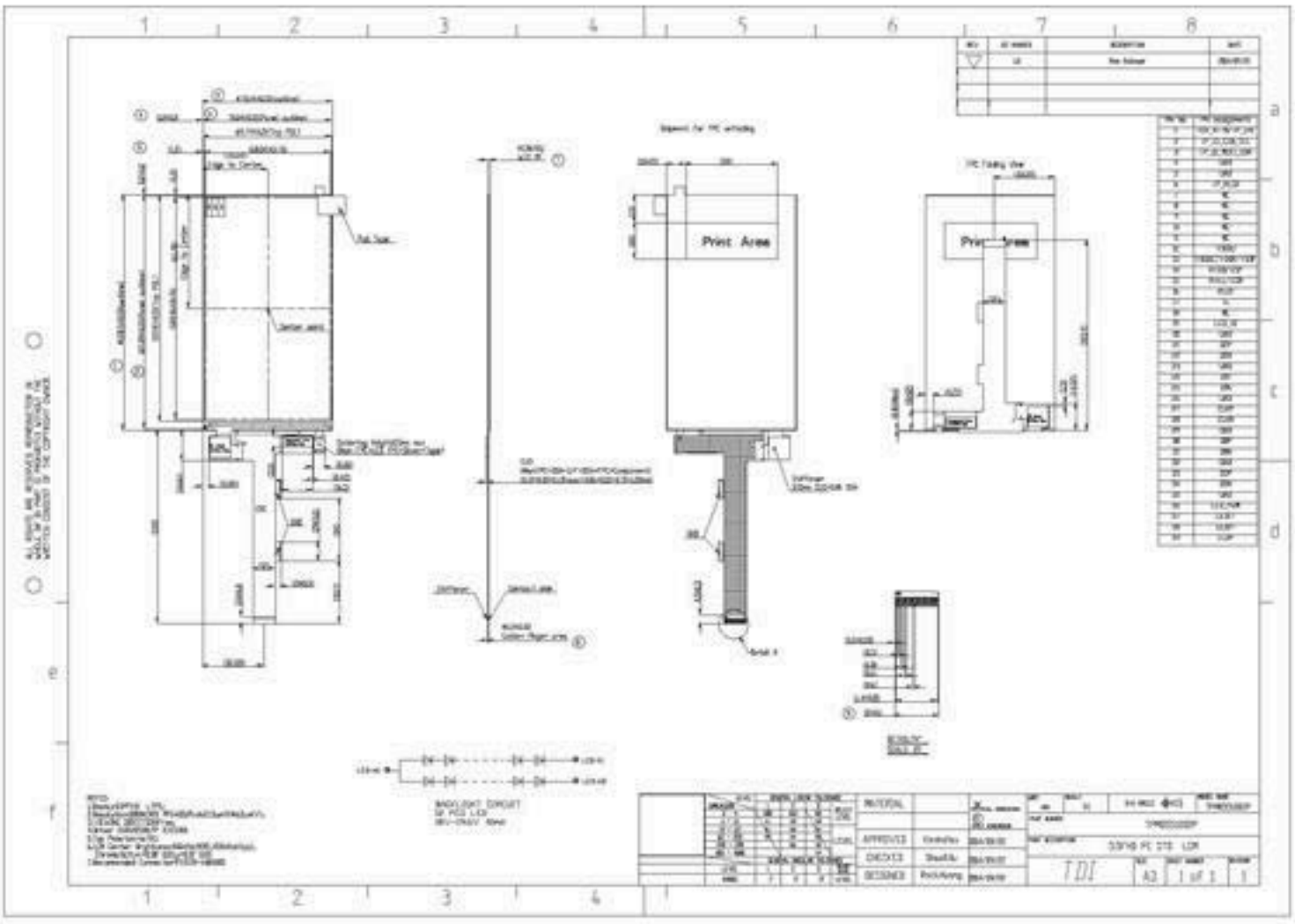
7.4. Storage

Store the products in a dark place at +25℃±10℃ with low humidity (65%RH or less).
DO NOT store the products in an atmosphere containing organic solvents or corrosive gas.

7.5. Cleaning

DO NOT wipe the touch panel with dry cloth, as it may cause scratch.
Wipe off the stain on the product by using soft cloth moistened with ethanol. DO Not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

8. Mechanical Drawing



9. Packing Drawing

	Module/tray (pcs)	Module/carton (pcs)	Carton/ floor(pcs)	Module/ floor(pcs)	Floor/pallet	Module/pallet (pcs)
数量 quantity	6	162	6	6*162=972	5	972*5=4860
Dimension(mm)	449*320		468*349*258			1130*975*130

Explanation :

1. This specification drawing applies to 449*320mm tray.