

# NTD80N02

## Power MOSFET

### 24 V, 80 A, N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### Features

- Pb-Free Packages are Available

#### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	24	Vdc
Gate-to-Source Voltage – Continuous	V <sub>GS</sub>	±20	Vdc
Drain Current – Continuous @ T <sub>C</sub> = 25°C – Single Pulse (t <sub>p</sub> = 10 μs)	I <sub>D</sub> I <sub>DM</sub>	80* 200	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C	P <sub>D</sub>	75	Watts
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 24 Vdc, V <sub>GS</sub> = 10 Vdc, I <sub>L</sub> = 17 Apk, L = 5.0 mH, R <sub>G</sub> = 25 Ω)	E <sub>AS</sub>	733	mJ
Thermal Resistance – Junction-to-Case – Junction-to-Ambient (Note 1) – Junction-to-Ambient (Note 2)	R <sub>θJC</sub> R <sub>θJA</sub> R <sub>θJA</sub>	1.65 67 120	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in<sup>2</sup>).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).

\*Chip current capability limited by package.

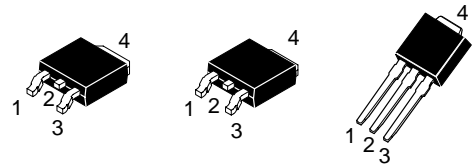
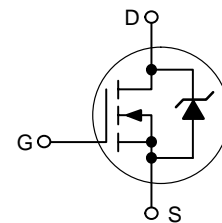


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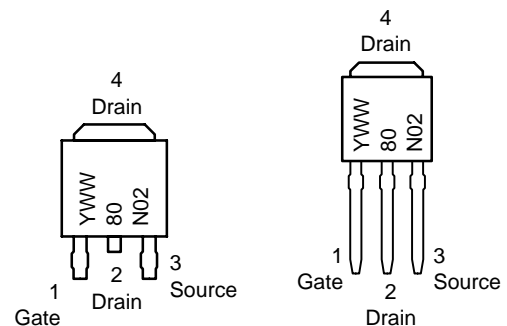
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
24 V	5.0 mΩ	80 A

#### N-Channel



**CASE 369AA** DPAK STYLE 2  
**CASE 369C** DPAK STYLE 2  
**CASE 369D** DPAK STYLE 2  
 (Surface Mount) (Surface Mount) (Straight Lead)

#### MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year  
 WW = Work Week  
 80N02 = Device Code

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTD80N02

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Positive Temperature Coefficient	V <sub>(BR)DSS</sub>	24 –	27 25	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = 24 Vdc) (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = 24 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	–	–	±100	nAdc

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Negative Threshold Temperature Coefficient	V <sub>GS(th)</sub>	1.0 –	1.9 –3.8	3.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 80 Adc) (V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 40 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 20 Adc) (V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 20 Adc)	R <sub>DS(on)</sub>	– – –	5.0 7.5 5.0 7.5	5.8 9.0 5.8 9.0	mΩ
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 10 Adc) (Note 3)	g <sub>FS</sub>	–	20	–	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 V, f = 1.0 MHz)	C <sub>iss</sub>	–	2250	2600	pF
Output Capacitance		C <sub>oss</sub>	–	900	1100	
Transfer Capacitance		C <sub>rss</sub>	–	400	525	

### SWITCHING CHARACTERISTICS (Note 4)

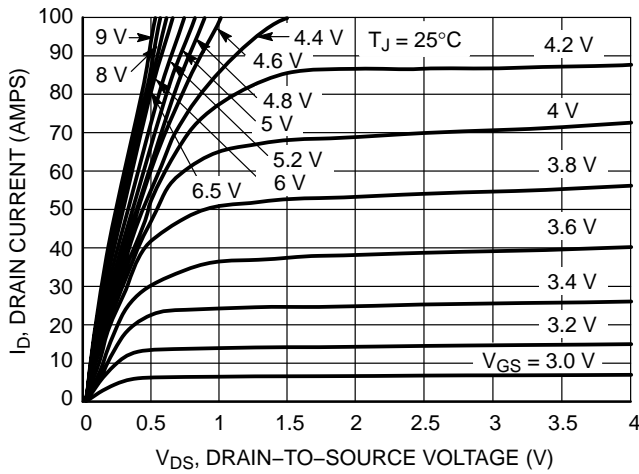
Turn-On Delay Time	(V <sub>GS</sub> = 4.5 Vdc, V <sub>DD</sub> = 20 Vdc, I <sub>D</sub> = 20 Adc, R <sub>G</sub> = 2.5 Ω)	t <sub>d(on)</sub>	–	17	30	ns
Rise Time		t <sub>r</sub>	–	67	125	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	28	45	
Fall Time		t <sub>f</sub>	–	40	75	
Gate Charge	(V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 20 Adc, V <sub>DS</sub> = 20 Vdc) (Note 3)	Q <sub>T</sub>	–	30	42	nC
		Q <sub>1</sub>	–	7.0	12	
		Q <sub>2</sub>	–	18	28	

### SOURCE-DRAIN DIODE CHARACTERISTICS

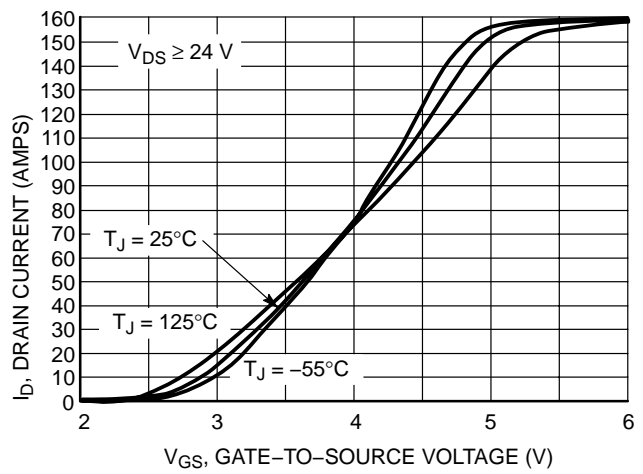
Forward On-Voltage (I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc) (Note 3) (I <sub>S</sub> = 40 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	– – –	0.92 1.05 0.70	1.2 – –	Vdc	
Reverse Recovery Time	(I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	–	38	52	ns
		t <sub>a</sub>	–	20	–	
		t <sub>b</sub>	–	18	–	
Reverse Recovery Stored Charge	Q <sub>rr</sub>	–	0.038	–	μC	

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

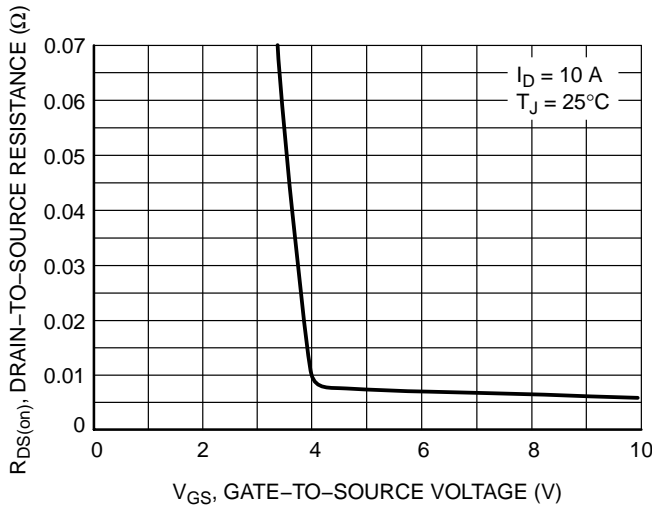
# NTD80N02



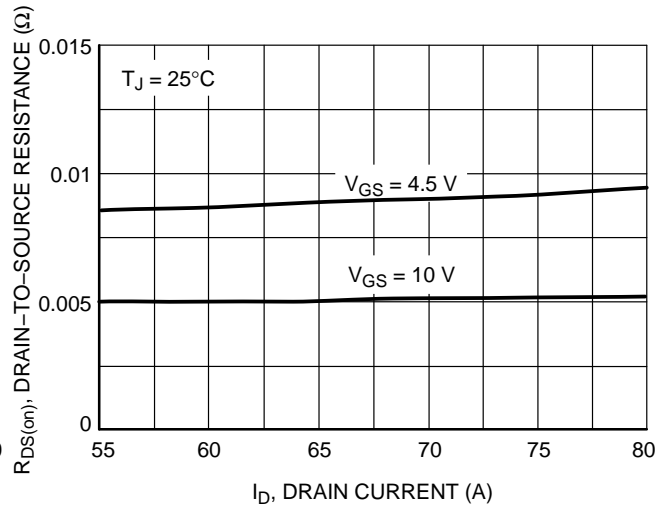
**Figure 1. On-Region Characteristics**



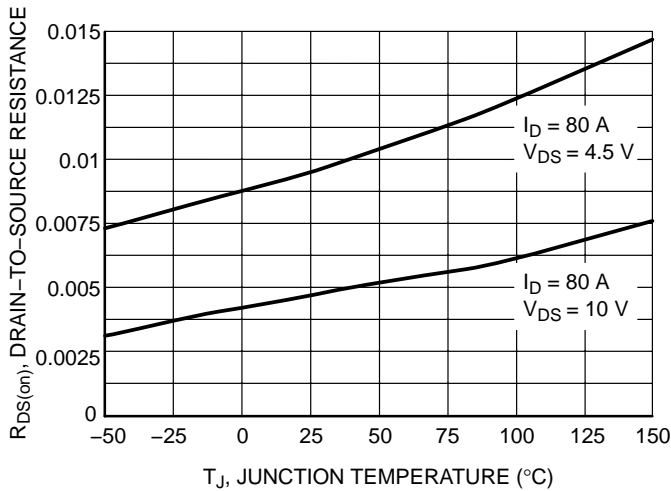
**Figure 2. Transfer Characteristics**



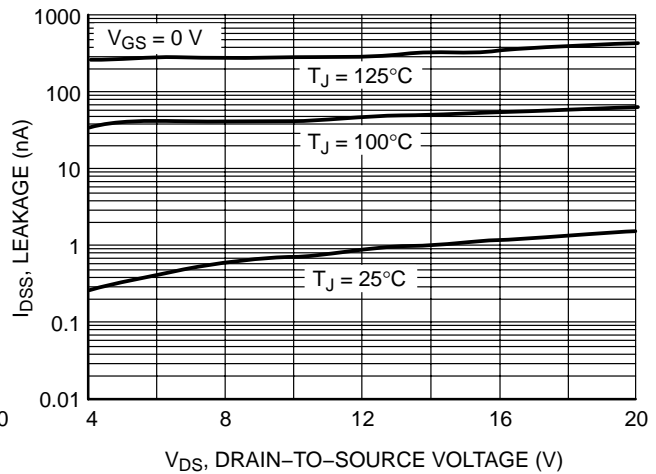
**Figure 3. On-Resistance versus Gate-to-Source Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

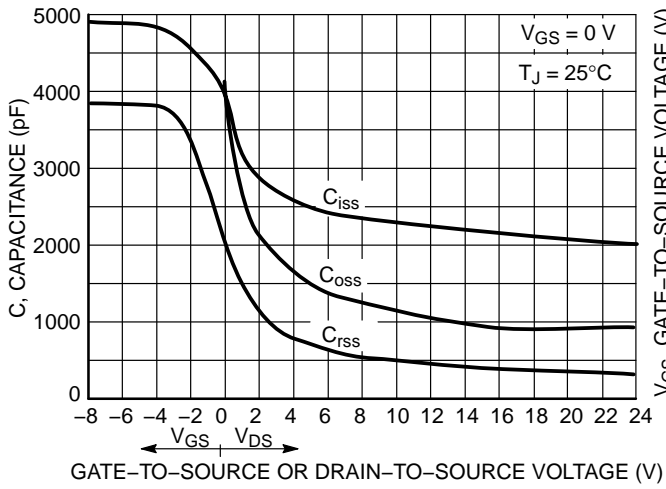


**Figure 5. On-Resistance Variation with Temperature**

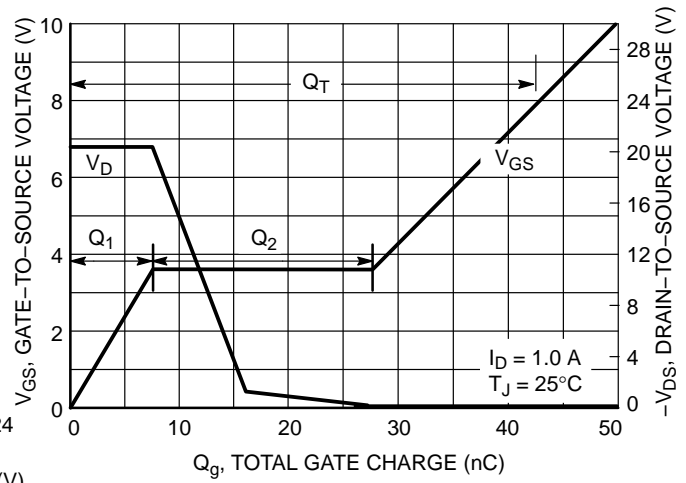


**Figure 6. Drain-to-Source Leakage Current versus Voltage**

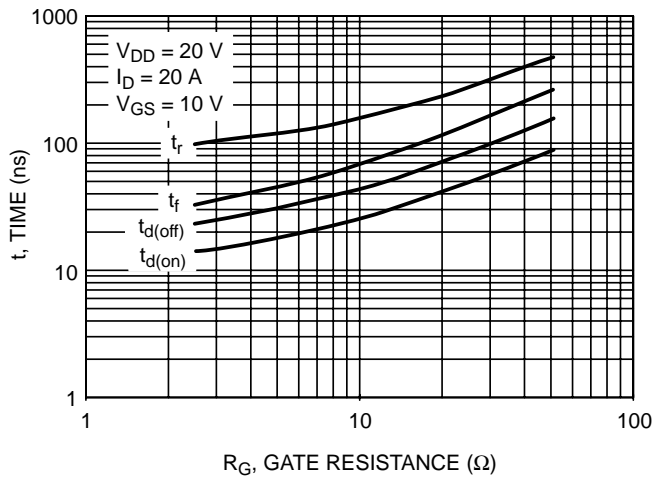
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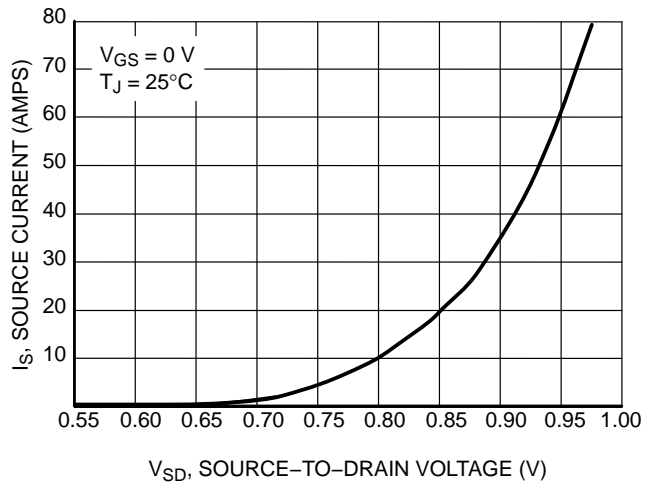
**Figure 7. Capacitance Variation**



**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**

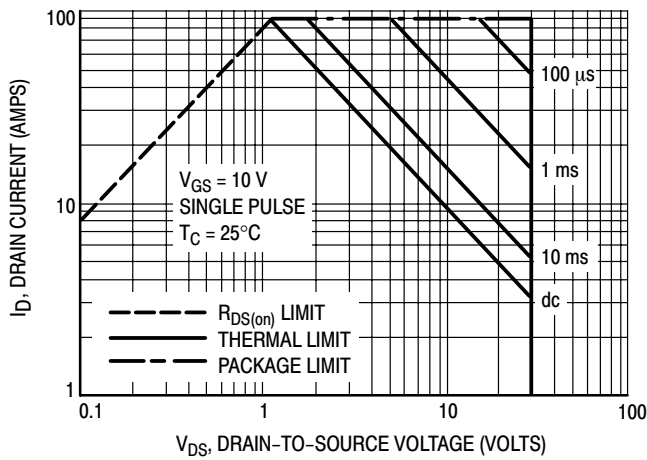


**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

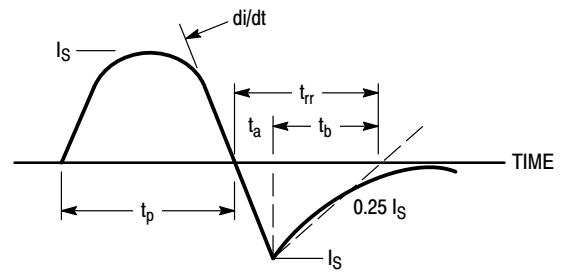


**Figure 10. Diode Forward Voltage versus Current**

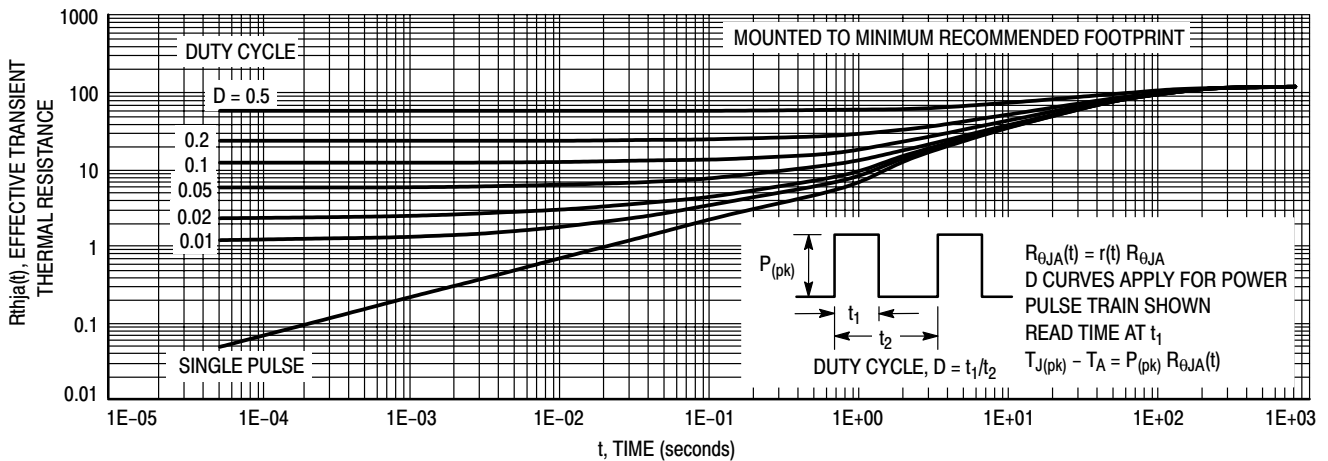
# NTD80N02



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Diode Reverse Recovery Waveform**



**Figure 13. Thermal Response - Various Duty Cycles**

## ORDERING INFORMATION

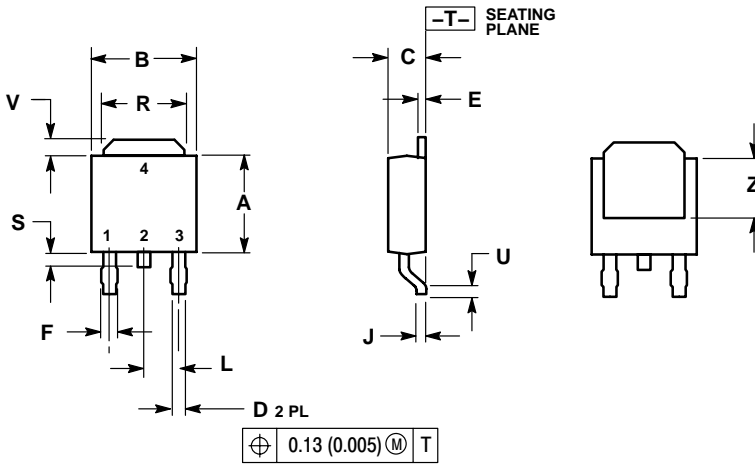
Order Number	Package	Shipping†
NTD80N02	DPAK-3	75 Units / Rail
NTD80N02G	DPAK-3 (Pb-Free)	75 Units / Rail
NTD80N02T4	DPAK-3	2500 / Tape & Reel
NTD80N02T4G	DPAK-3 (Pb-Free)	2500 / Tape & Reel
NTD80N02-001	DPAK-3 Straight Lead	75 Units / Rail
NTD80N02-1G	DPAK-3 Straight Lead (Pb-Free)	75 Units / Rail
NTD80N02-032	DPAK-3 Straight Lead (3.2 ± 0.5 mm)	75 Units / Rail
NTD80N02-032G	DPAK-3 Straight Lead (3.2 ± 0.5 mm) (Pb-Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTD80N02

## PACKAGE DIMENSIONS

DPAK  
CASE 369AA-01  
ISSUE O

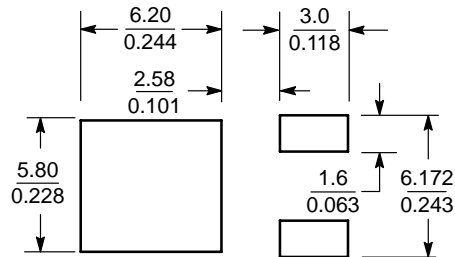


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

## SOLDERING FOOTPRINT\*



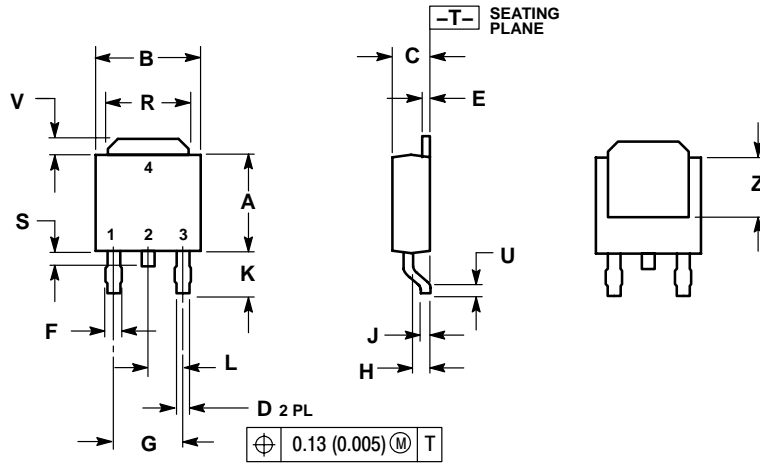
SCALE 3:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTD80N02

## PACKAGE DIMENSIONS

DPAK  
CASE 369C-01  
ISSUE O

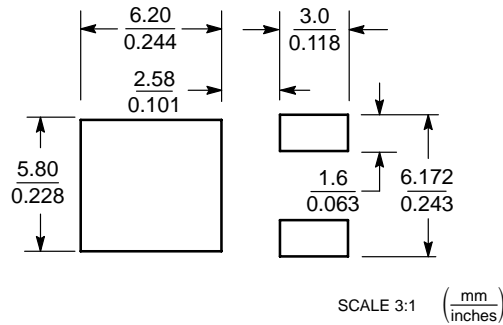


NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

### SOLDERING FOOTPRINT\*

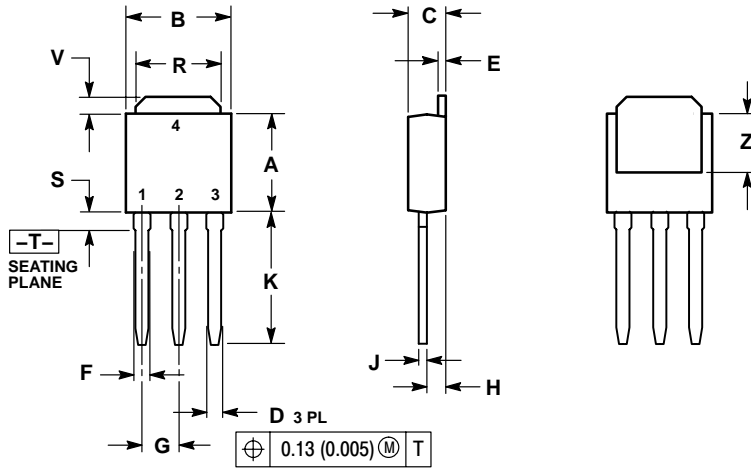


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PACKAGE DIMENSIONS

### DPAK CASE 369D-01 ISSUE B



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

#### STYLE 2:

- PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

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