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LM1076DCW

LCD Module User Manual

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Date: 2016-08-04	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary release	2016-08-04

Table of Content

1. Basic Specifications

1.1 Display Specifications

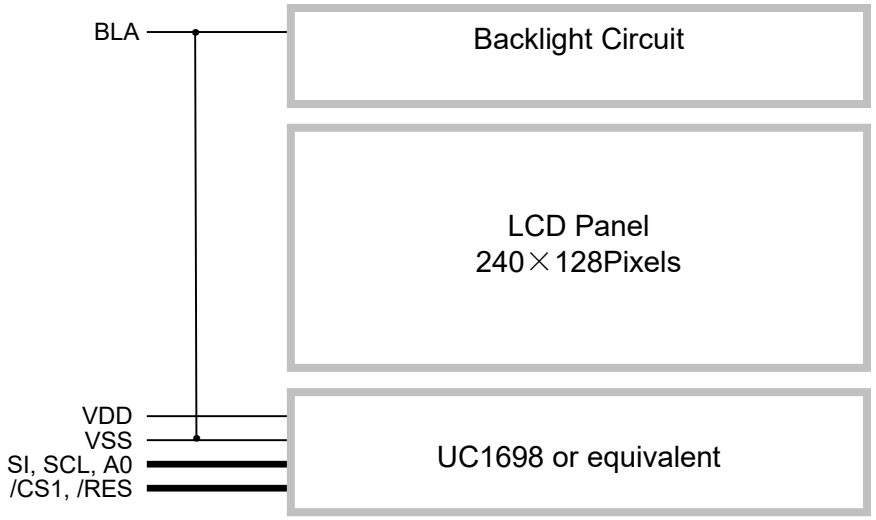
1) LCD Display Mode : FSTN, Positive, Transflective
2) Display Color : Display Data = “1” : Dark Gray(*1)
: Display Data = “0” : Light Gray(*2)
3) Viewing Angle : 6H
4) Driving Method : 1/128 duty, 1/12 bias
5) Backlight : White LED backlight

Note:
*1. Color tone may slightly change by Temperature and Driving Condition.
*2. The Color is defined as the inactive / background color
*3. Fine Contrast adjustment function is necessary in the application design for optimal display result

1.2 Mechanical Specifications

1) Outline Dimension : 79.5 x 64.0 x 10.1MAX (mm)
(See attached Outline Drawing for details)

1.3 Block Diagram



1.4 Terminal Functions

Pin No. (K1&K2)	PIN Name	I/O	Descriptions
			Serial mode
1	VSS	Power	Negative power supply,0V
2	VDD	Power	Positive power supply
3	SI	Input	Serial data input
4	SCL	Input	Serial clock input
5	A0	Input	Register Select A0 = H, Transferring the Display Data A0 = L, Transferring the Control Data
6	/RES	Input	Reset signal /RES = L, Initialization is executed /RES = H, Normal running.
7	/CS1	Input	Chip Select /CS1=L, enable access to the LCD module /CS1=H, disable access to the LCD module
8	BLA	Power	Positive power for LED backlight

2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+3.6	V	V_{SS} = 0V
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

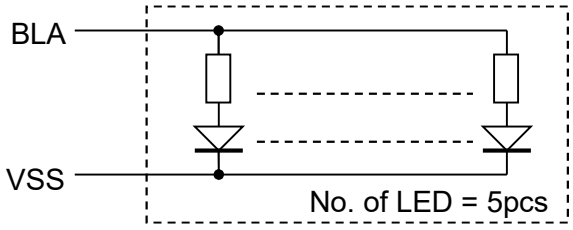
Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition / Application Pin
Operating Voltage	V_{DD}	2.7	3.3	3.465	V	VDD
Input High Voltage	V_{IH}	0.8xV_{DD}	-	V_{DD}	V	/RES, /CS1, A0, SI,SCL
Input Low Voltage	V_{IL}	V_{SS}	-	0.2xV_{DD}	V	
Operating Current	I_{DD}	-	1.2	3	mA	VDD

3.2 LED Backlight Circuit Characteristics

V_{SS}=0V, BLA=3.3V, T_{OP} =25°C

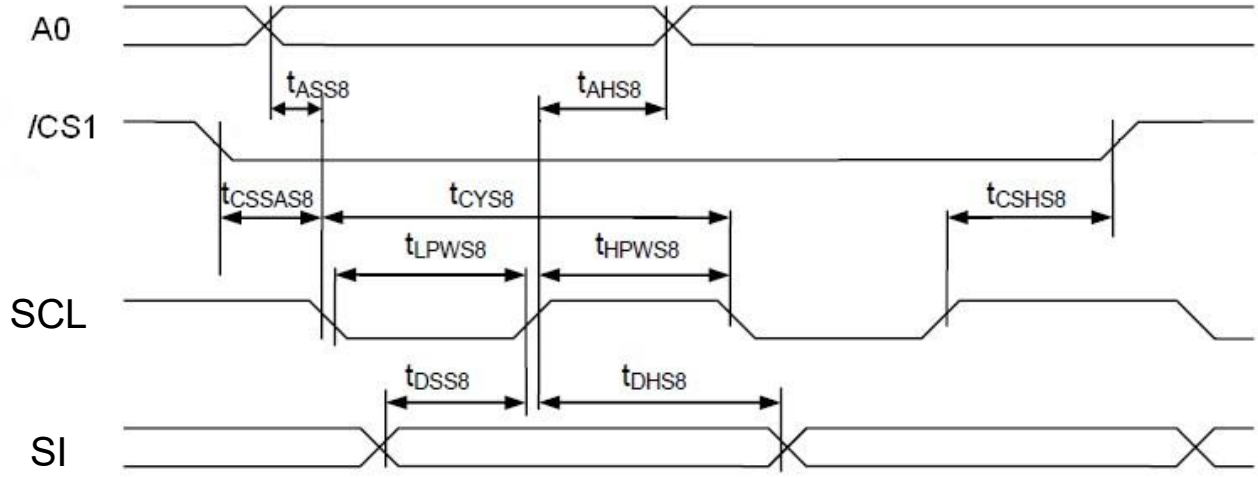
Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	BLA	-	3.3	-	V	BLA
Forward Current	I_{BLA}	-	90	100	mA	BLA

Cautions:
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



3.3 AC Characteristics

3.3.1 4-Write serial

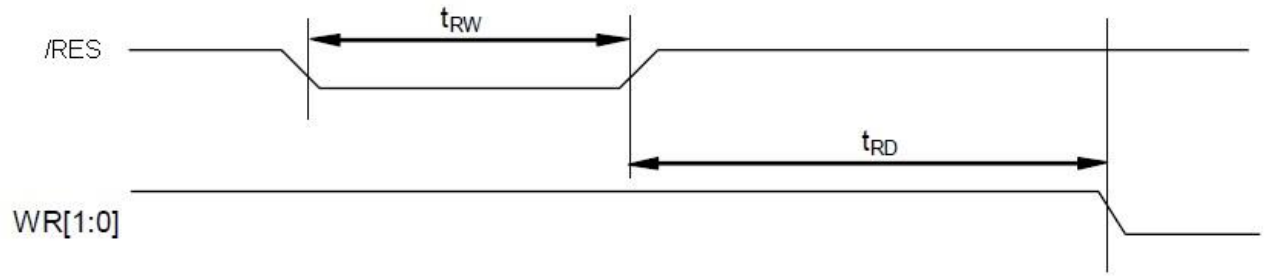


V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time (A0)	tass8	5	-	-	ns
Address hold time (A0)	tahs8	5	-	-	ns
System cycle time	tcys8	91	-	-	ns
SCLK low pulse width	tlpws8	26	-	-	ns
SCLK high pulse width	thpws8	26	-	-	ns
SDA data setup time	tdss8	20	-	-	ns
SDA data hold time	tdhs8	5	-	-	ns
Chip select setup time	tcssas8	7	-	-	ns
Chip select hold time	tcshs8	7	-	-	ns

Note:
*1. Input signal rise/fall time should be less than 15ns .
*2. CL=100pF
*3.All timing is using 20% and 80% of VDD as the reference.

3.3.2 Reset Timing



V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset LOW pulse width	trw	4	-	-	ms
Reset to WR pulse delay	tRD	10	-	-	

Note:
*1.All timing is using 20% and 80% of VDD as the reference.

4. Function specifications

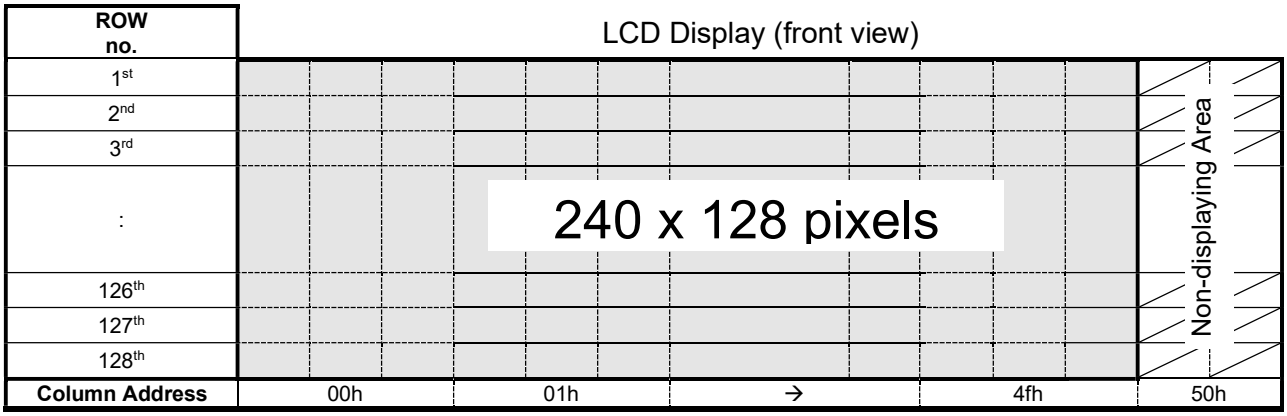
4.1 Adjusting the Display Contrast

This LCD module equipped with latest digital contrast adjustment function.
Its display contrast could be adjusted by MCU command.
(please see the command tables for details)
It is recommended to provide a contrast adjustment interface for end-user,
where the best display result could meet the individual preference in mass production.

4.2 Resetting the LCD module

The LCD module should be initialized by using /RES terminal.
While turning on the VDD and VSS power supply, maintain /RES terminal at LOW level. After the power supply stabilized, release the reset terminal (/RES=HIGH)

4.2.1 Display Memory Map



Note:
*1. This mono LCM is driven by a color LCD driver.
Every three dots are being driven by R G B segment driver.
*2. The above is based on:
- 4R4G4B setting, each dot will be driven by 4bit; LC[7:6]=0:1, DC[4]=1
- Mirror Y direction; LC[2]=0
- Normal X direction; LC[1]=1
- Color Mapping as BGR; LC[5]=0

*3. For details please refer to UC1698 datasheet

4.3 Display Commands

The LCD module contains register, which control the operation. These register can be modified by commands. The following table is a summary of the control registers, their meaning and their default value.

4.3.1 Register Table

Name	Bits	Default	Description
SL	8	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (159 – 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections: 2xFLT on one side non-scrollable, 2xFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	8	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 5 01b: 10 10b: 11 **11b: 12**
TC	2	0H	Temperature Compensation (per °C) **00b: -0.00%** 01b: -0.05% 10b: -0.15% 11b: -0.25%
PM	8	40H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	7	00H	PM offset. PMO[6]=1b: The effective PM value, PMV = PM - PMO[5:0] PMO[6]=0b: The effective PM value, PMV = PM + PMO[5:0]
PC	2	2H	Power Control. PC[0]: **0b: LCD ⩽ 13nF** 1b: 13nF < LCD ⩽ 22nF PC[1]: 0b: External V_{LCD} **1b:** Internal V_{LCD} (10x charge pump)
AC	4	1H	Address Control. AC[0]: WA: Automatic column/row Wraparound (Default **1 : ON**) AC[1]: Auto-Increment order **0b : Column (CA) first** 1b : Row (RA) first AC[2]: RID: RA (row address) Auto Increment Direction (**L : +1** H : -1) AC[3] : Window Program Mode **0b : Inside Mode:** Write to SRAM within the window defined by (WPC0,WPP0) and (WPC1,WPP1) 1b : Outside Mode: Write to SRAM but skip the window defined by (WPC0,WPP0) and (WPC1,WPP1)

Register Table (continue)

Name	Bits	Default	Description
DC	5	18H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray-shade Modulation mode. 0 : On/Off mode **1 : 32-shade Mode** DC[4]: Green Enhance Mode. *Only valid in 4K-color mode.* 0 : Enable. Allows an extra display bit for green color. **1 : Disable**
LC	9	090H	LCD Control: LC[0]: Enable the top FLTx2 and bottom FLBx2 lines in partial display mode (Default **0: OFF**). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: **0: OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **0: OFF**) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 25.2. Klps 01b: 30.5 Klps **10b: 37.0 Klps** 11b: 44.8 Klps Line Rate (for On/Off mode) 00b: 8.5 Klps 01b: 10.4 Klps **10b: 12.6 Klps** 11b: 15.2 Klps (Line-Rate = Frame-Rate x Mux-Rate) LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3) **0 : BGR-BGR** 1 : RGB-RGB LC[7:6] : Color and input mode when DC[4]=1: 01b : 4K color mode. 4R-4G-4B (12-bit/RGB) **10b : 64K color mode**. 5R-6G-5B (16-bit/RGB) when DC[4]=0: 01b : 4K color mode. 4R-5G-3B (12-bit/RGB) 10b : 64K color mode. 5R-6G-5B (16-bit/RGB) LC[8] : Partial Display Control **0b: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 1b: Enabled Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2
NIV	5	1DH	N-Line Inversion: NIV[2:0]: 000b: 11 lines 001b: 19 lines 010b: 21 lines 011b: 25 lines 100b: 29 lines **101b: 31 lines** 110b: 37 lines 111b: 43 lines NIV[3]: 0b: no-XOR **1b: XOR** NIV[4]: 0b: Disable NIV **1b: Enable NIV**
CSF	3	0H	COM Scan Function CSF[0]: Interlace Scan Function **0b: LRM sequence: AEBCD-AEBCD** 1b: LRM sequence: AEBCD-EBCDA CSF[1]: FRC function **0: Disable FRC** 1: Enable FRC CSF[2]: Shade-1 / Shade-30 option **0: Dither directly on input data (SRAM Change)** 1: PWM (Pulse-width modulation) on SEG output stage

Register Table (continue)

Name	Bits	Default	Description
CEN DST DEN	8 8 8	9FH 00H 9FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9
WPC0	7	00H	Window program starting column address. Value range: 0 ~127.
WPP0	8	00H	Window program starting row address. Value range: 0~159.
WPC1	7	7FH	Window program ending column address. Value range: 0~127.
WPP1	8	9FH	Window program ending row address. Value range: 0~159
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command **000** : **Idle** 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip's debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore **1: Use**
MTP	7	--	Multiple-Time Programming. For V_{LCD} fine tune.
MTPID	2	--	Multiple-Time Programming. For LCM manufacturer's configuration.
MTPM	7	00H	MTP Write Mask. Bit =1: program, Bit=0: no action.
MTPM1	2	0H	MTP Write Mask. Bit =1: program, Bit=0: no action.
APC		N/A	Advanced Program Control. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag: 1 for MTP version, 0 for non-MTP version.
MS	1	–	MTP programming in-progress
WS	1	–	MTP Operation Succeeded
ID	2	PIN	Access the connected status of ID pins.

Note: Please refer to UC1698 data sheet for details

4.3.2 Command Table

The following is the list of host command supported.

#	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	Product Code: 8h
				Ver	PMO[6:0]								
				Product Code				PID[1:0]		MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Adv. Program Control	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0 or 1	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0
10	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	0
		0	0	#	#	#	#	#	#	#	#		
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
19	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[4:0]	1DH
				-	-	-	#	#	#	#	#		
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
22	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP commands	Set WPC0	0
		0	0	-	#	#	#	#	#	#	#		
31	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1		Set WPP0	0
		0	0	#	#	#	#	#	#	#	#		
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0		Set WPC1	127
		0	0	-	#	#	#	#	#	#	#		
33	Set Window Program Ending Row Address	0	0	1	1	1	1	0	1	1	1		Set WPP1	159
		0	0	#	#	#	#	#	#	#	#		
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0: Inside
35	Set MTP Operation control	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]		10H
		0	0	-	-	-	#	#	#	#	#			
36	Set MTP Write Mask	0	0	1	0	1	1	1	0	0	1	Set MTPM[6:0] MTPM1[1:0]		0
		0	0	-	#	#	#	#	#	#	#			
		0	0	-	-	-	-	-	-	#	#			
37	Set V_{MTP1} Potentiometer	0	0	1	1	1	1	0	1	0	0	Shared with Window Program commands	Set MTP1	N/A
		0	0	#	#	#	#	#	#	#	#			
38	Set V_{MTP2} Potentiometer	0	0	1	1	1	1	0	1	0	1		Set MTP2	N/A
		0	0	#	#	#	#	#	#	#	#			
39	Set MTP Write Timer	0	0	1	1	1	1	0	1	1	0		Set MTP3	N/A
		0	0	#	#	#	#	#	#	#	#			
40	Set MTP Read Timer	0	0	1	1	1	1	0	1	1	1		Set MTP4	N/A
		0	0	#	#	#	#	#	#	#	#			

Note:
Please refer to UC1698 data sheet for details

5. Design and Handling Precaution

Please refer to "LCD-Module-Design-Handling-Precaution.pdf".