SKY85703-11: 5 GHz WLAN Front-End Module

Applications

- 802.11ac networking and personal computing systems
- PC cards, PCMCIA cards, mini-cards, and half-mini cards
- WLAN-enabled wireless video systems

Features

- Integrated high performance 5 GHz PA, LNA with bypass, and T/R switch
- Fully-matched input and output
- Integrated power detector and directional coupler
- Transmit gain: 30 dB
- Receive gain: 12 dB
- Output power: +16 dBm @ 1.8% EVM, HT80, MCS9
- Output power: +17 dBm @ 3% EVM, HT40, MCS7
- Small, QFN (16-pin, 3 x 3 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

Skyworks Pb-free products are compliant with all applicable legislation. For additional information, refer to *Skyworks Definition of Lead (Pb)-Free*, document number SQ04-0073.
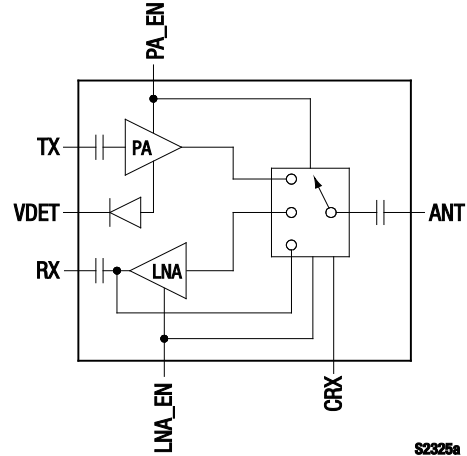

Figure 1. SKY85703-11 Block Diagram

Description

The SKY85703-11 is a highly-integrated, 5 GHz Front-End Module (FEM) incorporating a 5 GHz Single-Pole, Double-Throw (SPDT) transmit/receive (T/R) switch, a 5 GHz Low-Noise Amplifier (LNA) with bypass, and a 5 GHz Power Amplifier (PA) intended for mobile/portable 802.11ac applications and systems.

The LNA and PA disable functions ensure low leakage current in off mode. An integrated power detector is included to provide closed-loop power control within the system. The power detector also acts as a directional coupler to enhance detector accuracy over temperature and load mismatches.

The device is provided in a compact, 16-pin 3 x 3 mm Quad Flat No-Lead (QFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.
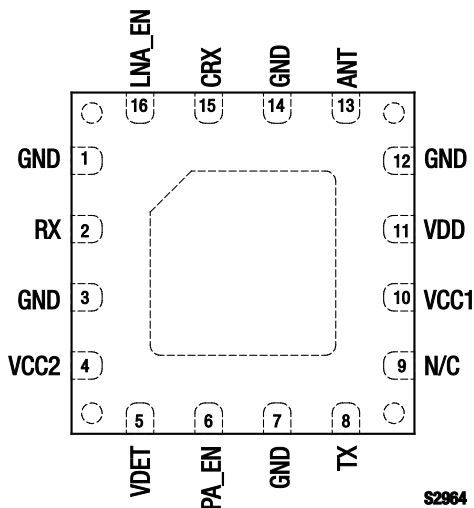

Figure 2. SKY85703-11 Pinout – 16-Pin QFN
(Top View)

Technical Description

The SKY85703-11 is comprised of a high performance 5 GHz PA, 5 GHz LNA, and broadband SPDT switch. The device is fully-matched, and requires few external components for optimal performance, which makes it ideal for small portable/mobile applications. The FEM provides up to +30 dB of gain over the frequency band. The LNA supports an enable/disable mode for power savings when not in receive mode and a bypass function for increased receive dynamic range. The PA can be shut off using the PA_EN signal (pin 6).

The low-loss broadband switch provides the T/R switching function on the SKY85703-11 and has a 1 dB Output Compression Point (OP1dB) of approximately +26 dBm.

Electrical and Mechanical Specifications

Signal pin assignments and functional pin descriptions are described in Table 1. The absolute maximum ratings of the SKY85703-11 are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

The state of the SKY85703-11 is determined by the logic provided in Table 5.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY85703-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

Table 1. SKY85703-11 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	GND	Ground	9	N/C	No connection
2	RX	RF receive output	10	VCC1	PA supply voltage
3	GND	Ground	11	VDD	LNA supply voltage
4	VCC2	PA supply voltage	12	GND	Ground
5	VDET	Detector output voltage	13	ANT	Antenna
6	PA_EN	PA enable	14	GND	Ground
7	GND	Ground	15	CRX	Switch control voltage
8	TX	RF transmit input	16	LNA_EN	LNA enable

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Table 2. SKY85703-11 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	VCC1, VCC2	−0.3	+4.0	V
Supply voltage	V_{DD}		+4.0	V
DC input on control pins (PA_EN, LNA_EN, CRX)	V_{IN}	−0.3	+3.6	V
Input power (50 Ω load)	P_{IN}		+10	dBm
Supply current	I_{CC}		400	mA
Storage temperature	T_{ST}	−40	+150	°C
Junction temperature	T_J		150	°C
Electrostatic Discharge: Human Body Model (HBM), all RF lines, Class 1A HBM, all digital lines, Class 1B			250 500	V V

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Table 3. SKY85703-11 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	VCC1, VCC2, V_{DD}	3.0	3.3	3.6	V
Control logic: High Low	V_{IH} V_{IL}	2.5 0		3.6 0.4	V V
PA enable current	I_{ENABLE}		0.5		mA
LNA bias current	I_{DD}		8	10	mA
LNA enable current				10	µA
CRX enable current				10	µA
Operating temperature	T_{OP}	−40		+85	°C

Table 4. SKY85703-11 Electrical Specifications (1 of 2) (Note 1)
(VCC1 = VCC2 = V$_{DD}$ = 3.3 V, T$_{OP}$ = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f	Main frequency band	5.15		5.85	GHz
Transmit Mode						
Gain	G		24	28	31	dB
Gain flatness		Over any 40 MHz bandwidth	−0.5		+0.5	dB
Output power	P$_{OUT}$	With −45 dB EVM source: MCS9, HT80, 1.8 % DEVM, AT off	+14	+16		dBm
		MCS7, HT40, 3 % DEVM, AT off		+17		dBm
		MCS0, mask compliance		+19		dBm
Current consumption		@ quiescent @ +14 dBm @ +16 dBm @ +19 dBm		175 195 210 240		mA mA mA
Harmonics (2nd and 3rd)	2fo, 3fo	+19 dBm MCS0		−28	−25	dBm/MHz
All spurious		+19.5 dBm OFDM, 6 Mbps		−28	−25	dBm
Isolation		From ANT to either TX or RX pin		40		dB
Input return loss	|S11|			10	7	dB
Output return loss	|S22|			10		dB

Power detector output:
  @ +10 dBm
  @ +16 dBm
  @ +23 dBm
				0.40
				0.65
				1.20
						V
						V
						V

Power detector output impedance	Z$_{OUT\_DET}$	RF output = −30 dBm	2.7		2.9	kΩ
PA switching time		From 10% <−> 90% power change of rising or falling edge, state 1			400	ns
Receive Mode						
Gain	G		10	12	14	dB
1 dB Input Compression Point	IP1dB	LNA active		−5		dBm
Gain step			19	21	23	dB
Gain flatness		Over any 40 MHz bandwidth	−0.25		+0.25	dB
Noise Figure	NF			2.5		dB
Input return loss	|S11|			8		dB
Output return loss	|S22|		5	8		dB
3rd Order Input Intercept Point	IIP3			+6		dBm
Switching time	t$_{SW}$	LNA <−> bypass			200	ns
		RX <−> TX			1	µs

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Table 4. SKY85703-11 Electrical Specifications (2 of 2) (Note 1)
(VCC1 = VCC2 = V_DD = 3.3 V, T_OP = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Receive Bypass Mode						
Insertion loss	|S21|			−9		dB
1 dB Input Compression Point	IP1dB	LNA bypass		+10		dBm

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 5. SKY85703-11 Logic

Mode	State	CRX (J5, Pin 10)	LNA_EN (J5, Pin 4) (Note 1)	PA_EN (J5, Pin 9) (Note 2)
All off (switch in TX mode)	1	0	0	0
WLAN receive	2	1	1	0
WLAN receive bypass mode	3	1	0	0
WLAN transmit	4	0	0	1

Note 1: LNA is on while LNA_EN is high. LNA is off and in bypass mode when LNA_EN is low.

Note 2: PA_EN controls only the PA. It does not control the switch.

Evaluation Board Description

The SKY85703-11 Evaluation Board is used to test the performance of the SKY85703-11 FEM. A suggested application schematic diagram is shown in Figure 3. A photograph of the Evaluation Board is shown in Figure 4. Table 6 provides the Bill of Materials (BOM) list for Evaluation Board components.

Evaluation Board Setup Procedure

Step 1: Connect system ground to pin 2 of the J4 header and to pin 2 of the J5 header.

Step 2: Apply 3.3 V to pins 1 and 3 of the J4 header and to pin 3 of the J5 header.

Step 3: Select a path according to the information in Table 5 (L=0 V, H=3.3 V):

Connect a DMM to pin 12 of the J5 header to monitor the power detector voltage.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

1. Paths to ground should be made as short as possible.

2. The ground pad of the SKY85703-11 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

NOTE: A poor connection between the slug and ground increases junction temperature (T_J), which reduces the lifetime of the device.

3. Place component C10 close to pin 4.

4. Place component C6 close to pin 10.

Package Dimensions

The PCB layout footprint for the SKY85703-11 is shown in Figure 5. Typical case markings are shown in Figure 6. Package dimensions for the 16-pin QFN are shown in Figure 7, and tape and reel dimensions are provided in Figure 8.
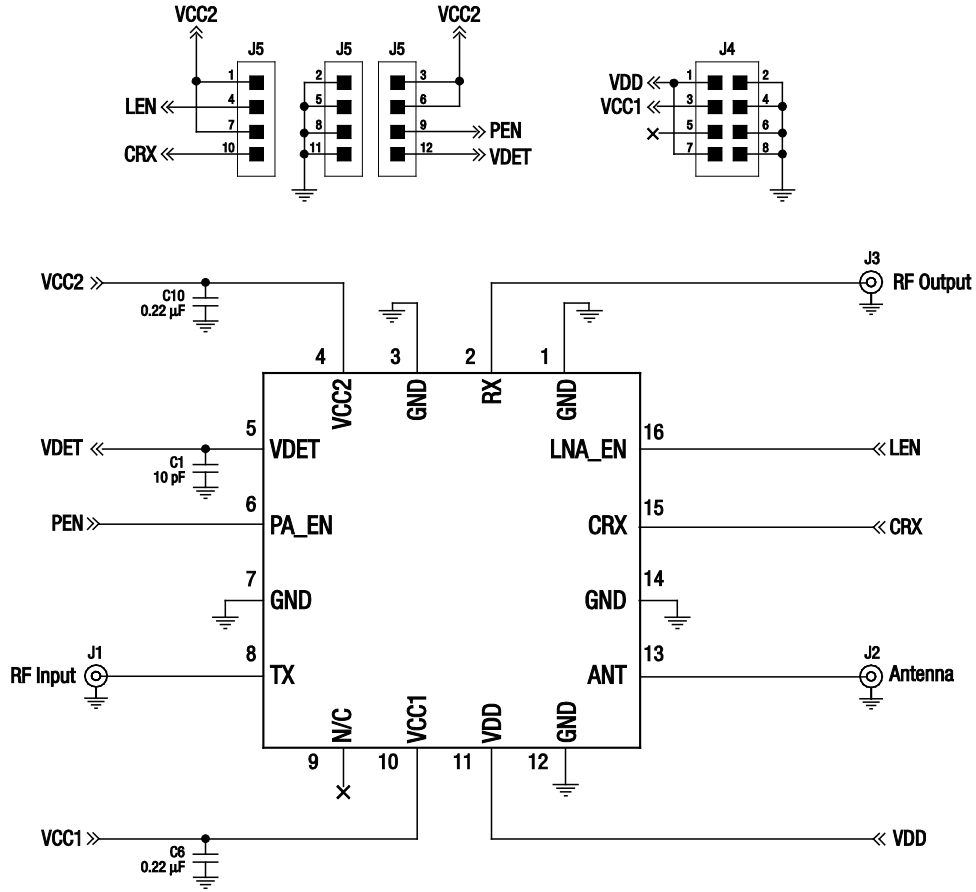
Notes: *0 Ω resistors and DNI components are not shown in schematic.*

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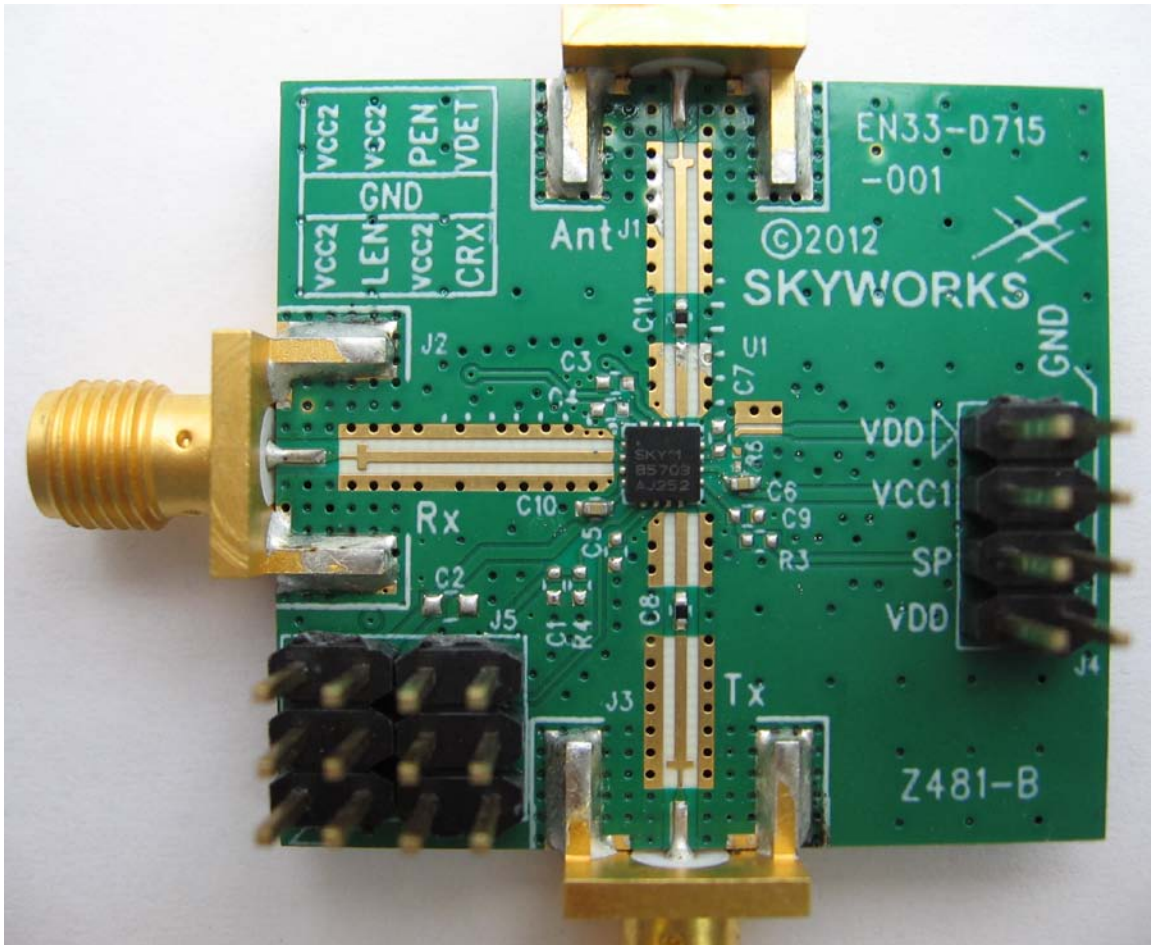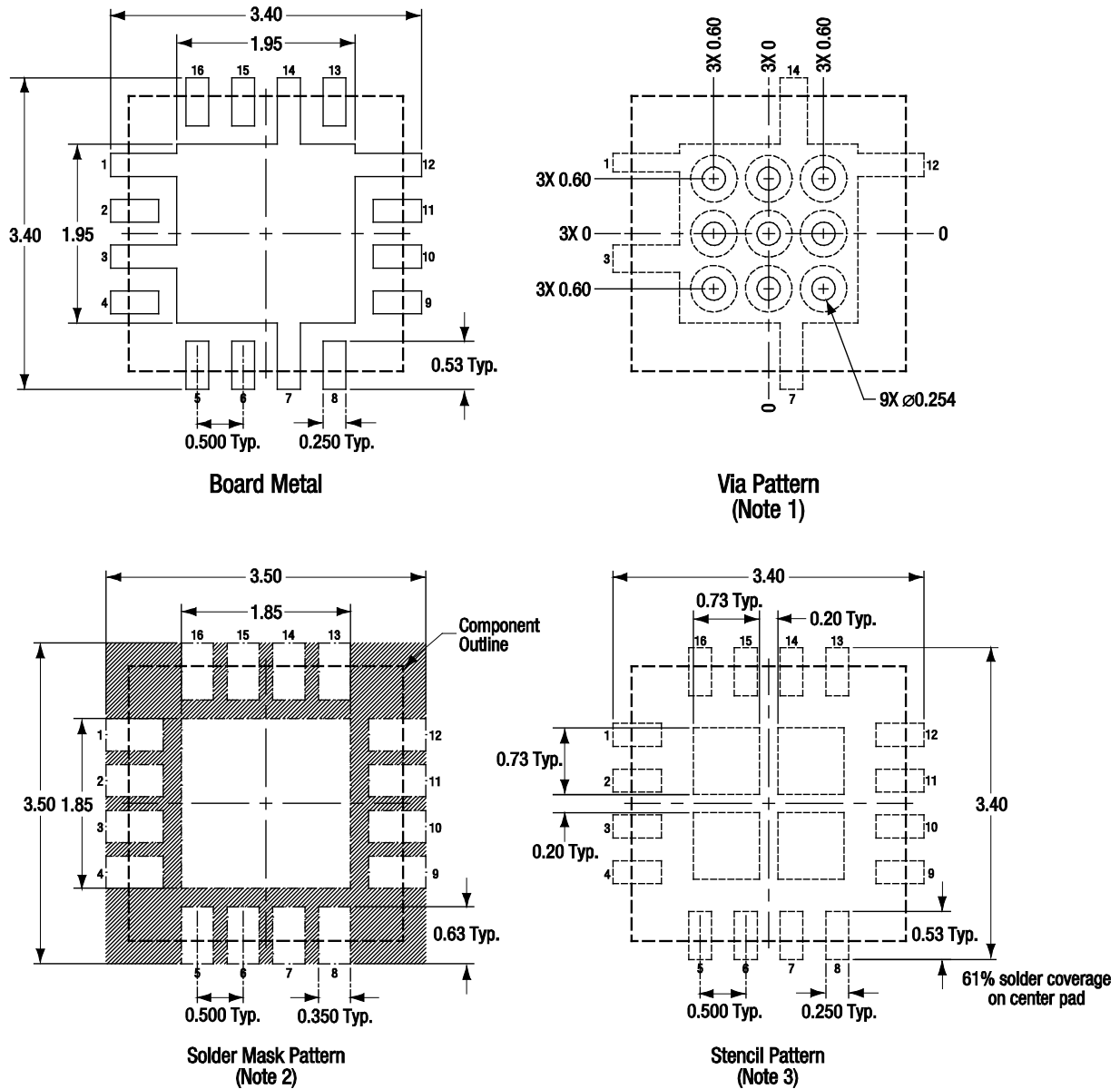
Figure 3. SKY85703-11 Application Schematic

Figure 4. SKY85703-11 Evaluation Board

Table 6. SKY85703-11 Evaluation Board Bill of Materials

Component	Value	Size	Vendor	Part Number	Description
C1	10 pF	0402	Murata	GRM1555C1H100JZ01	Multilayer ceramic
C6, C10	0.22 µF	0402	Murata	GRM155R60J224KE01	Multilayer ceramic
J1, J2, J3					
J4, J5					

Board Metal

Via Pattern
(Note 1)

Solder Mask Pattern
(Note 2)

Stencil Pattern
(Note 3)

NOTES:
1. Via hole recommendations:
        0.025 mm Cu via wall plating (minimum),
        soldermask on the far side should tent
        or plug via holes.
2. Soldermask recommendations:
        Contact board fabricator for recommended
        soldermask offset and tolerance.
3. Stencil recommendations:
        0.125 mm stencil thickness, laser cut apertures,
        trapezoidal walls and rounded corners offer
        better paste release.

Dimension and tolerancing according to ASME Y14.5M-1994.
Unless specified, dimensions are symmetrical about center lines.
All dimensions are in millimeters.

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Figure 5. SKY85703-11 PCB Layout Footprint
(Top View)
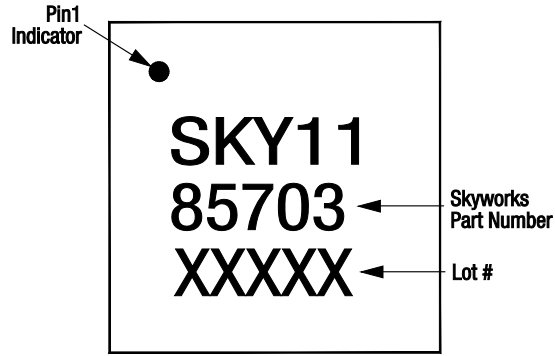
Figure 6. Typical Case Markings
(Top View)

Figure 7. SKY85703-11 16-Pin QFN Package Dimensions
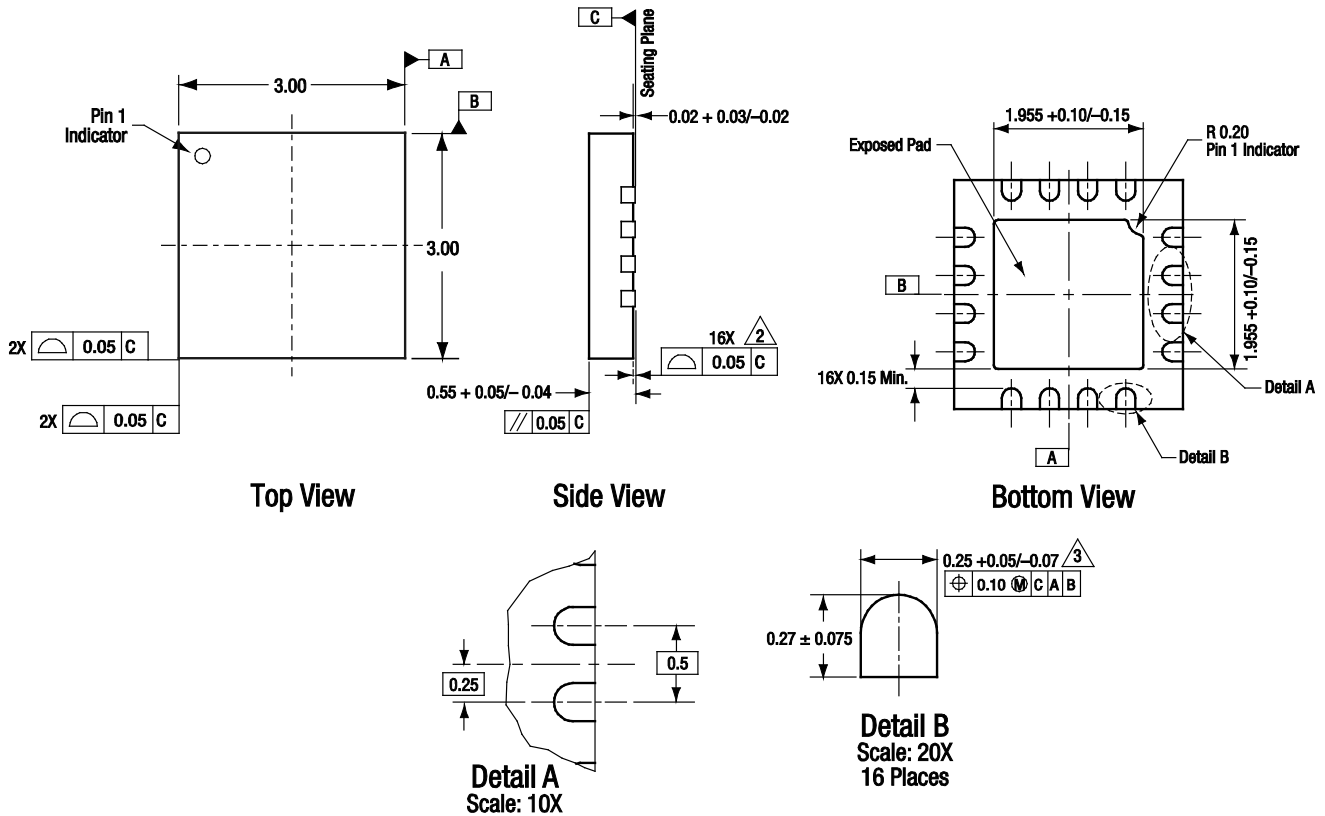
All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Coplanarity applies to the exposed heat sink slug as well as the terminals.

S1977a

0.30 ± 0.05 (T)

∅1.55 ± 0.05 (Do)

P2
2.00 ± 0.1 (Note 1)

Po
4.00 ± 0.1 (Note 2)

E1
1.75 ± 0.1

Pin 1 Location

3.30 ± 0.1 (Bo)

∅1.5 Min. (D1)

A

5.50 ± 0.1 (Note 1)

12.00 ± 0.3

Ref. 3°

0.80 ± 0.1 (Ko)

8.00 ± 0.1 (P1)

3.30 ± 0.1 (Ao)

Section Y-Y

Ref. R0.6

Ref. R0.35

Ref. R0.50

Detail A
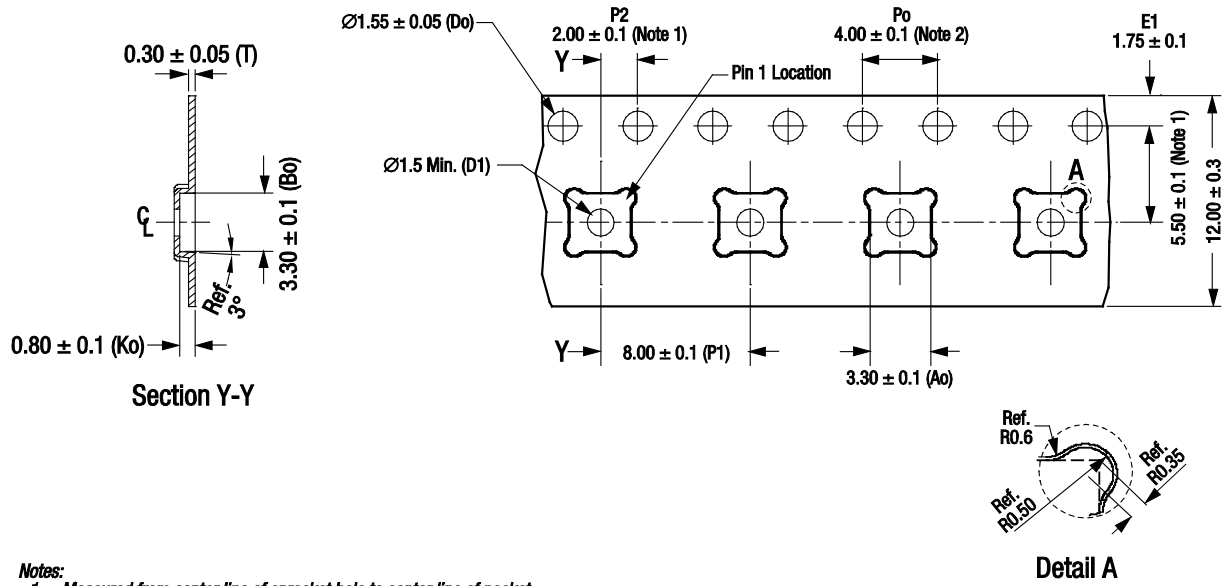
Notes:
1. *Measured from center line of sprocket hole to center line of pocket.*
2. *Cumulative toelrance of 10 sprocket holes is ± 0.20 mm.*
3. *Other material available.*
4. *Typical ESD surface resistivity is from 10^5 to 10^{11} Ohms/square per EIA, JEDEC tape and reel specification.*

All measurements are in millimeters.

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Figure 8. SKY85703-11 Tape and Reel Dimensions

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Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY85703-11 5 GHz WLAN Front-End Module	SKY85703-11	SKY85703-EK1