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6435 PDFN5X6-8L

P-Channel Enhancement Mode Power MOSFET

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客户确认：

公司签章：

部门

工程部

品保部

采购部

签名

日期



6435 30V P-Channel MOSFET

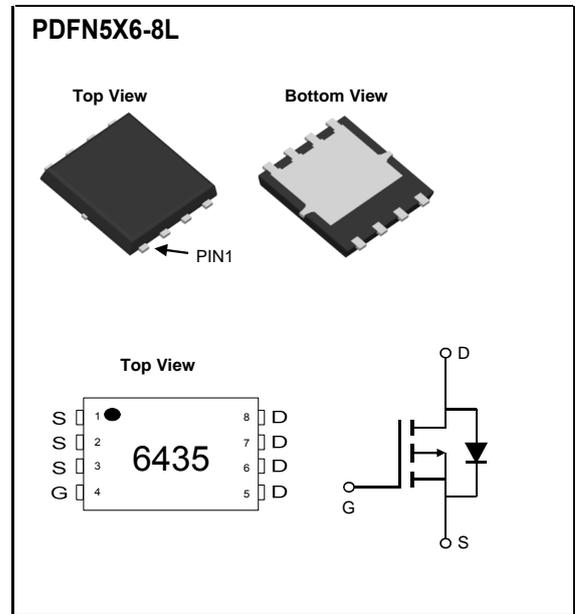
V _{(BR)DSS}	R _{DS(on)MAX}	I _D
-30V	0.012Ω@-10V	-34 A
	0.020Ω@-5.0V	

General FEATURE

- TrenchFET Power MOSFET
- Lead free product is acquired
- Surface mount package

APPLICATION

- Load Switch for Portable Devices
- DC/DC Converter



Absolute Maximum Ratings T _A =25°C unless otherwise noted			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	±25	V
Continuous Drain Current	I _D	T _C =25°C	-34
		T _C =100°C	-21.5
Pulsed Drain Current ^C	I _{DM}	-95	A
Continuous Drain Current	I _{DSM}	T _A =25°C	-12
		T _A =70°C	-10
Avalanche Current ^C	I _{AS}	24	A
Avalanche energy L=0.1mH ^C	E _{AS}	29	mJ
Power Dissipation ^B	P _D	T _C =25°C	31
		T _C =100°C	12.5
Power Dissipation ^A	P _{DSM}	T _A =25°C	4.1
		T _A =70°C	2.6
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter	Symbol	Typ	Max	Units	
Maximum Junction-to-Ambient ^A	R _{θJA}	24	30	t ≤ 10s	°C/W
Maximum Junction-to-Ambient ^{A D}				Steady-State	53
Maximum Junction-to-Case	R _{θJC}	3.4	4	Steady-State	°C/W

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Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}, V_{GS}=0\text{V}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30\text{V}, V_{GS}=0\text{V}$			-1	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 25\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1.7	-2.3	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}, V_{DS}=-5\text{V}$	-95			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}, I_D=-20\text{A}$		12	15	$\text{m}\Omega$
		$V_{GS}=-5\text{V}, I_D=-15\text{A}$		20	25	Ω
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}, I_D=-20\text{A}$		28		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}, V_{GS}=0\text{V}$		-0.73	-1	V
I_S	Maximum Body-Diode Continuous Current				-35	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=-15\text{V}, f=1\text{MHz}$		1130	1400	pF
C_{oss}	Output Capacitance			240		pF
C_{rss}	Reverse Transfer Capacitance			155		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		5.8	8	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=-10\text{V}, V_{DS}=-15\text{V}, I_D=-20\text{A}$		21		nC
$Q_g(4.5\text{V})$	Total Gate Charge			10		nC
Q_{gs}	Gate Source Charge			4		nC
Q_{gd}	Gate Drain Charge			6		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=-10\text{V}, V_{DS}=-15\text{V}, R_L=0.75\Omega, R_{GEN}=3\Omega$		10		ns
t_r	Turn-On Rise Time			8		ns
$t_{D(off)}$	Turn-Off Delay Time			15		ns
t_f	Turn-Off Fall Time			7		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-20\text{A}, dI/dt=500\text{A}/\mu\text{s}$		13.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-20\text{A}, dI/dt=500\text{A}/\mu\text{s}$		29		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$. Maximum UIS current limited by test equipment.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

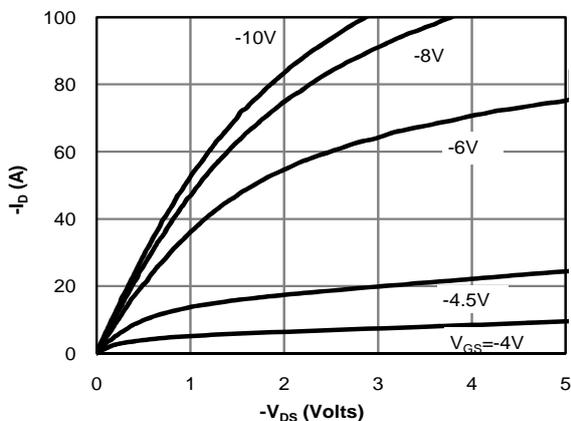


Fig 1: On-Region Characteristics (Note E)

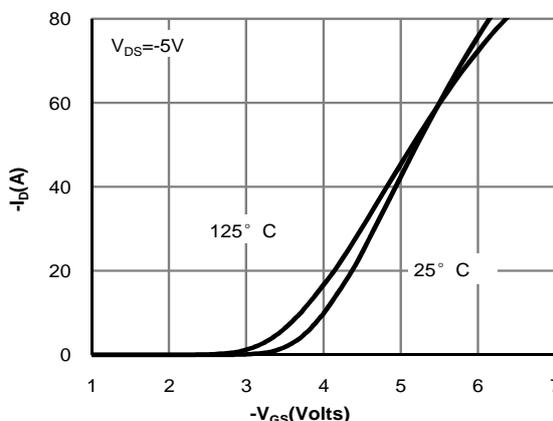


Figure 2: Transfer Characteristics (Note E)

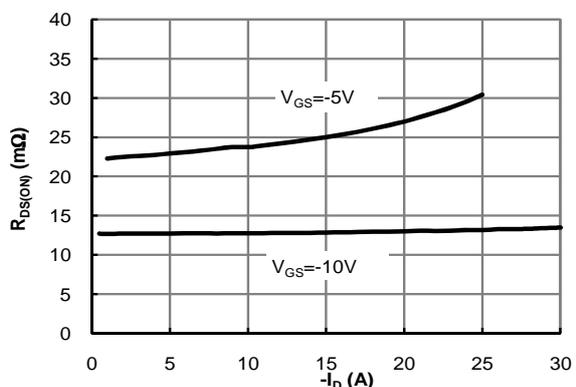


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

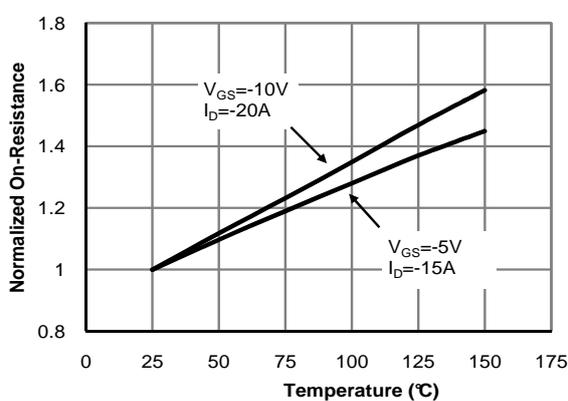


Figure 4: On-Resistance vs. Junction Temperature (Note E)

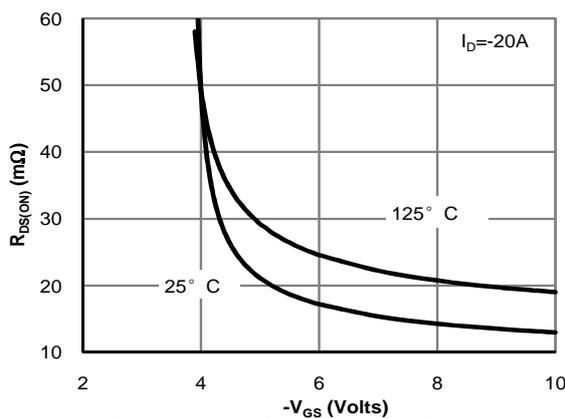


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

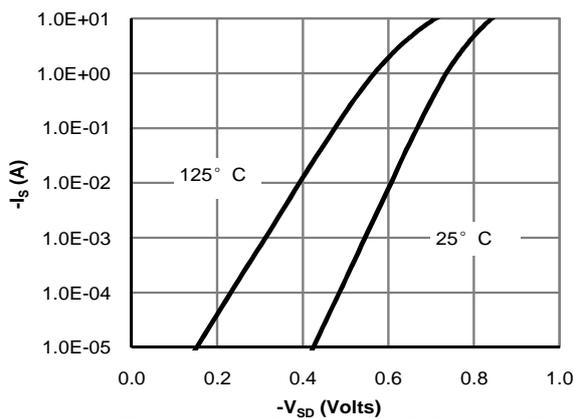


Figure 6: Body-Diode Characteristics (Note E)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

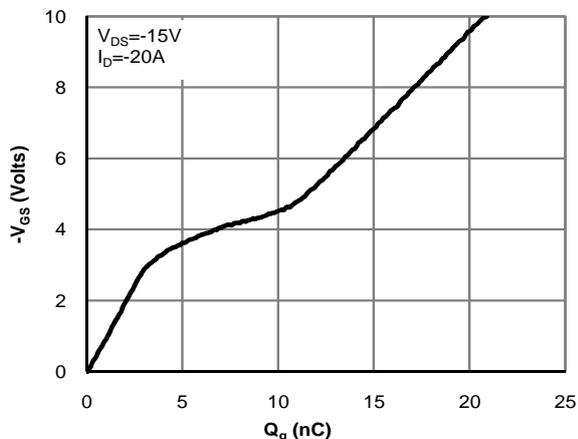


Figure 7: Gate-Charge Characteristics

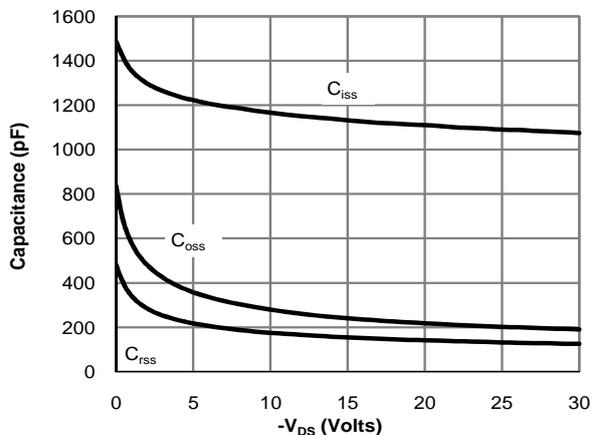


Figure 8: Capacitance Characteristics

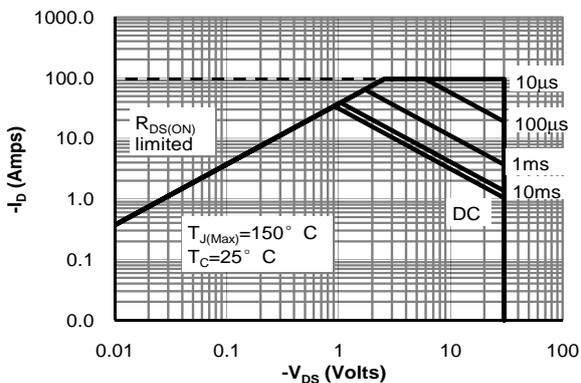


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

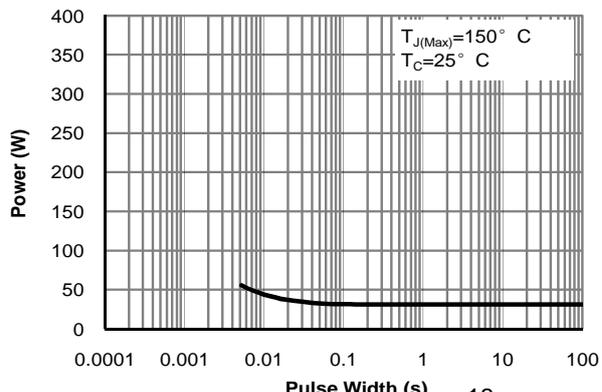


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

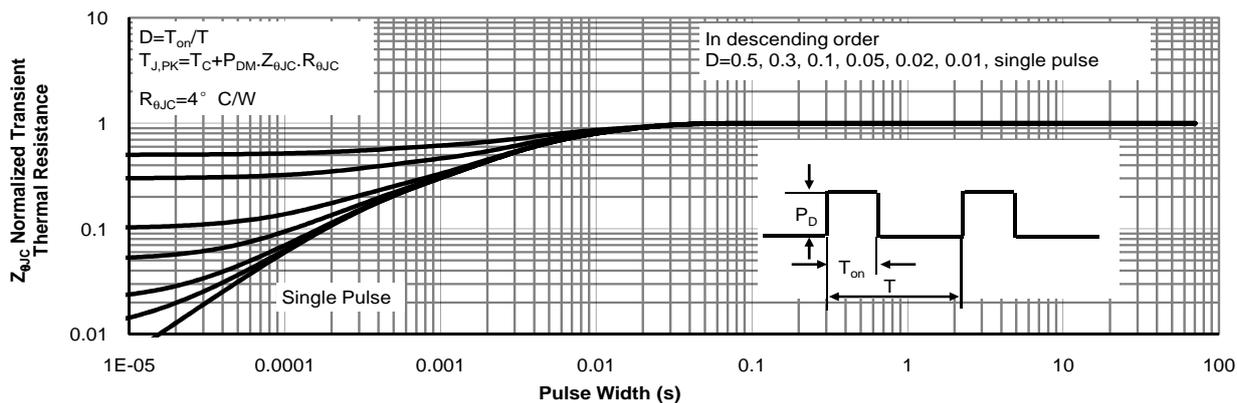


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

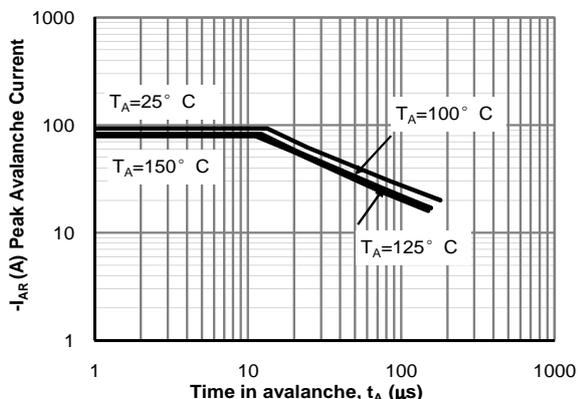


Figure 12: Single Pulse Avalanche capability (Note C)

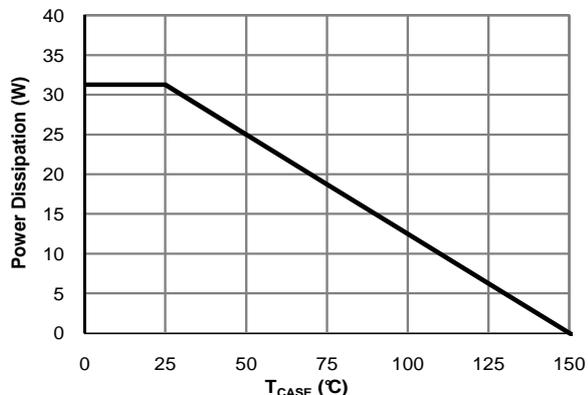


Figure 13: Power De-rating (Note F)

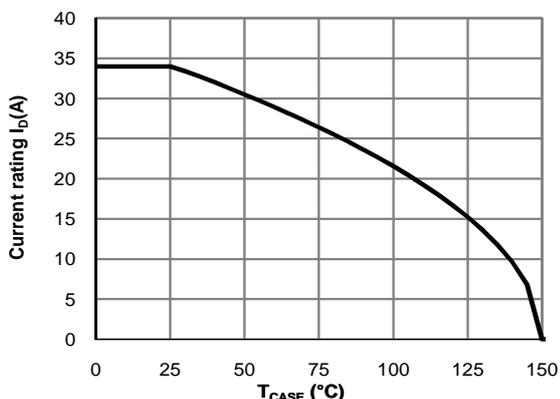


Figure 14: Current De-rating (Note F)

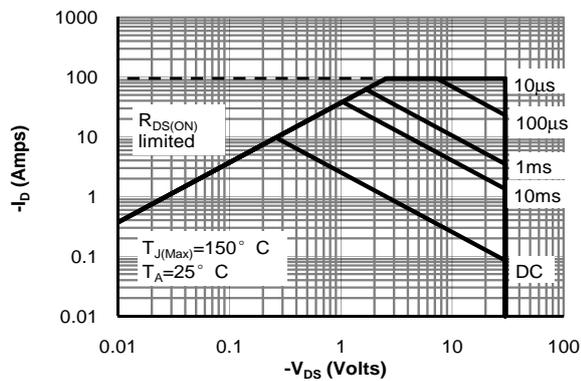


Figure 15: Maximum Forward Biased Safe Operating Area (Note H)

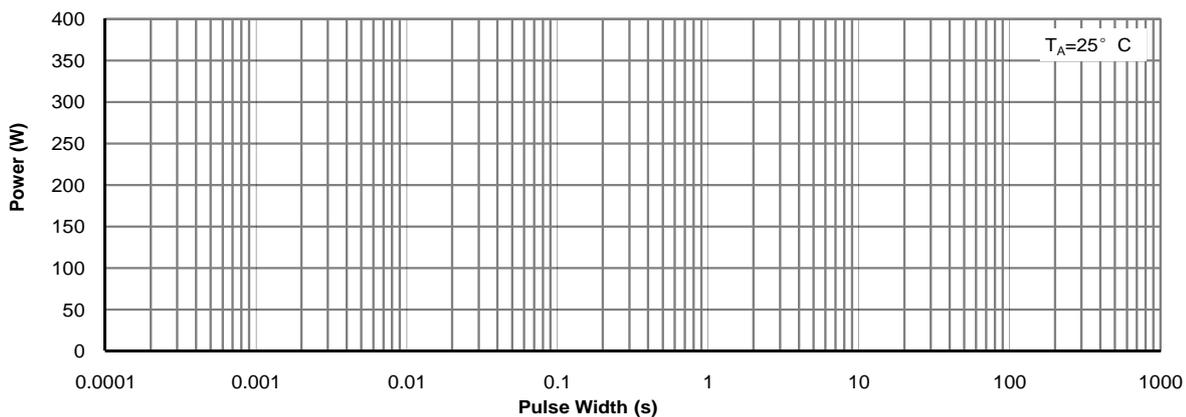
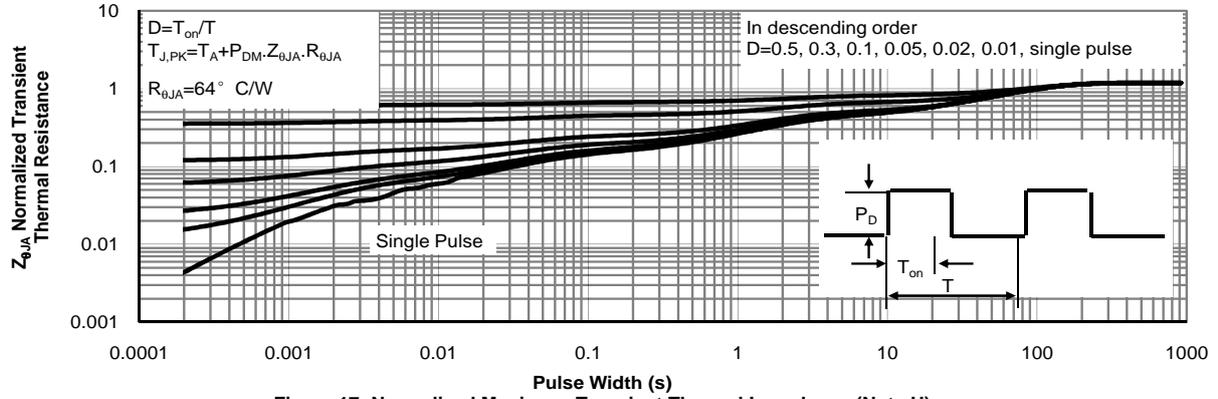


Figure 16: Single Pulse Power Rating Junction-to-Ambient (Note H)

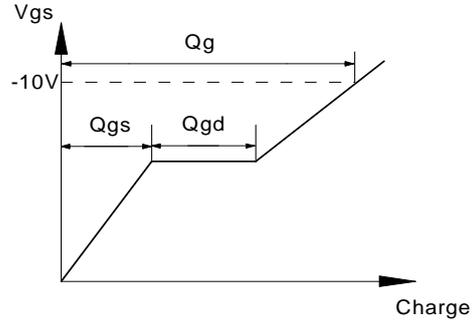
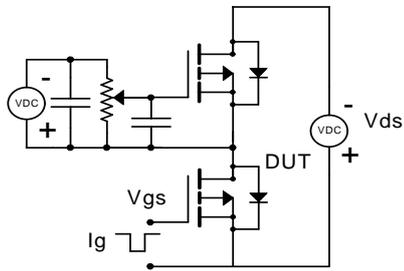
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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

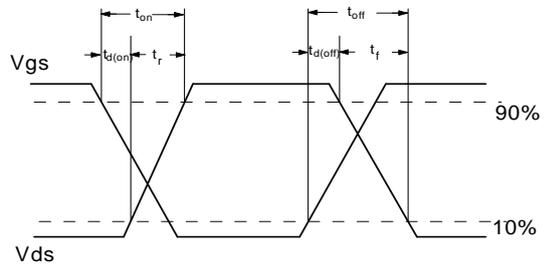
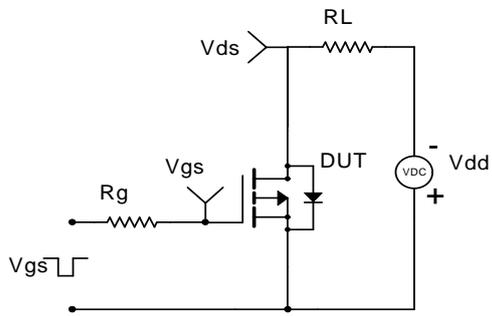


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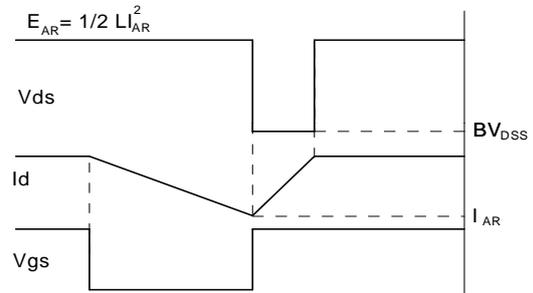
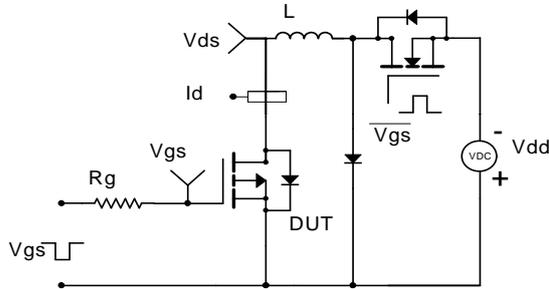
Gate Charge Test Circuit & Waveform



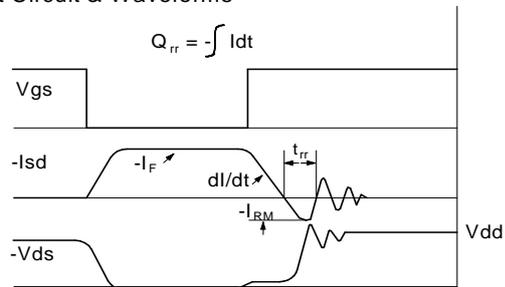
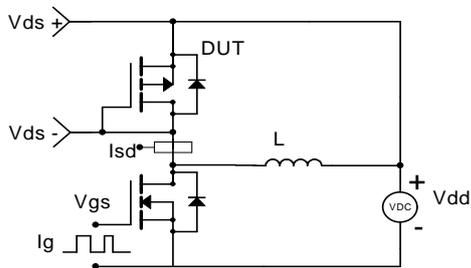
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

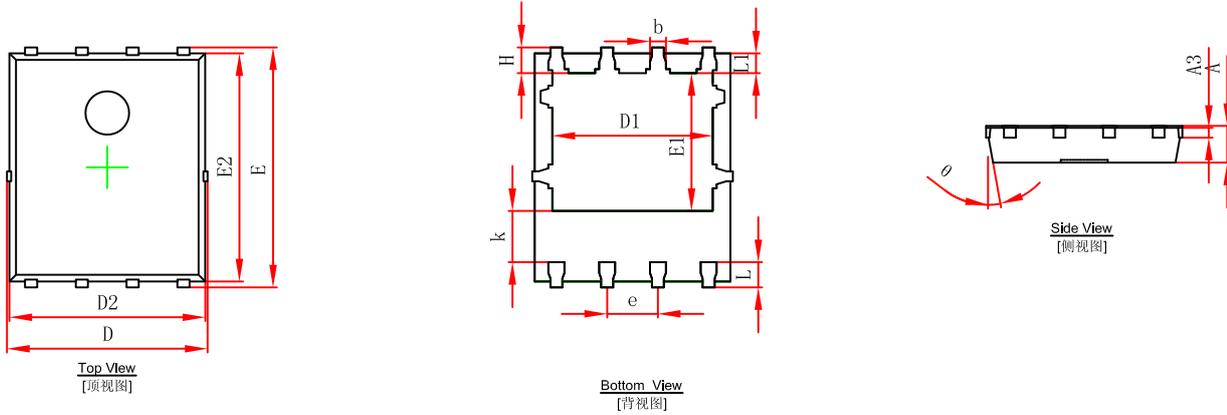


Diode Recovery Test Circuit & Waveforms



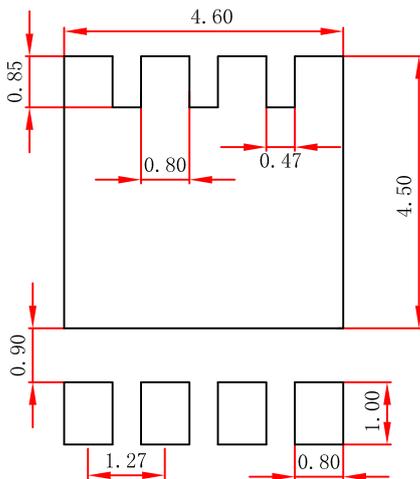
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PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.