Features

- Operating voltage: 2.4V~5.5V
- Multiple LED display − 32 ROW /8 COM and 24 ROW & 16 COM
- Integrated display RAM − select 32 ROW & 8 COM for 64×4 display RAM, or select 24 ROW & 16 COM for 96×4 display RAM
- 16-level PWM brightness control
- Integrated 256kHz RC oscillator
- Serial MCU interface − $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, DATA
- Data mode & command mode instruction
- Cascading function for extended applications
- Selectable NMOS open drain output driver and PMOS open drain output driver for commons
- 48/52-pin LQFP package

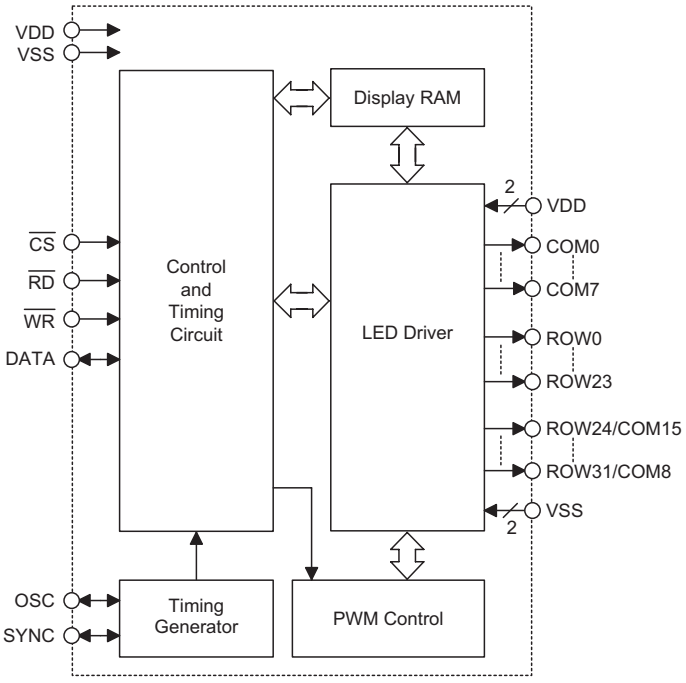
Applications

- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Other consumer application
- LED Displays

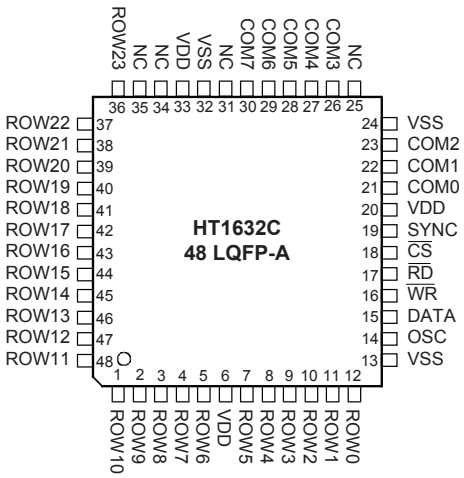
General Description

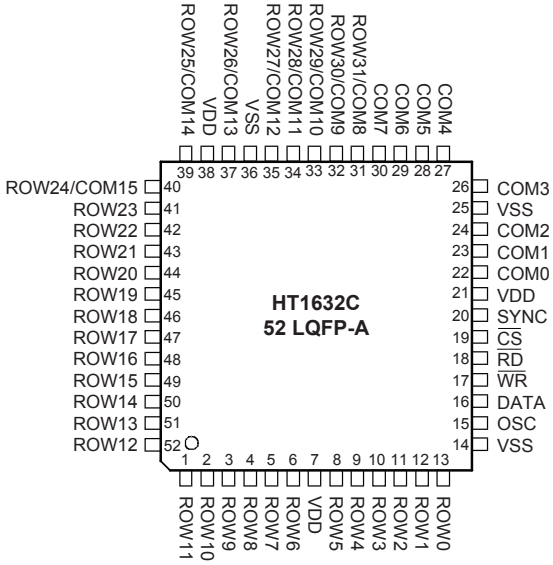
The HT1632C is a memory mapping LED display controller/driver, which can select a number of ROW and commons. These are 32 ROW & 8 Commons and 24 ROW & 16 Commons. The device supports 16-gradation LEDs for each out line using PWM control with software instructions. A serial interface is conveniently provided for the command mode and data mode. Only three or four lines are required for the interface between the host controller and the HT1632C. The display can be extended by cascading the HT1632C for wider applications.

Block Diagram



Pin Assignment





Note: When the 48-pin LQFP is selected, this device does not support 1/16 duty.

Pin Description

Pad Name	I/O	Description
ROW0~ROW23	O	Line drivers. These pins drive the LEDs.
ROW24/COM15~ ROW31/COM8	O	Drive LED outputs or common outputs. Each COM pin is double bonded.
COM0~COM7	O	Common outputs. Each COM pin is double bonded.
SYNC	I/O	If the RC Master Mode or EXT CLK Master Mode command is programmed, the synchronous signal is output to SYN pin. If the Slave Mode command is programmed, the synchronous signal is input from SYN pin.
OSC	I/O	If the RC Master Mode command is programmed, the system clock source is from on-chip RC oscillator and system clock is output to OSC pin. If the Slave Mode or EXT CLK Master Mode command is programmed, the system clock source is input from external clock via the OSC pin.
DATA	I/O	Serial data input or output with pull-high resistor
$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA lines are latched into the HT1632C on the rising edge of the $\overline{WR}$ signal.
$\overline{RD}$	I	READ clock input with pull-high resistor. The HT1632C RAM data is clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
$\overline{CS}$	I	Chip select input with pull-high resistor When the $\overline{CS}$ line is high, the data and command read from or written to the HT1632C is disabled, and the serial interface circuit is also reset. If $\overline{CS}$ is low, the data and command transmission between the host controller and the HT1632C are all enabled.
VSS	—	Negative power supply, ground. In the PCB layout, all VSS pins should be connected to the GND plane.
VDD	—	Positive power supply. In the PCB layout, all VDD pins should be connected to the power plane.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+6.0V
Operating Temperature .....−40°C to 85°C
Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V
Storage Temperature .....−50°C to 125°C
Max Junction Temperature (Tj) ..... 125°C

Package	Conditions	52LQFP	48LQFP
Thermal Resistance (Rth) θja (°C/W)		54.61	60
Power Dissipation (PD) (W)	Ta=25°C	1.83	1.67
	Ta=85°C	0.73	0.67

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{DD}=2.4V~5.5V, Ta=25°C (Unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	5.0	5.5	V
I_{DD}	Operating Current	5V	No load, LED ON, on-chip RC oscillator	—	0.3	0.6	mA
I_{STB}	Standby Current	5V	No load, power down mode	—	1.5	3.0	μA
V_{IL}	Input Low Voltage	5V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	$0.3V_{DD}$	V
V_{IH}	Input High Voltage	5V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	$0.7V_{DD}$	—	5	V
I_{OL1}	OSC, SYNC, DATA	5V	V_{OL}=0.5V	18	25	—	mA
I_{OH1}	OSC, SYNC, DATA	5V	V_{OH}=4.5V	-10	-13	—	mA
I_{OL2}	ROW Sink Current	5V	V_{OL}=0.5V	12	16	—	mA
I_{OH2}	ROW Source Current	5V	V_{OH}=4.5V	-50	-70	—	mA
I_{OL3}	COM Sink Current	5V	V_{OL}=0.5V	250	350	—	mA
I_{OH3}	COM Source Current	5V	V_{OH}=4.5V	-45	-60	—	mA
R_{PH}	Pull-high Resistor	5V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	18	27	40	kΩ

A.C. Characteristics

V_{DD}=2.4V~5.5V, Ta=25°C (Unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS}	System Clock	5V	On-chip RC oscillator	230	256	282	kHz
f_{LED}	LED Duty Cycle & Frame Frequency	5V	1/8 duty	—	f_{SYS}/2624	—	Hz
			1/16 duty	—	f_{SYS}/2624	—	Hz
f_{CLK1}	Serial Data Clock ($\overline{WR}$ pin)	5V	Duty cycle 50%	—	—	1	MHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ pin)	5V	Duty cycle 50%	—	—	500	kHz
t_{CS}	Serial Interface Reset Pulse Width	—	$\overline{CS}$	250	—	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width	5V	Write mode	0.5	—	—	μs
			Read mode	1.0	—	—	
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	—	—	50	100	ns
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	—	—	50	100	—	ns
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$, Clock Width (Figure 2)	—	—	100	200	—	ns
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$, Clock Width (Figure 3)	—	—	200	300	—	ns
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$, Clock Width (Figure 3)	—	—	100	200	—	ns
t_{od}	Data Output Delay Time (Figure 4)	—	—	—	100	200	ns

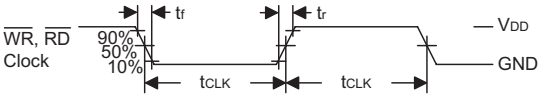


Figure 1

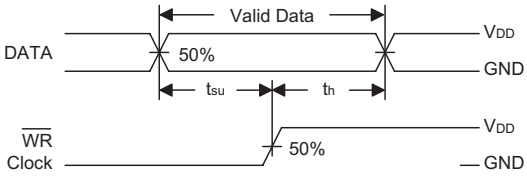


Figure 2

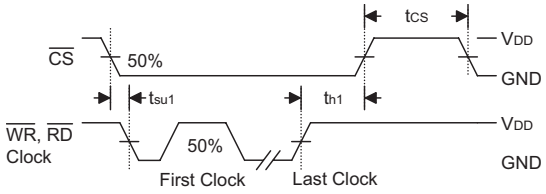


Figure 3

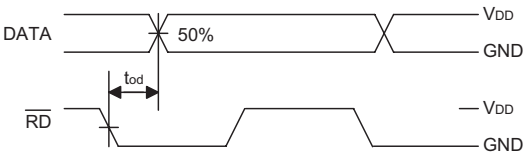


Figure 4

Functional Description

Display Memory − RAM

The static display memory (RAM) is organized into 64×4 bits or 96×4 bits and is used to store the display data. If 32 ROW & 8 COM is selected, the RAM size is 64×4 bits. If 24 ROW & 16 COM is selected, the RAM size is 96×4 bits. The contents of the RAM are directly mapped to the contents of the LED driver. If the data in RAM is set to ″1″, the corresponding LED will be lighted. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The contents of the RAM can be read or written from bit 0 of the specific address. The following is a mapping from the RAM to the LED pattern:

	COM7	COM6	COM5	COM4		COM3	COM2	COM1	COM0	
ROW0					01H					00H
ROW1					03H					02H
ROW2					05H					04H
ROW3					07H					06H
ROW4					09H					08H
ROW5					0BH					0AH
ROW6					0DH					0CH
ROW7					0FH					0EH
ROW8					11H					10H
ROW9					13H					12H
ROW10					15H					14H
ROW11					17H					16H
ROW12					19H					18H
ROW13					1BH					1AH
ROW14					1DH					1CH
ROW15					1FH					1EH
ROW16					21H					20H
ROW17					23H					22H
ROW18					25H					24H
ROW19					27H					26H
ROW20					29H					28H
ROW21					2BH					2AH
ROW22					2DH					2CH
ROW23					2FH					2EH
ROW24					31H					30H
ROW25					33H					32H
ROW26					35H					34H
ROW27					37H					36H
ROW28					39H					38H
ROW29					3BH					3AH
ROW30					3DH					3CH
ROW31					3FH					3EH
	D3	D2	D1	D0	Addr. / Data	D3	D2	D1	D0	Addr. / Data

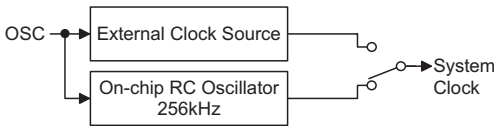
32 ROW & 8 COM for 64×4 Display RAM

	COM15	COM14	COM13	COM12		.....	COM3	COM2	COM1	COM0	
ROW0					03H	.....					00H
ROW1					07H						04H
ROW2					0BH						08H
ROW3					0FH						0CH
ROW4					13H						10H
ROW5					17H						14H
ROW6					1BH						18H
ROW7					1FH						1CH
ROW8					23H						20H
ROW9					27H						24H
ROW10					2BH						28H
ROW11					2FH						2CH
ROW12					33H						30H
ROW13					37H						34H
ROW14					3BH						38H
ROW15					3FH						3CH
ROW16					43H						40H
ROW17					47H						44H
ROW18					4BH						48H
ROW19					4FH						4CH
ROW20					53H						50H
ROW21					57H						54H
ROW22					5BH						58H
ROW23					5FH	.....					5CH
	D3	D2	D1	D0	Addr. / Data		D3	D2	D1	D0	Addr. / Data

24 ROW & 16 COM for 96×4 Display RAM

System Oscillator

The HT1632C system clock is used to generate the time base clock frequency, LED-driving clock. The clock may be sourced from an on-chip RC oscillator (256kHz), or an external clock using the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LED duty cycle generator will turn off. This command is, however, available only for the on-chip RC oscillator. Once the system clock stops, the LED display will become blank, and the time base will also lose its function. The LED OFF command is used to turn the LED duty cycle generator off. After the LED duty cycle generator switches off by issuing the LED OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor execute the power down mode. The crystal oscillator option can be applied to connect an external frequency source to the OSC pin. In this case, the system fails to enter the power down mode, similar to the case in the external clock source operation. At the initial system power on, the HT1632C is in the SYS DIS state.



System Oscillator Configuration

LED Driver

The HT1632C has a 256 (32×8) and 384 (24×16) pattern LED driver. It can be configured in a 32×8 or 24×16 pattern and common pad N-MOS open drain output or P-MOS open drain output LED driver using the S/W configuration. This feature makes the HT1632C suitable for multiple LED applications. The LED-driving clock is derived from the system clock. The driving clock frequency is always 256kHz, an on-chip RC oscillator frequency, or an external frequency. The LED corresponding commands are summarized in the table. The bold form of 1 0 0, namely 1 0 0, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The LED OFF command turns the LED display off by disabling the LED duty cycle generator. The LED ON command, on the other hand, turns the LED display on by enabling the LED duty cycle generator.

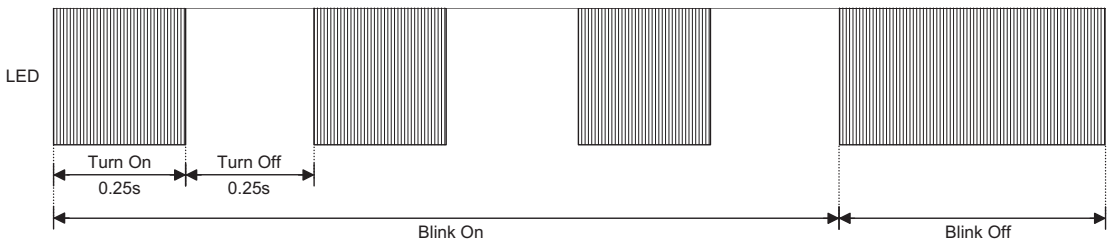
Name	Command Code	Function
LED OFF	**100**00000010X	Turn off LED outputs
LED ON	**100**00000011X	Turn on LED outputs
Commons Option	**100**0010abXXX	ab=00: N-MOS open drain output and 8 common option ab=01: N-MOS open drain output and 16 common option ab=10: P-MOS open drain output and 8 common option ab=11: P-MOS open drain output and 16 common option

Cascade Operation

For the cascade operation, the first IC is set to master mode and its SYNC and OSC pins are set to output pins. The second IC is set to slave mode and its SYNC and OSC pins are set to input pins which are connected to the the master IC. Please refer to the ″Cascade control flow chart″ for detail settings.

Blinker

The HT1632C has display blinking capabilities. The blink function generates all LED blinking. The blink rates is 0.25s LED on and 0.25s LED off for one blinking period . This blinking function can be effectively performed by setting the BLINK ON or BLINK OFF command.



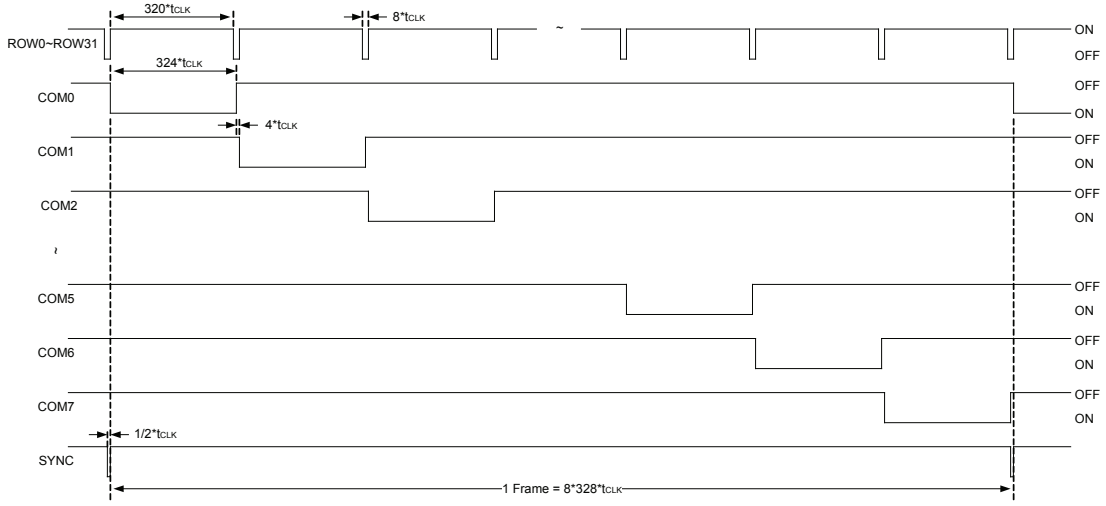
Example of Waveform for Blinker

Command Format

The S/W setting can configure the HT1632C. There are two mode commands to configure the HT1632C resources and to transfer the LED display data. The configuration mode of the HT1632C is knows as the command mode,with a command mode ID of 1 0 0. The command mode consists of a system configuration command, a system frequency selection command, a LED configuration command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations.

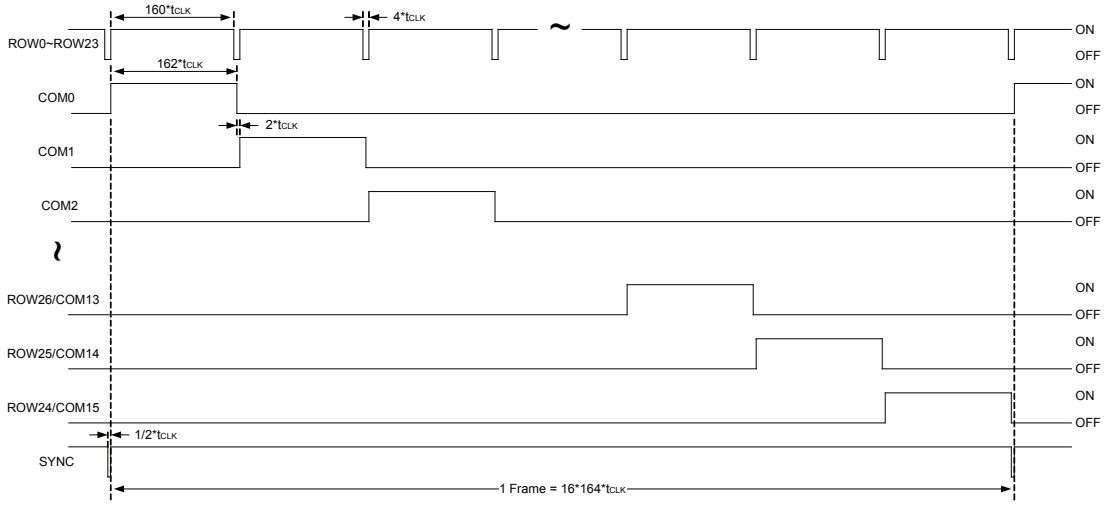
LED Driver Mode Output Waveform

N-MOS Open Drain of 32×8 Driver Mode



Note: $t_{CLK}=1/f_{SYS}$

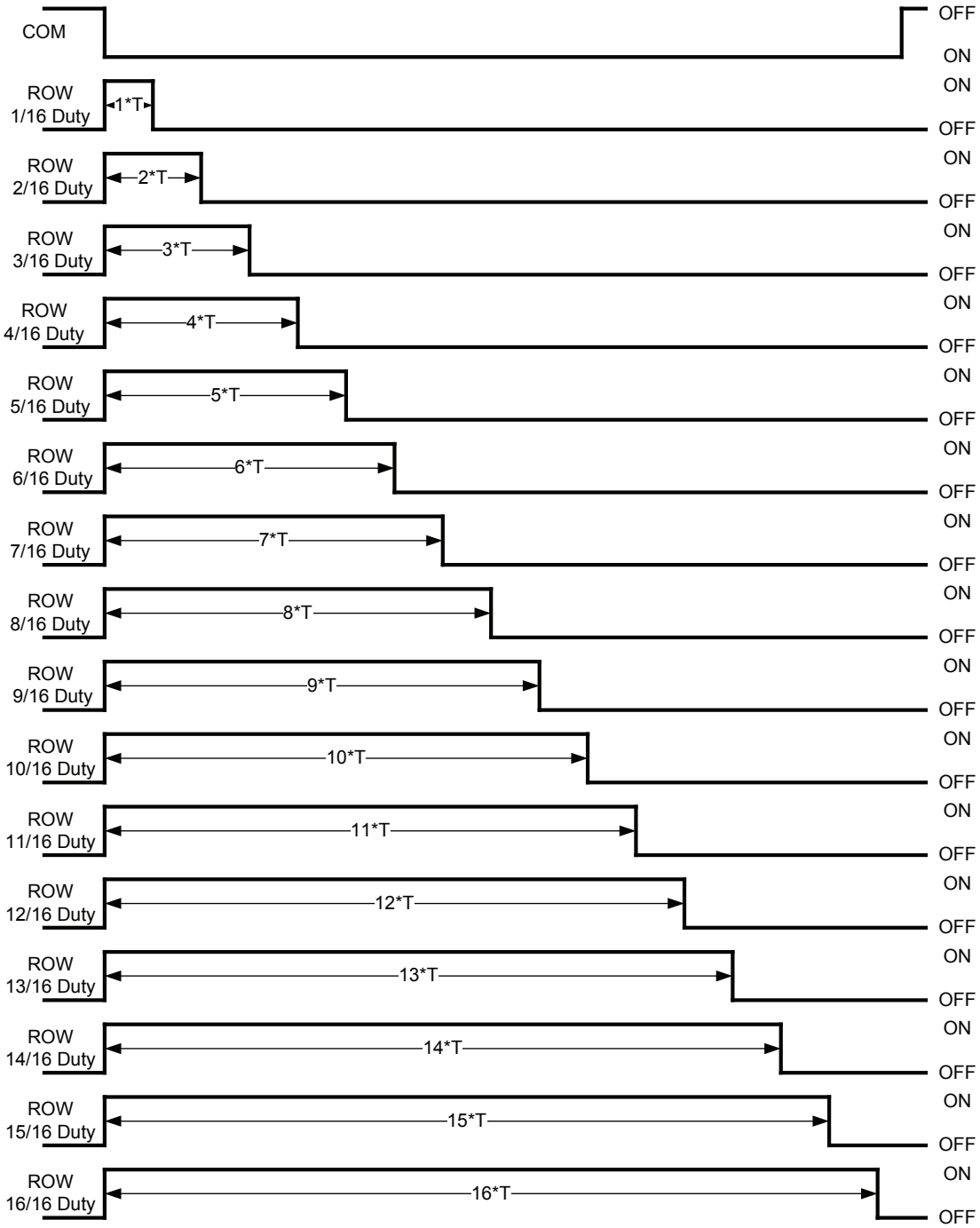
P-MOS Open Drain of 24×16 Driver Mode (COM pin with Transistor Buffer)



Note: $t_{CLK}=1/f_{SYS}$

Digital Dimming

The Display Dimming capabilities of the HT1632C are very versatile. The whole display can be dimmed using pulse width modulation techniques for the ROW driver with the Dimming command. The relationship between ROW and COM digital dimming duty time are shown as below:



Note: (1) $T=20 \times t_{CLK}$ (32×8 driver mode)

(2) $T=10 \times t_{CLK}$ (24×16 driver mode)

(3) $t_{CLK}=1/f_{SYS}$

The following are the data mode ID and the command mode ID:

Operation	Mode	ID
Read	Data	1 1 0
Write	Data	1 0 1
Read-Modify-Write	Data	1 0 1
Command	Command	1 0 0

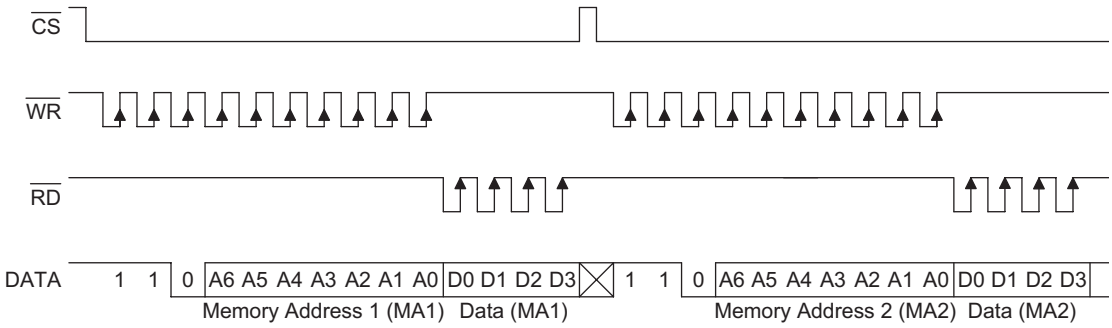
The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 1 0 0, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. Once the $\overline{CS}$ pin returns to "0", a new operation mode ID should be issued first.

Interfacing

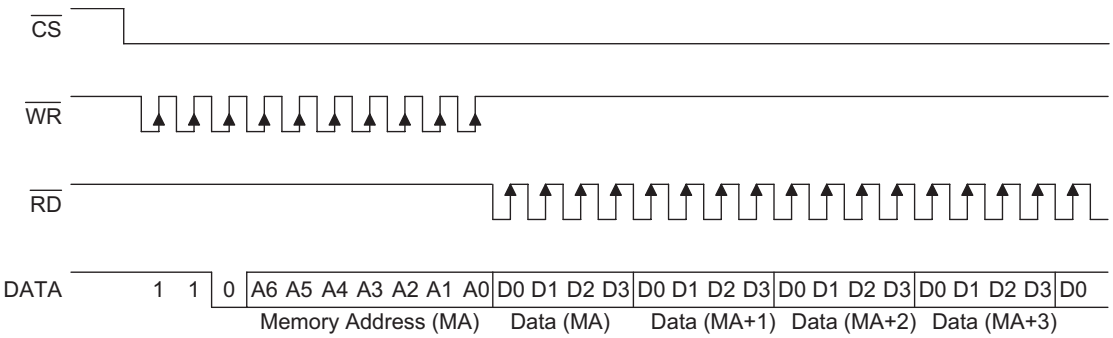
Only four lines are required to interface to the HT1632C. The $\overline{CS}$ line is used to initialise the serial interface circuit and to terminate the communication between the host controller and the HT1632C. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the HT1632C are first disabled and then initialised. Before issuing a mode command or mode switching, a high level pulse is required to initialise the serial interface of the HT1632C. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The $\overline{RD}$ line is the READ clock input. Data in the RAM is clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller reads in the correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the HT1632C on the rising edge of the $\overline{WR}$ signal.

Timing Diagrams

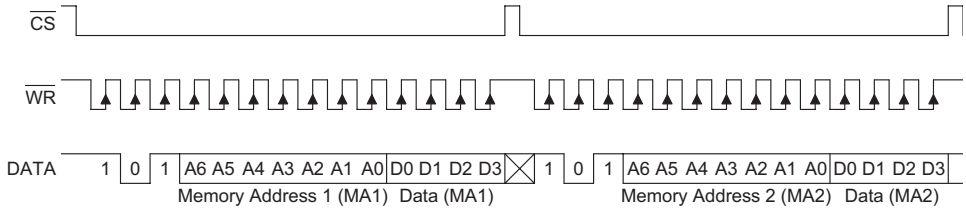
READ Mode − Command Code = 1 1 0



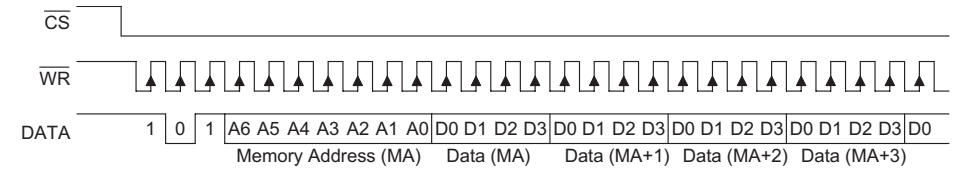
READ Mode − Successive Address Reading



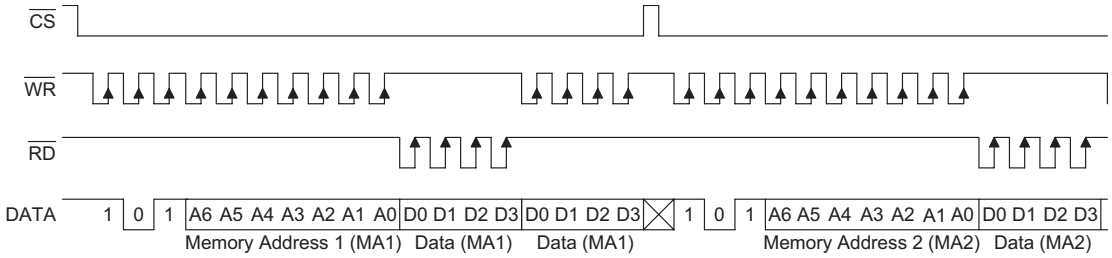
WRITE Mode − Command Code = 1 0 1



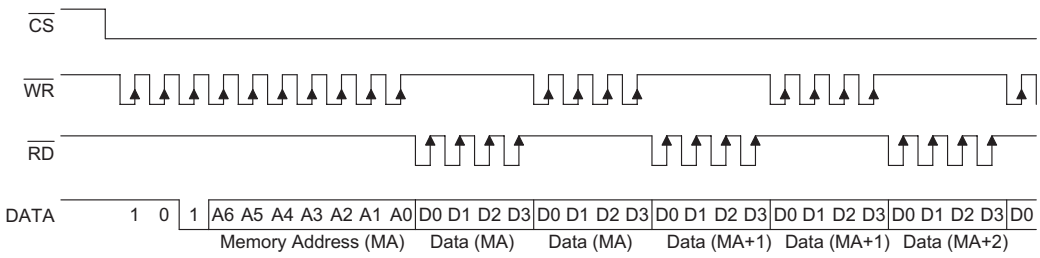
WRITE Mode − Successive Address Writing



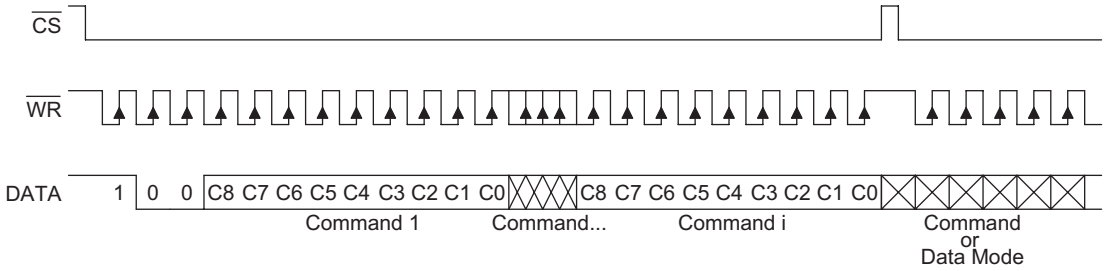
READ-MODIFY-WRITE Mode − Command Code = 1 0 1



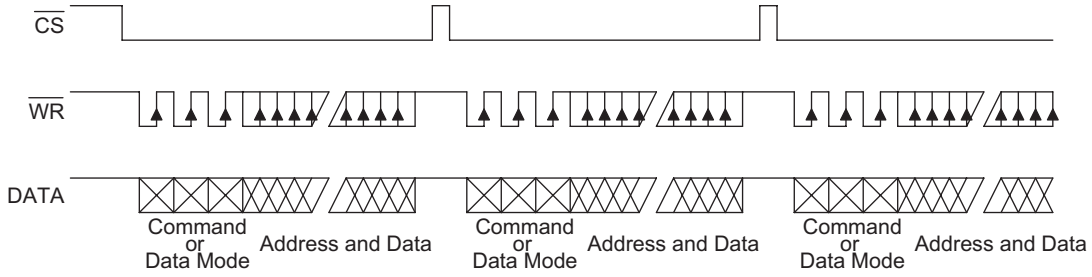
READ-MODIFY-WRITE Mode − Successive Address Accessing



Command Mode − Command Code = 1 0 0



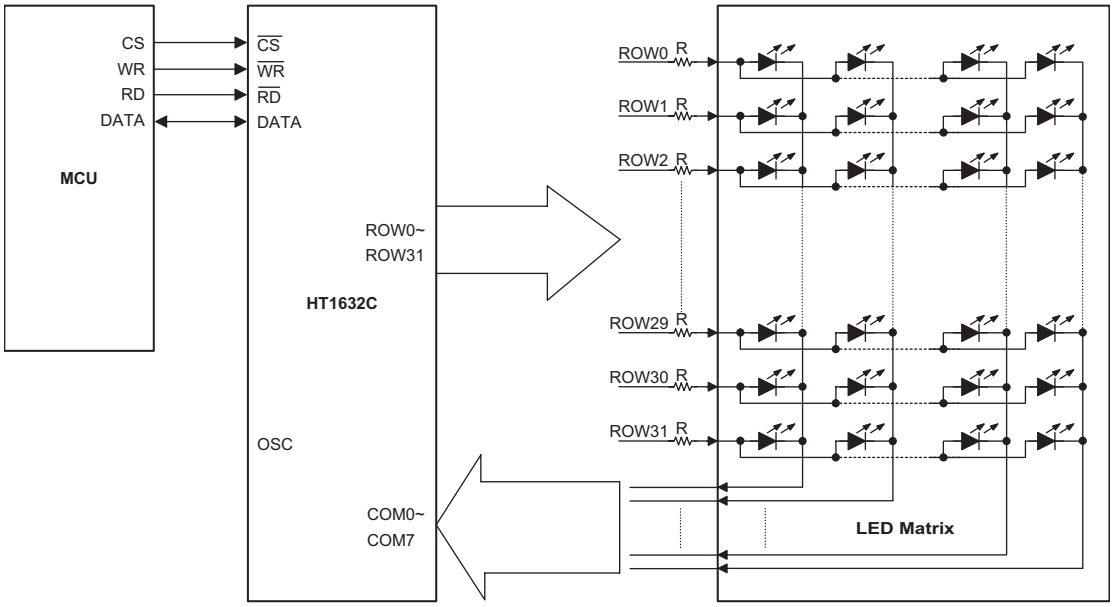
Mode − Data and Command Mode



Application Circuits

Low Power LED Application (Direct Drive)

32 ROW × 8 COM Example: N-MOS open drain output and 8 COM option

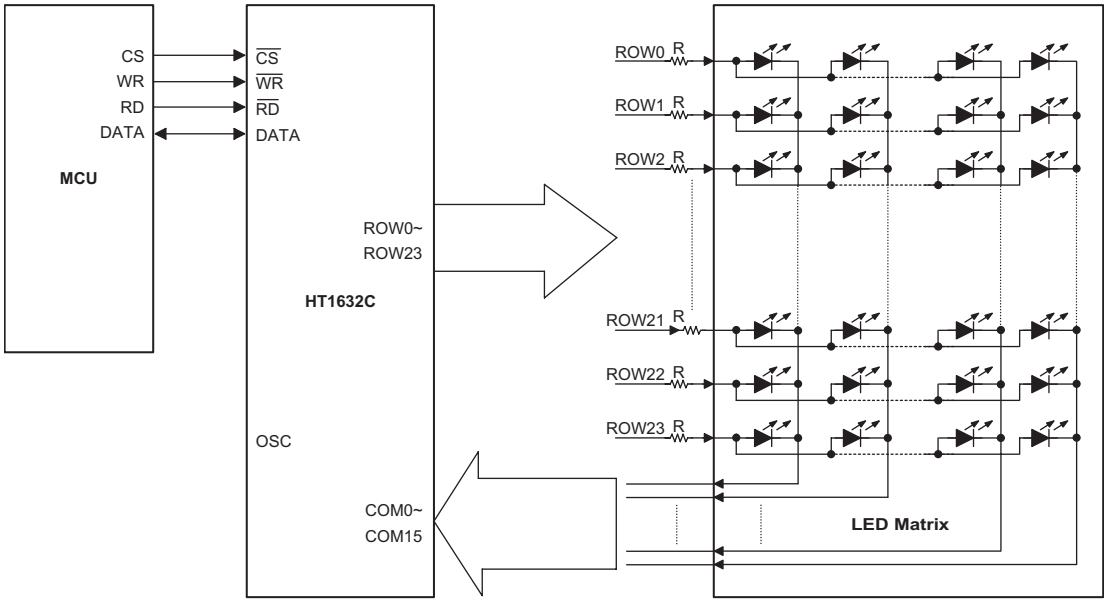


Note: 1.Values of the "R" resistors are selected depending on the power consumption of the LEDs.

2. In the PCB layout all VDD pins should be connected to the power plane.

3. In the PCB layout all VSS pins should be connected to the GND plane.

24 ROW × 16 COM Example: N-MOS open drain output and 16 COM option



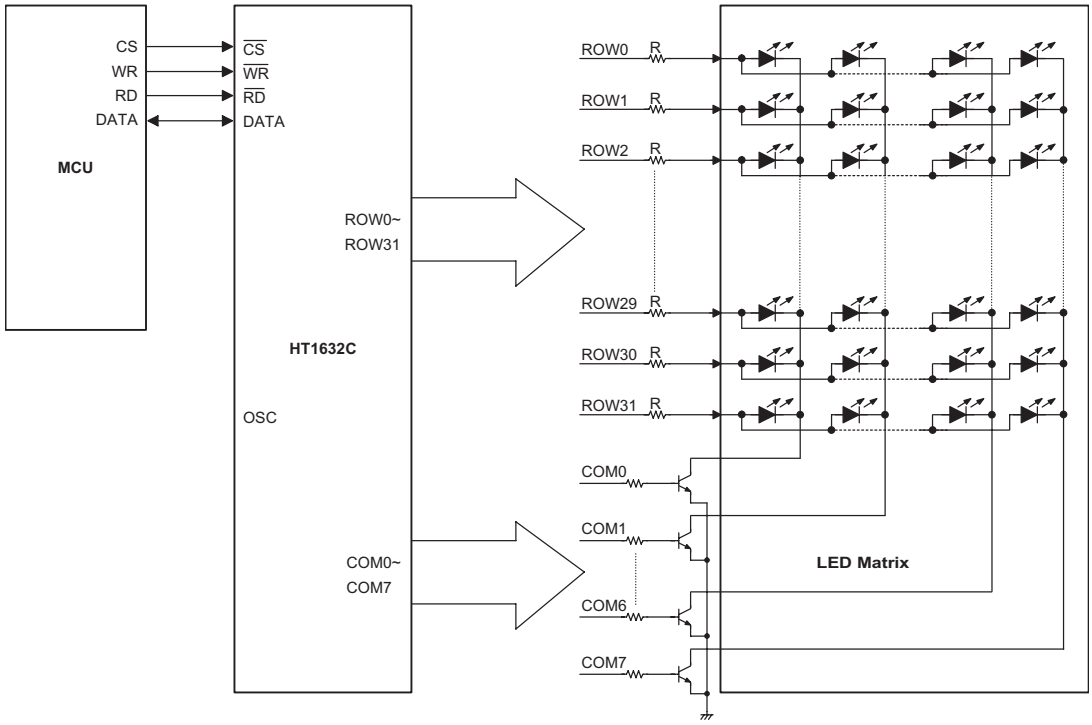
Note: 1. Values of the "R" resistors are selected depending on the power consumption of the LEDs.

2. In the PCB layout all VDD pins should be connected to the power plane.

3. In the PCB layout all VSS pins should be connected to the GND plane.

Middle Power LED Application (COM with Transistor Buffer)

32 ROW × 8 COM Example: P-MOS open drain output and 8 COM option

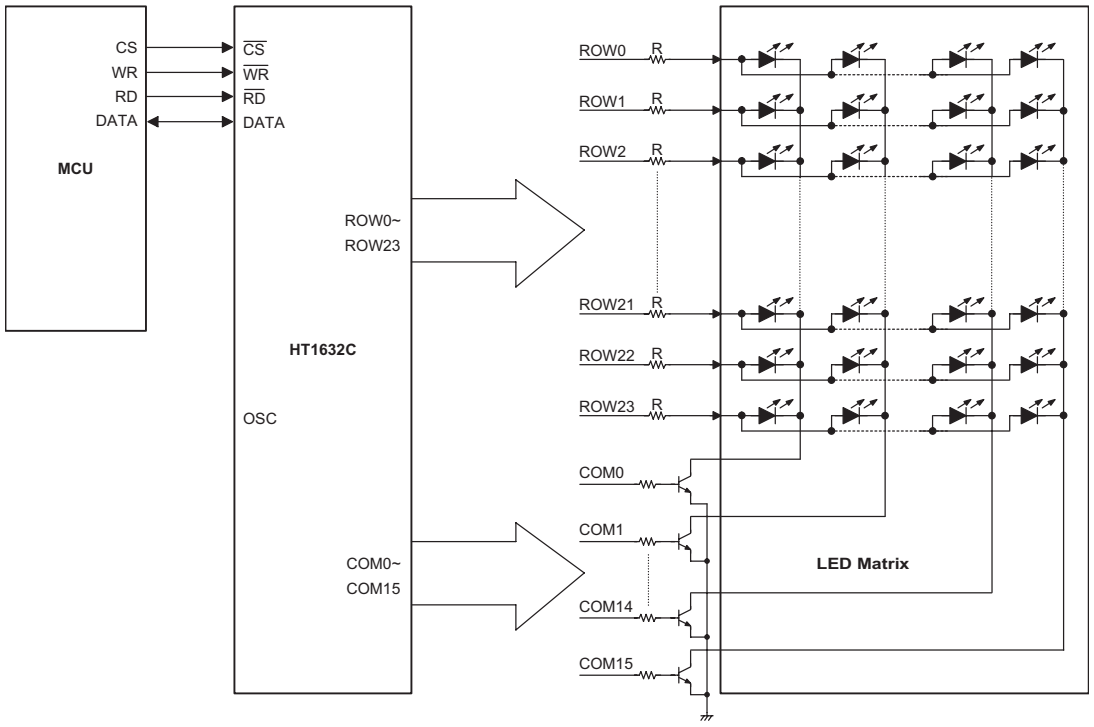


Note: 1.Values of the "R" resistors are selected depending on the power consumption of the LEDs.

2. In the PCB layout all VDD pins should be connected to the power plane.

3. In the PCB layout all VSS pins should be connected to the GND plane.

24 ROW × 16 COM Example: P-MOS open drain output and 16 COM option



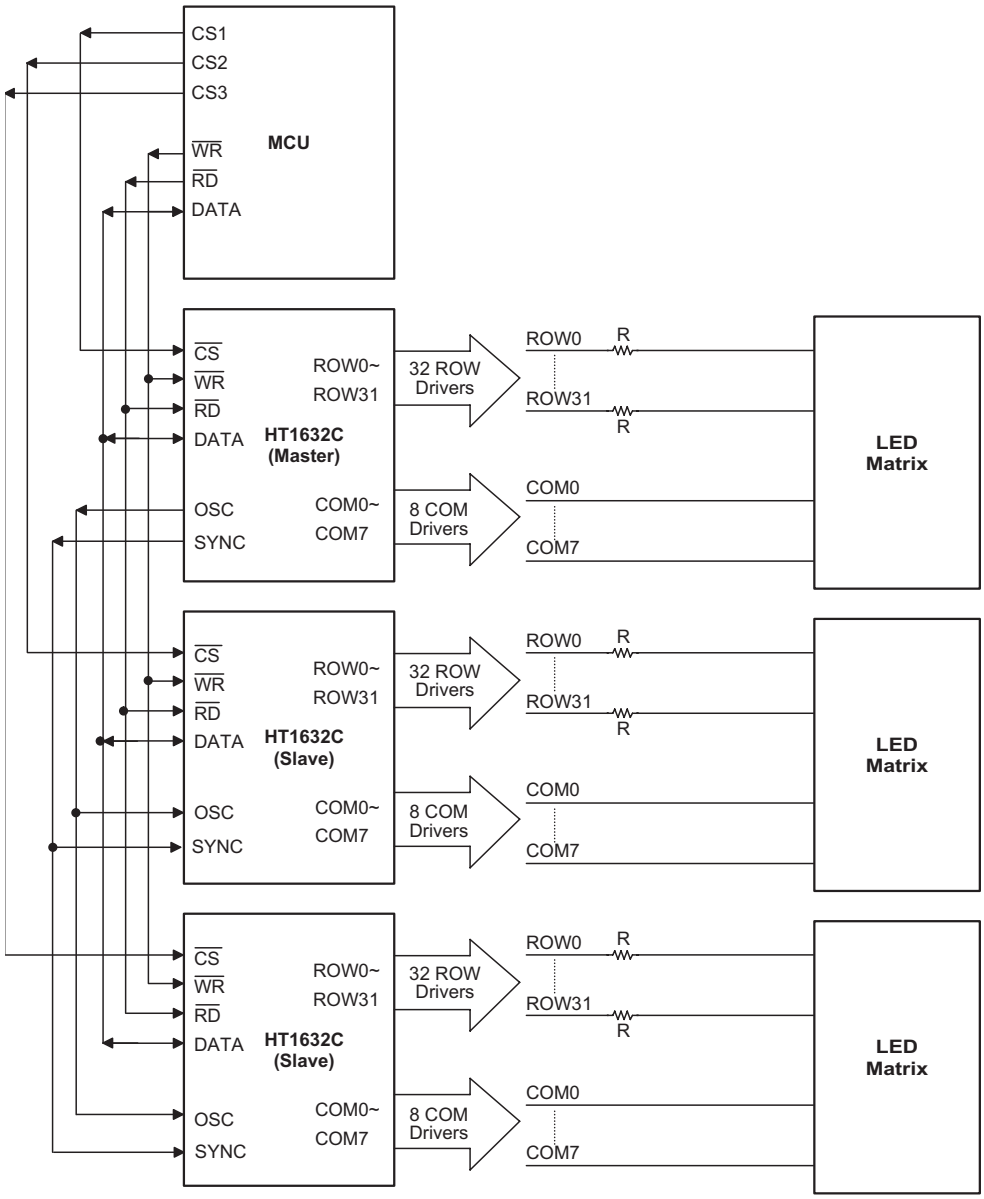
Note: 1. Values of the ″R″ resistors are selected depending on the power consumption of the LEDs.

2. In the PCB layout all VDD pins should be connected to the power plane.

3. In the PCB layout all VSS pins should be connected to the GND plane.

Cascade Function

32 ROW × 8 COM Example (Direct Drive): N-MOS open drain output and 8 COM option



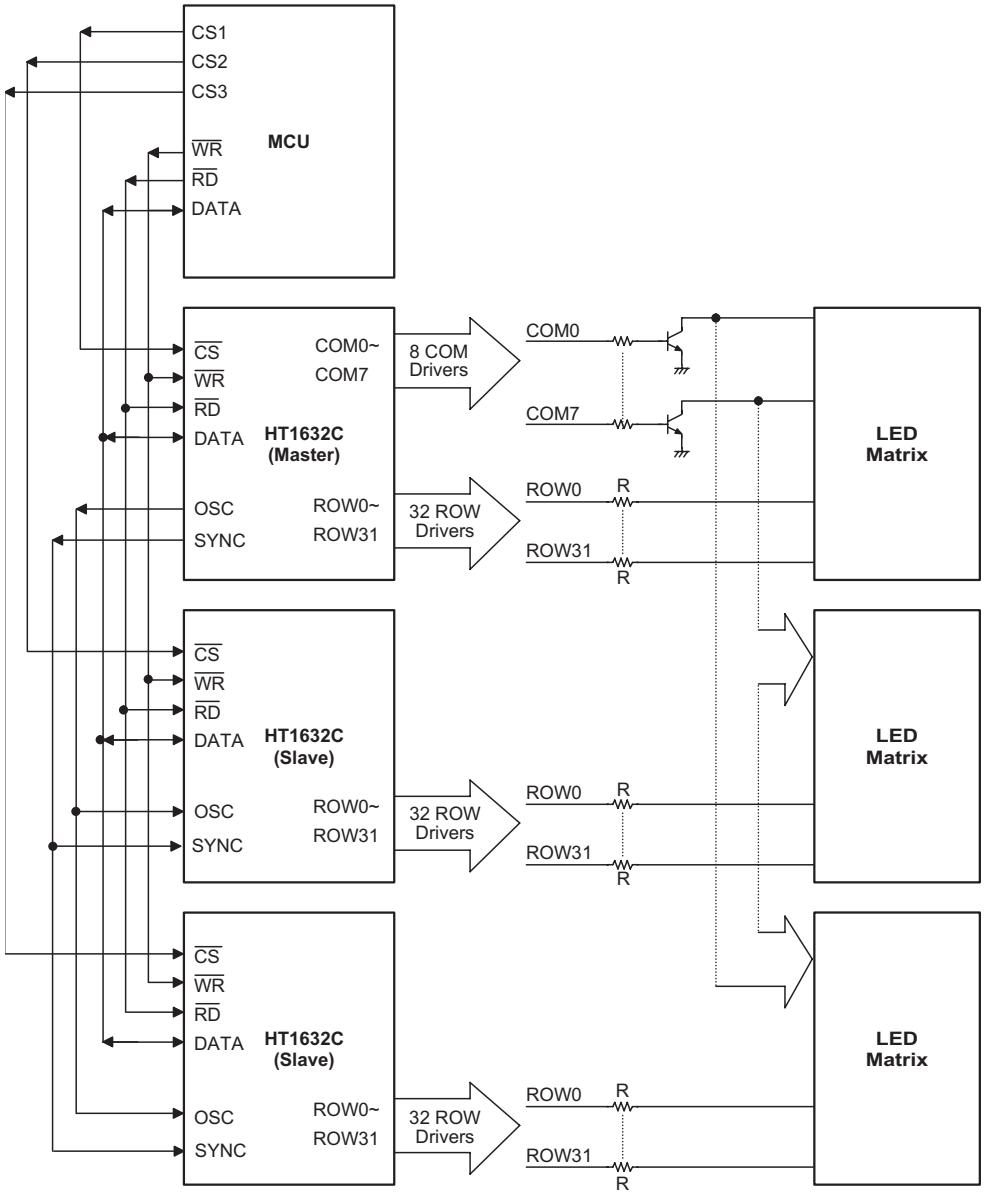
Note: 1. It also can set cascade mode by software. User must set the Master in master mode and Slaves in slave mode with command. The $\overline{CS}$ pin must be connected to MCU individually for independent read and write.

2. Values of the "R" resistors are selected depending on the power consumption of the LEDs.

3. In the PCB layout all VDD pins should be connected to the power plane.

4. In the PCB layout all VSS pins should be connected to the GND plane.

32 ROW × 8 COM Example (COM with Transistor Buffer):P-MOS open drain output and 8 COM option



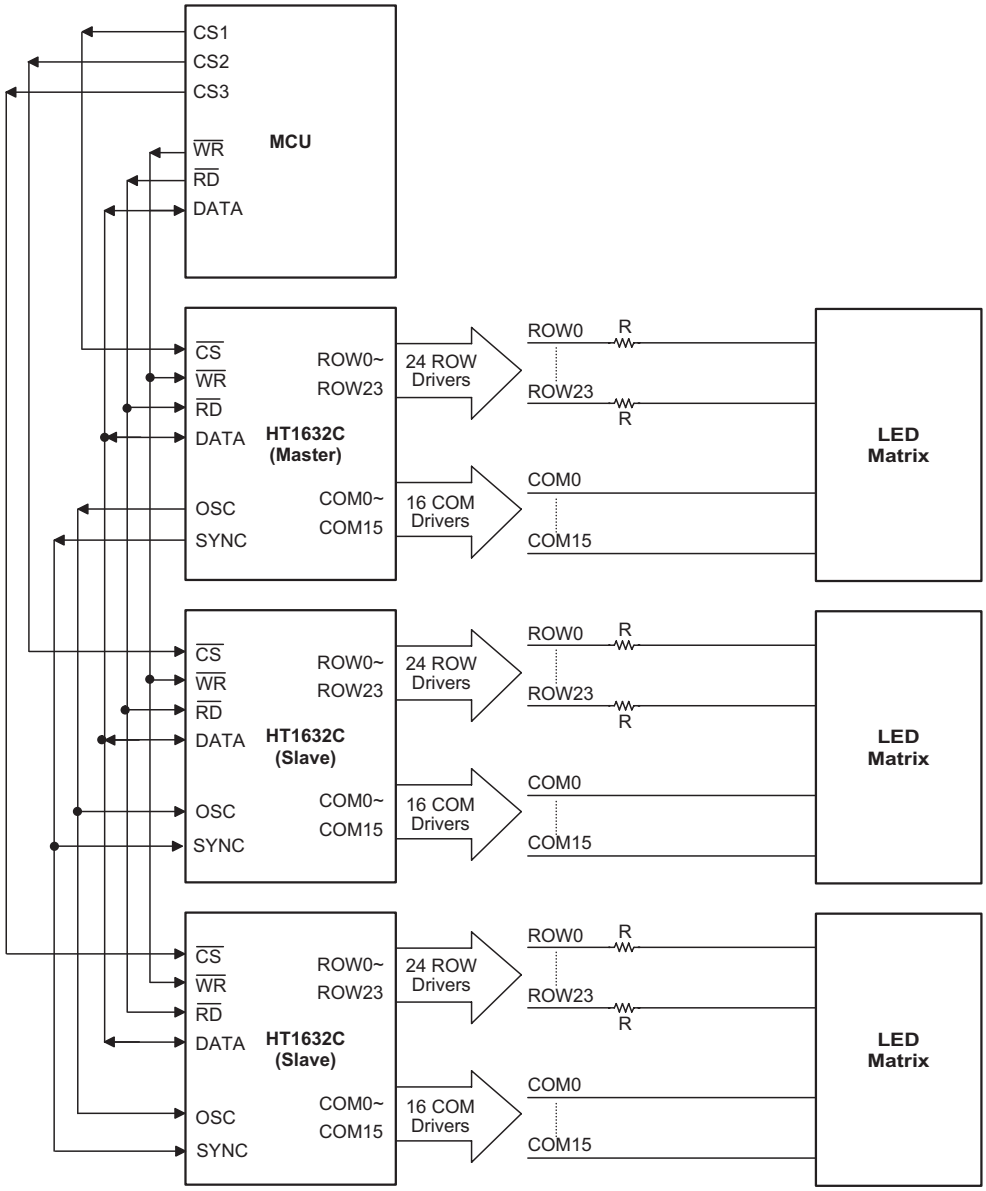
Note: 1. It also can set cascade mode by software. User must set the Master in master mode and Slaves in slave mode with command. The $\overline{CS}$ pin must be connected to MCU individually for independent read and write.

2. Values of the "R" resistors are selected depending on the power consumption of the LEDs.

3. In the PCB layout all VDD pins should be connected to the power plane.

4. In the PCB layout all VSS pins should be connected to the GND plane.

24 ROW × 16 COM Example (Direct Drive): N-MOS open drain output and 16 COM option



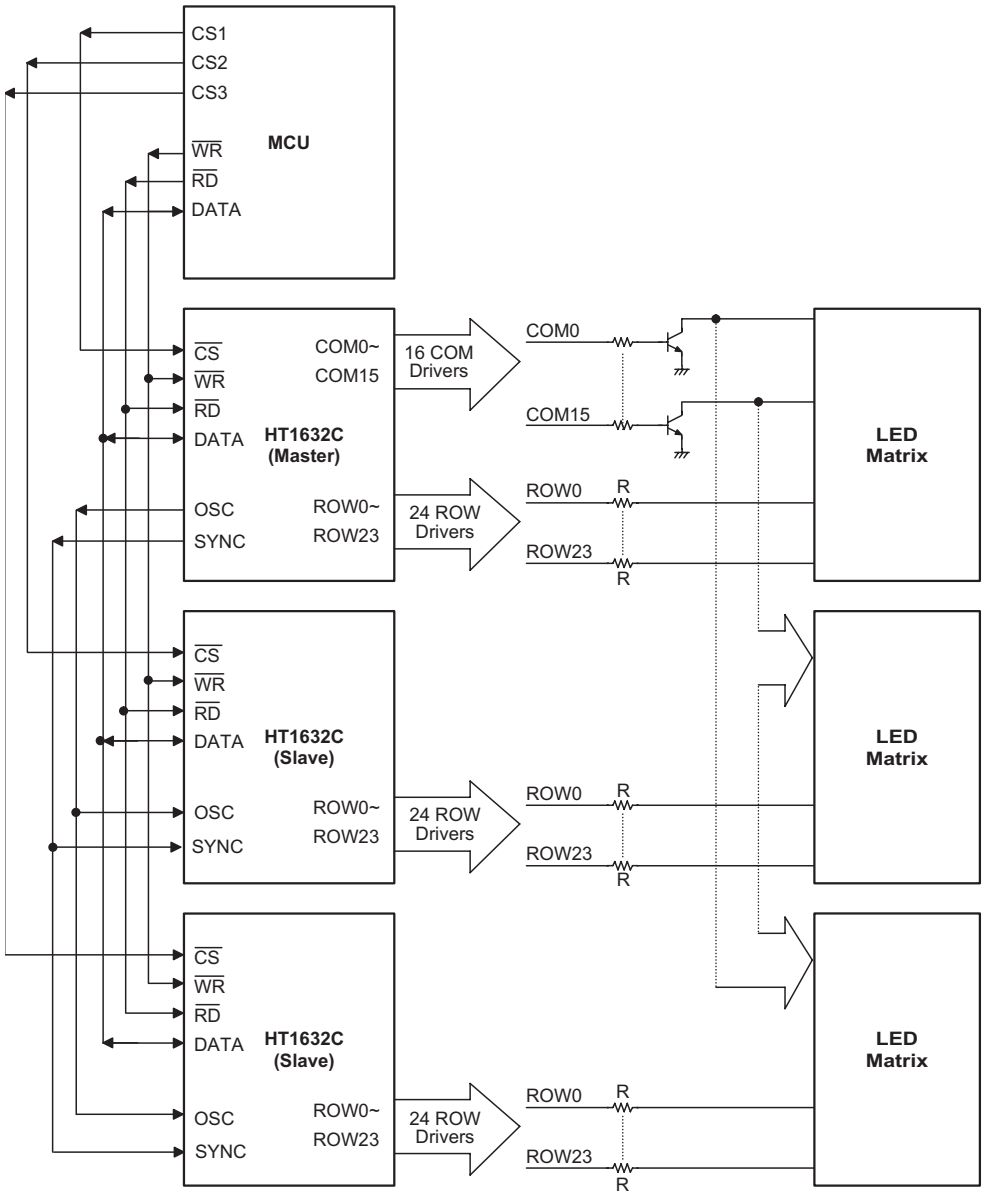
Note: 1. It also can set cascade mode by software. User must set the Master in master mode and Slaves in slave mode with command. The $\overline{CS}$ pin must be connected to MCU individually for independent read and write.

2. Values of the "R" resistors are selected depending on the power consumption of the LEDs.

3. In the PCB layout all VDD pins should be connected to the power plane.

4. In the PCB layout all VSS pins should be connected to the GND plane.

24 ROW × 16 COM Example (COM with Transistor Buffer):P-MOS open drain output and 16 COM option



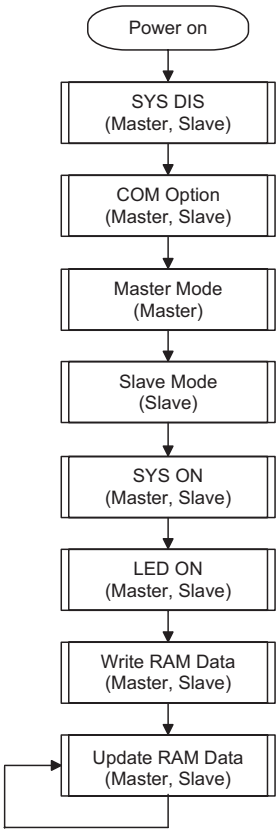
Note: 1. It also can set cascade mode by software. User must set the Master in master mode and Slaves in slave mode with command. The $\overline{CS}$ pin must be connected to MCU individually for independent read and write.

2. Values of the "R" resistors are selected depending on the power consumption of the LEDs.

3. In the PCB layout all VDD pins should be connected to the power plane.

4. In the PCB layout all VSS pins should be connected to the GND plane.

Cascade Control Flow



Command Summary

Name	ID	Command Code	D/C	Function	Default
READ	1 1 0	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A6A5A4A3A2A1A0D0D1D2D3	D	Read and Write data to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LED duty cycle generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LED Off	1 0 0	0000-0010-X	C	Turn off LED duty cycle generator	Yes
LED On	1 0 0	0000-0011-X	C	Turn on LED duty cycle generator	
BLINK Off	1 0 0	0000-1000-X	C	Turn off blinking function	Yes
BLINK On	1 0 0	0000-1001-X	C	Turn on blinking function	
SLAVE Mode	1 0 0	0001-0XXX-X	C	Set slave mode and clock source from external clock, the system clock input from OSC pin and synchronous signal input from SYN pin	
RC Master Mode	1 0 0	0001-10XX-X	C	Set master mode and clock source from on-chip RC oscillator, the system clock output to OSC pin and synchronous signal output to SYN pin	Yes

Name	ID	Command Code	D/C	Function	Default
EXT CLK Master Mode	1 0 0	0001-11XX-X	C	Set master mode and clock source from external clock, the system clock input from OSC pin and synchronous signal output to SYN pin	
COM Option	1 0 0	0010-abXX-X	C	ab=00: N-MOS open drain output and 8 COM option ab=01: N-MOS open drain output and 16 COM option ab=10: P-MOS open drain output and 8 COM option ab=11: P-MOS open drain output and 16 COM option	ab =00
PWM Duty	1 0 0	101X-0000-X	C	PWM 1/16 duty	
	1 0 0	101X-0001-X	C	PWM 2/16 duty	
	1 0 0	101X-0010-X	C	PWM 3/16 duty	
	1 0 0	101X-0011-X	C	PWM 4/16 duty	
	1 0 0	101X-0100-X	C	PWM 5/16 duty	
	1 0 0	101X-0101-X	C	PWM 6/16 duty	
	1 0 0	101X-0110-X	C	PWM 7/16 duty	
	1 0 0	101X-0111-X	C	PWM 8/16 duty	
	1 0 0	101X-1000-X	C	PWM 9/16 duty	
	1 0 0	101X-1001-X	C	PWM 10/16 duty	
	1 0 0	101X-1010-X	C	PWM 11/16 duty	
	1 0 0	101X-1011-X	C	PWM 12/16 duty	
	1 0 0	101X-1100-X	C	PWM 13/16 duty	
	1 0 0	101X-1101-X	C	PWM 14/16 duty	
	1 0 0	101X-1110-X	C	PWM 15/16 duty	
	1 0 0	101X-1111-X	C	PWM 16/16 duty	Yes

Note: X: Don't care

A6~A0: RAM addresses

D3~D0: RAM data

D/C: Data/command mode

Default: Power on reset default

All the bold forms, namely 1 1 0, 1 0 1, and 1 0 0, are mode commands. Among these, 1 0 0 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base clock frequency can be derived from an on-chip RC oscillator or an external clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1632C after power on reset, for power on reset may fail, which in turn leads to the malfunction of the HT1632C

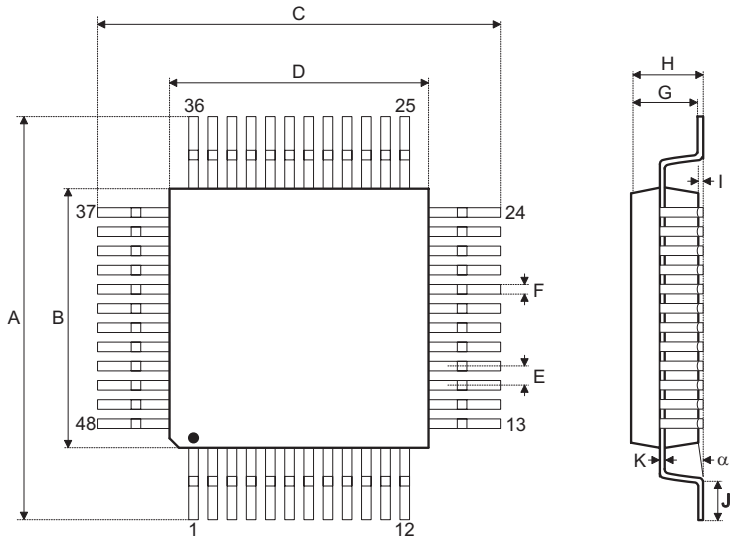
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

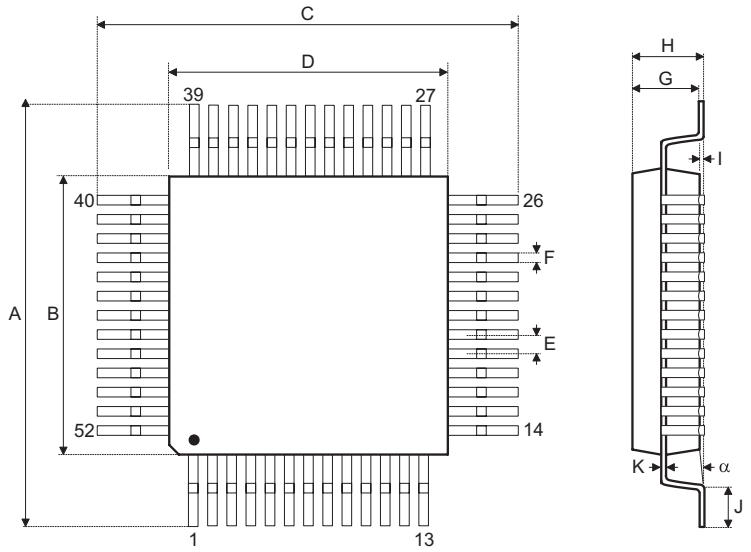
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

52-pin LQFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.622	0.630	0.638
B	0.547	0.551	0.555
C	0.622	0.630	0.638
D	0.547	0.551	0.555
E	—	0.039 BSC	—
F	0.015	—	0.019
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.008
J	0.018	—	0.030
K	0.005	—	0.007
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	15.80	16.00	16.20
B	13.90	14.00	14.10
C	15.80	16.00	16.20
D	13.90	14.00	14.10
E	—	1.00 BSC	—
F	0.39	—	0.48
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.20
J	0.45	—	0.75
K	0.13	—	0.18
α	0°	—	7°

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