SC4215H

Very Low Input /Very Low Dropout 2 Amp Regulator With Enable

Features

- Input Voltage as low as 1.4V
- 400mV dropout @ 2A
- Adjustable output from 0.5V
- Over current and over temperature protection
- Enable pin
- 10µA quiescent current in shutdown
- Full industrial temperature range
- Available in SOIC-8-EDP Lead-free package, fully WEEE and RoHS compliant and halogen free

Applications

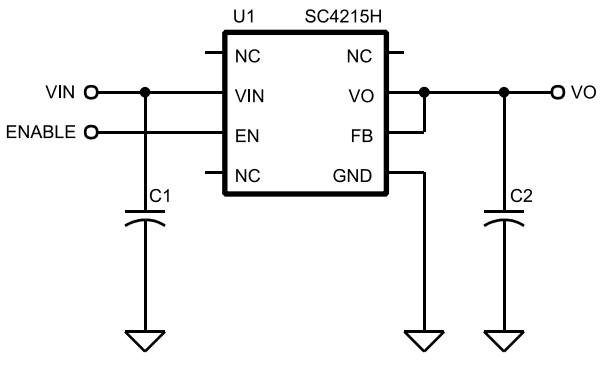
- Telecom/Networking cards
- Motherboards/Peripheral cards
- Industrial applications
- Wireless infrastructure
- Set top boxes
- Medical equipment
- Notebook computers
- Battery powered systems

Description

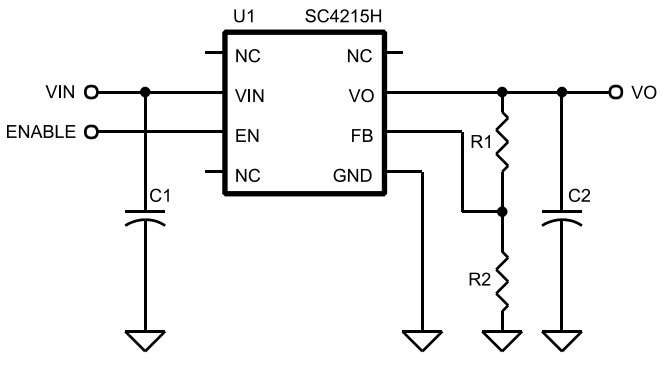
The SC4215H is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 2 amperes. It operates with a Vin as low as 1.4V, with output voltage programmable as low as 0.5V. The SC4215H features ultra low dropout, ideal for applications where Vout is very close to Vin. Additionally, the SC4215H has an enable pin to further reduce power dissipation while shutdown. The SC4215H provides excellent regulation over variations in line, load and temperature.

The SC4215H is available in the SOIC-8-EDP (Exposed Die Pad) package. The output voltage can be set via an external divider or to a fixed setting of 0.5V depending on how the FB pin is configured.

Typical Application Circuit

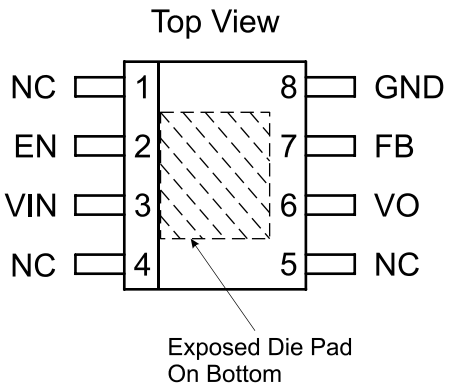


VO=0.5V



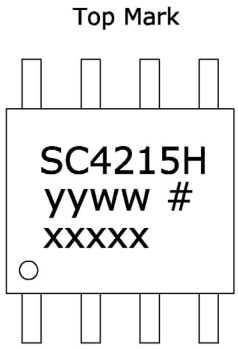
$$VO = \frac{0.5(R1+R2)}{R2} \text{ (Volts)}$$

Pin Configuration



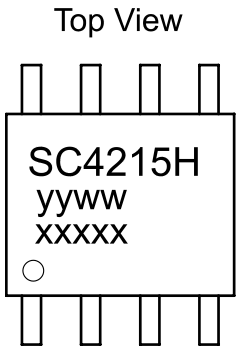
SOIC-8-EDP

Marking Information SC4215HSETRC



YYWW=Datecode (Example: 1601) #: Cu Wire Material
XXXXX=Semtech Lot No. (Example 00101)

Marking Information SC4215HSETRT



yyww = Datecode (Example: 0752)
xxxxx = Semtech Lot No. (Example: 00101)

Ordering Information

Device	Package
SC4215HSETRT(1)(2)	SOIC-8-EDP
SC4215HSETRC(1)(2)	SOIC-8-EDP
SC4215HEVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 2,500 devices.
(2) Available in lead-free package only. Device is WEEE and RoHS compliant and halogen free.

Absolute Maximum Ratings

VIN, EN, VO, FB to GND (V) ..... -0.3 to +7.0
Power Dissipation..... Internally Limited
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

VIN (V) ..... $1.4 \leq V_{IN} \leq 6.0$
Ambient Temperature Range (°C)..... $-40 \leq T_A \leq +105$
Junction Temperature Range (°C)..... $-40 \leq T_J \leq +125$
Maximum Output Current (A) 2

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) 36
Thermal Resistance, Junc to Case[2] (°C/W)..... 5.5
Maximum Junction Temperature (°C).....+150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: $V_{EN} = V_{IN}$, $V_{FB} = V_O$, V_{IN} = 1.40V to 6.0V, I_O = 10µA to 2A, T_A = 25° C.
Values in bold apply over the full operating temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VIN						
Quiescent Current	I_Q	V_{IN} = 3.3V, I_O = 0A			**3**	mA
		V_{IN} = 6.0V, V_{EN} =0V		10	**50**	µA
VO						
Output Voltage[1] (Fixed Voltage, $V_{FB} = V_O$)	V_O	$V_{IN} = V_O$ + 0.5V, I_O = 10mA	-2%	V_O	+2%	V
		V_{IN} = 1.8V, I_O = 0.8A, 0°C ≤ $T_J = T_A$ ≤85°C				
		1.40V ≤ V_{IN} ≤ 6.0V, I_O = 10mA	**-3%**		**+3%**	
Line Regulation[1]	$REG_{(LINE)}$	I_O =10mA		0.2	**0.4**	%/V
Load Regulation[1]	$REG_{(LOAD)}$	I_O =10mA to 2A		0.5	**1.5**	%

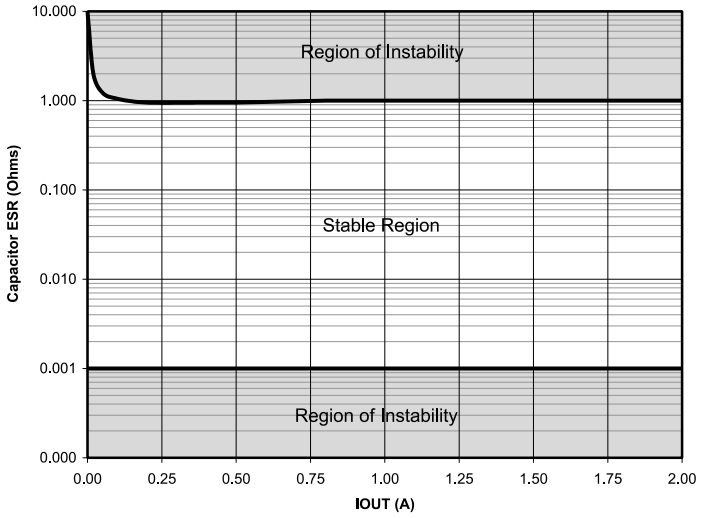
Electrical Characteristics (continued)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Dropout Voltage[1][2]	V_{DO}	I_O =1A	1.4V ≤ V_{IN} < 1.6V		90	**400**	mV
			1.6V ≤ V_{IN} ≤ 6.0V			**200**	
		I_O =1.5A	1.4V ≤ V_{IN} < 1.6V		200	**500**	
			1.6V ≤ V_{IN} ≤ 6.0V			**300**	
		I_O = 2A	1.4V ≤ V_{IN} < 1.6V		300	**600**	
			1.6V ≤ V_{IN} ≤ 6.0V			**400**	
Minimum Load Current[3][4]	I_O					**10**	µA
Current Limit[4]	I_{CL}			**2.1**	3	**4.4**	A
Feedback							
Reference Voltage[1]	V_{REF}	V_{IN} = 3.3V, V_{FB} = V_{OUT} , I_O =10mA		0.495	0.5	0.505	V
				0.490		**0.510**	
Feedback Pin Current[4]	I_{ADJ}	V_{FB} = V_{REF}			80	**200**	nA
EN							
Enable Pin Current	I_{EN}	V_{EN} = 0V, V_{IN} =3.3V			1.5	**10**	µA
Enable Pin Threshold	V_{IH}	V_{IN}=3.3V		**1.6**			V
	V_{IL}					**0.4**	
Over Temperature Protection							
High Trip Level	T_{HI}				160		°C
Hysteresis	T_{HYST}				10		°C

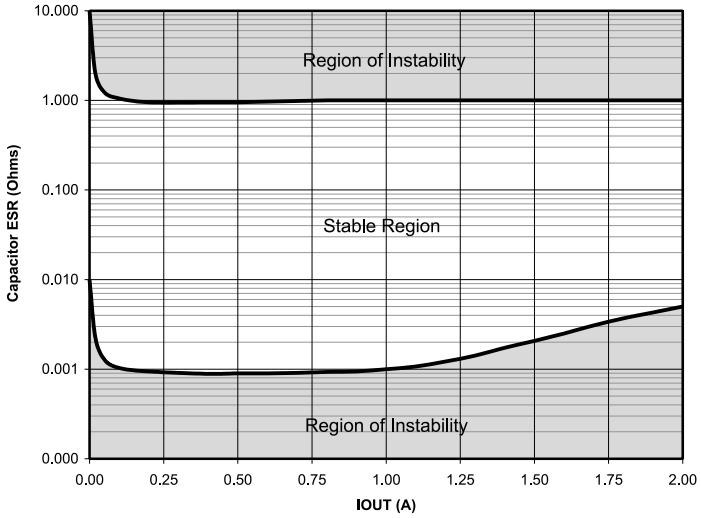
Notes:
(1) Low duty cycle pulse testing with Kelvin connections required.
(2) V_{DO} = V_{IN} -V_O when V_O decreases by 1.5% of its nominal output voltage with V_{IN} = V_O +0.8V.
(3) Required to maintain regulation. Voltage set resistors R1 and R2 are usually utilized to meet this requirement.
(4) Guaranteed by design.

Typical Characteristics

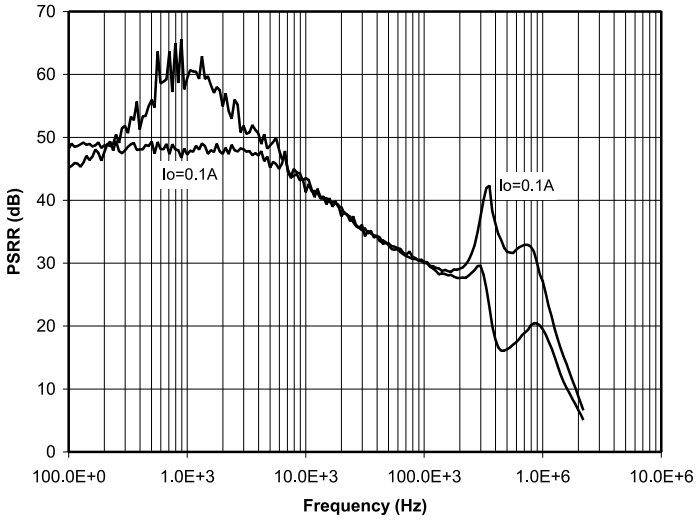
Stability Curve, Cout=10uF



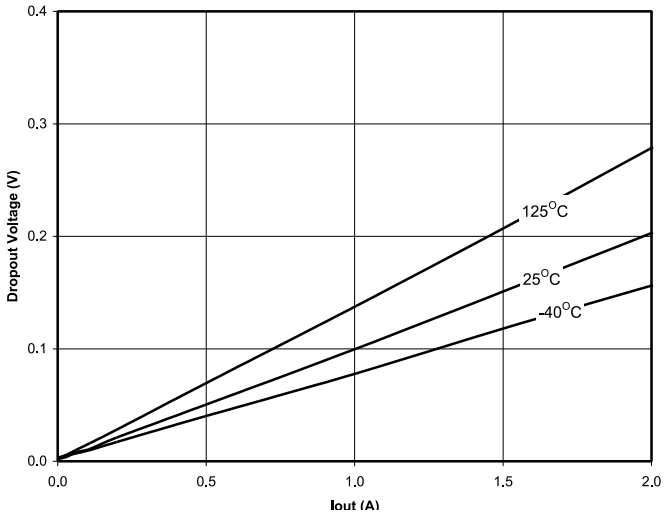
Stability Curve, Cout=100uF



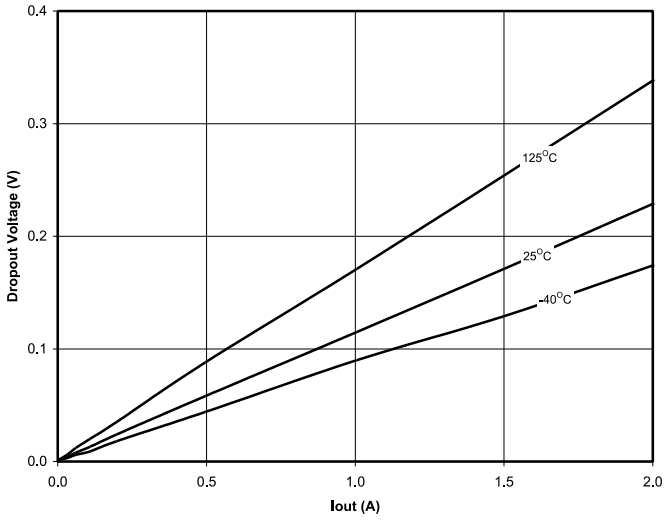
Typical PSSR Vin=5.0V; Vo=3.3V



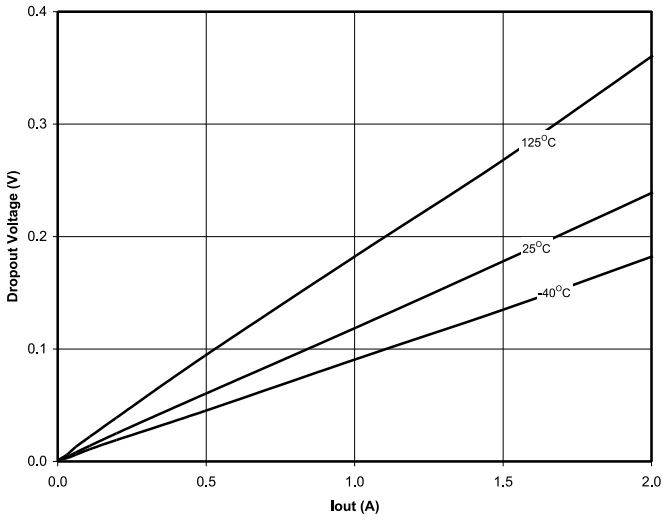
Typical Dropout Voltage at Vout = 3.3V



Typical Dropout Voltage at Vout = 1.6V



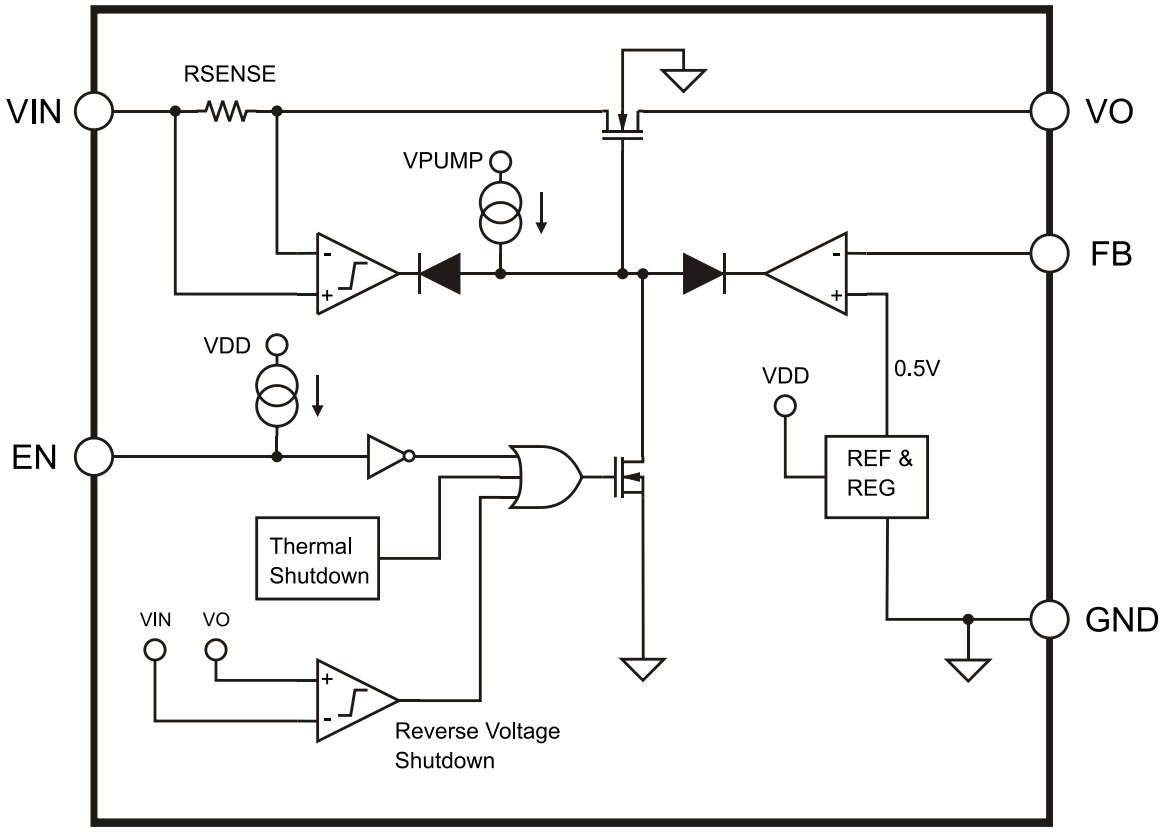
Typical Dropout Voltage at Vout = 1.4V



Pin Descriptions

Pin #	Pin Name	Pin Function
2	EN	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open. Connect to VIN if not being used.
3	VIN	Input voltage. For regulation at full load, the input to this pin must be between (VO+ 0.5V) and 6.0V. Minimum VIN = 1.4V. A large bulk capacitance should be placed closely to this pin to ensure that the input supply does not sag below 1.4V. Also a minimum of 4.7uF ceramic capacitor should be placed directly at this pin.
6	VO	The pin is the power output of the device. A minimum of 10uF capacitor should be placed directly at this pin.
7	FB	When this pin connected to the Vo pin, the output voltage will be set at 0.5V. If external feedback resistors are used, the output voltage will be determined by the resistor ratio (See Application Circuits on page 1):
8	GND	Reference ground. The GND pin and the exposed die pad must be connected together at the IC pin.
1, 4, 5	NC	No Connection.
	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias.

Block Diagram



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Applications Information (continued)

Introduction

The SC4215H is intended for applications where high current capability and very low dropout voltage are required. It provides a very simple, low cost solution that uses very little PCB real estate. Additional features include an enable pin to allow for a very low power consumption standby mode, and a fully adjustable output.

The SC4215H is especially recommended for applications where VO>3.8V, for lower output voltage requirements the SC4215A can be considered.

Component Selection

Input capacitor: A large bulk capacitance ≥ 10µF/A (output load) should be closely placed to the input supply pin of the SC4215H to ensure that Vin does not sag below 1.4V. Also a minimum of 4.7µF ceramic capacitor is recommended to be placed directly next to the Vin pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, input droop due to load transients is reduced, improving load transient response. Additional capacitance may be added if required by the application.

Output capacitor: A minimum bulk capacitance of ≥ 10µF/A (output load), along with a 0.1µF ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the SC4215H is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

Noise immunity: In very electrically noisy environments, it is recommended that 0.1µF ceramic capacitors be placed from IN to GND and OUT to GND as close to the device pins as possible.

Internal voltage selection: By connecting the FB pin directly to the VO pin, the output voltage will be regulated to the 0.5V internal reference.

External voltage selection resistors: The use of 1% resistors, and designing for a current flow ≥ 10µA is recommended to ensure a well regulated output (thus R2 ≤50kΩ). A suitable value for R2 can be chosen in the range of 1kΩ to 50kΩ. R1 can then be calculated from.

$$R_1 = R_2 \cdot \frac{(V_O - V_{REF})}{V_{REF}}$$

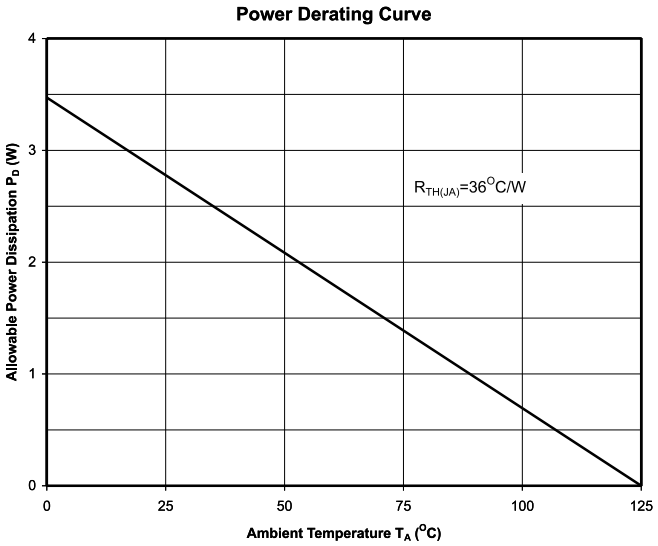
Enable: Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. A pull up resistor up to 400kOhms should be connected from this pin to the VIN pin in applications where supply voltages of Vin < 1.9V are required. For applications with higher voltages than 1.9V, EN pin could be left open or connected to VIN.

Thermal Considerations

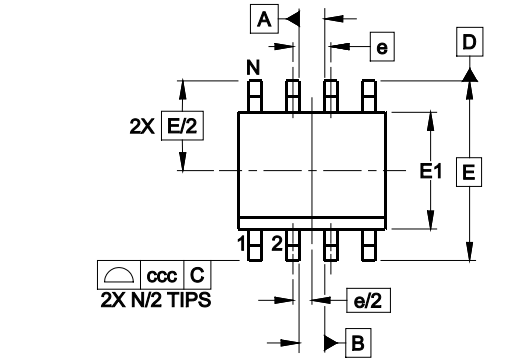
The power dissipation in the SC4215H is given by:

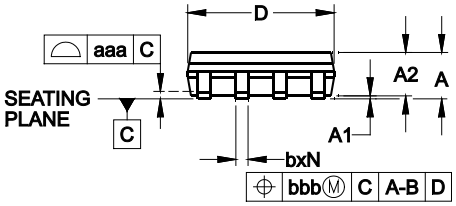
$$P_D \approx I_O \times (V_{IN} - V_O)$$

The allowable power dissipation will be dependant on the thermal impedance achieved in the application. The derating curve below is valid for the thermal impedance specified in the Thermal Information section on page 3.

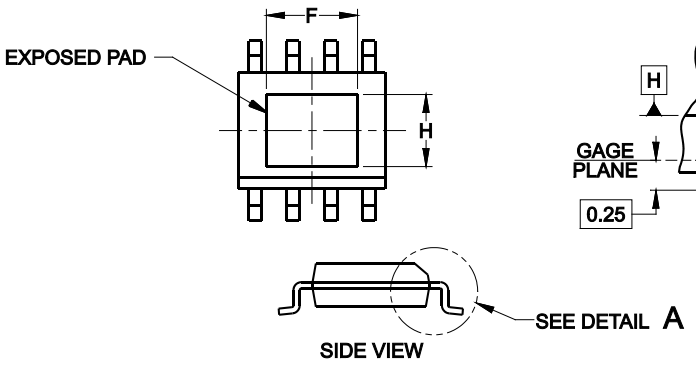


Outline Drawing — SOIC-8-EDP-2





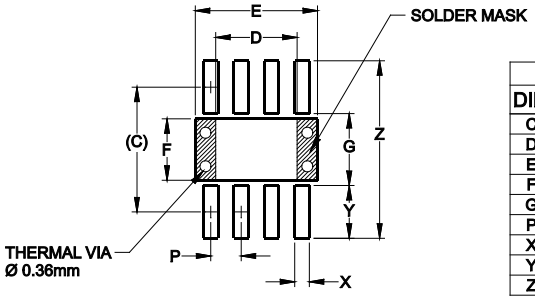
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.000	-	.005	0.00	-	0.13
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
F	.116	.120	.130	2.95	3.05	3.30
H	.085	.095	.099	2.15	2.41	2.51
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.05)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION BA.

Land Pattern — SOIC-8-EDP-2



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
D	.134	3.40
E	.201	5.10
F	.101	2.56
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

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