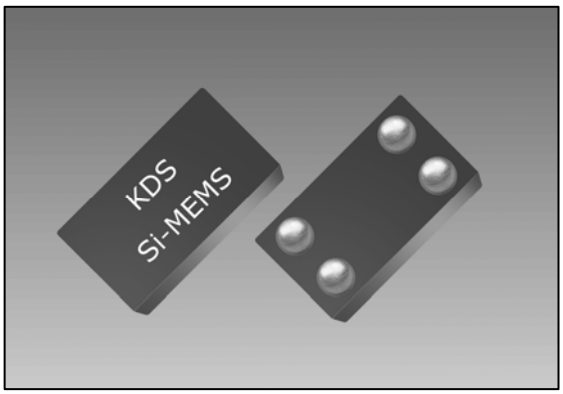
kHz Band Temperature Compensated MEMS Oscillator

MO1552



■Features

- ●Fixed 32.768 kHz
- ●Smallest footprint in chip-scale (CSP): 1.5 x 0.8 mm
- ●±5, ±10, ±20 x 10^{-6} frequency stability options over temp
- ●Ultra-low power: +990 nA (typ.)
- ●Internal filtering eliminates external Vdd bypass cap
- ●NanoDrive™ programmable output swing for lowest power

■Applications

- ●Smart meters
- ●Health and wellness monitors
- ●Pulse-per- second timekeeping
- ●RTC reference clock

■Standard Specification

Item	symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency	Fout		32.768		kHz	
Supply Voltage	Vdd	+1.5	-	+3.63	V	T_A = -40°C to +85°C
Operating Temperature Range	Op_Temp		0~+70 / -40~+85		°C	
Frequency Stability Over Temperature [1] (without Initial Offset [2])	F_stab	-5	-	+5	x 10^{-6}	Stability part number code = E
		-10	-	+10		Stability part number code = F
		-20	-	+20		Stability part number code = G
Frequency Stability Over Temperature (with Initial Offset [2])	F_stab	-10	-	+10		Stability part number code = E
		-13	-	+13		Stability part number code = F
		-22	-	+22		Stability part number code = G
First Year Frequency Aging	F_aging	-1.0	-	+1.0	x 10^{-6}	T_A = +25°C, Vdd = +3.3V
Core Supply Current [3]	Idd	-	+0.99	-	µA	T_A = +25°C, Vdd= +1.8V, LVCMOS Output configuration, No Load
		-	-	+1.52		T_A = -40°C to +85°C, Vdd= +1.5V – +3.63V, No Load
Start-up Time at Power-up	t_start	-	180	300	ms	T_A = -40°C to +60°C, valid output
		-	-	350		T_A = +60°C to +70°C, valid output
		-	-	380		T_A = +70°C to +85°C, valid output
LVCMOS Output						
Output Clock Duty Cycle	DC	48	-	52	%	
Output Voltage Low	V_{OL}	-	-	Vdd x 0.1	V	Vdd: +1.5V – +3.63V. I_{OL} = +1.0 µA, 15 pF Load
Output Voltage High	V_{OH}	Vdd x 0.9	-	-		Vdd: +1.5V – +3.63V. I_{OH} = -1.0 µA, 15 pF Load
Output Rise/Fall Time	tr,tf	-	100	200	ns	10-90% (Vdd), 15 pF Load
		-	-	50		10-90% (Vdd), 5 pF Load, Vdd ≥ +1.62V
NanoDrive™ Programmable, Reduced Swing Output						
Output Clock Duty Cycle	DC	48	-	52	%	
AC-coupled Programmable Output Swing	V_sw	-	+0.20 to +0.80	-	V	MO1552 does not internally AC-couple. This output description is intended for a receiver that is AC-coupled. Vdd: +1.5V – +3.63V, 10 pF Load, I_{OH} / I_{OL} = ±0.2 µA
DC-Biased Programmable Output Voltage Low Range	V_{OL}	-	+0.35 to +0.80	-	V	Vdd +1.5V – +3.63V. I_{OL} = +0.2 µA, 10 pF Load
DC-Biased Programmable Output Voltage High Range	V_{OH}	-	+0.60 to +1.225	-	V	Vdd: +1.5V – +3.63V. I_{OH} = -0.2 µA, 10 pF Load
Output Rise/Fall Time	tr,tf	-	-	200	ns	30-70% (V_{OL}/V_{OH}), 10 pF Load

[1]. No board level underfill. Measured as peak-to-peak/2. Inclusive of 3x-reflow and ±20% load variation. Tested with Keysight 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.

[2]. Initial offset is defined as the frequency deviation from the ideal 32.768 kHz at room temperature, post reflow.

[3]. Core operating current does not include output driver operating current or load current.To derive total operating current (no load), add core operating current +output driver operating current, which is a function of the output voltage swing. See the description titled, Calculating Load Current.

Consult our sales representative for other specifications.

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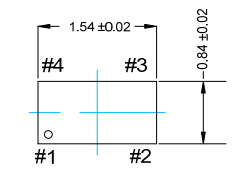
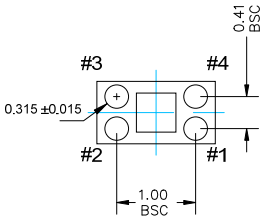
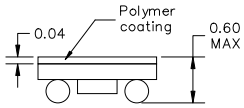
■Dimensions and Patterns

Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)

1.55 x 0.85 mm CSP

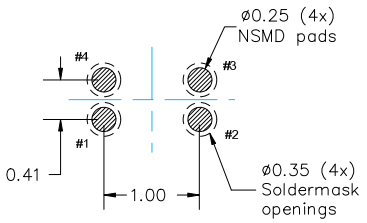






Pin Connections

Pin No.	Connection
#1	GND
#2	CLK Output
#3	Vdd
#4	GND



(soldermask openings shown with heavy dashed line)

Recommend 4-mil (0.1mm) stencil thickness