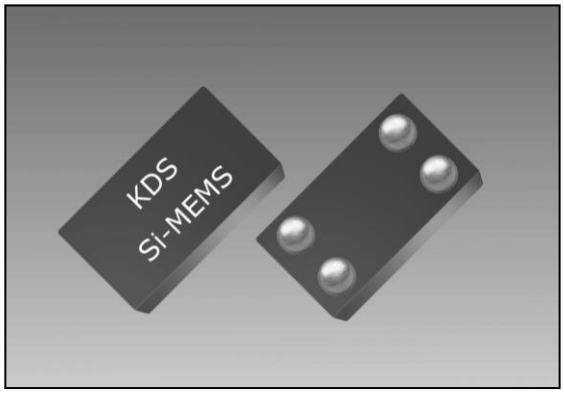
kHz Band Temperature Compensated MEMS Oscillator

KDS DAISHINKU CORP.

MO1568

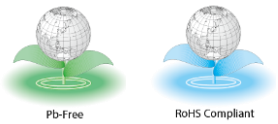


■Features

- ●32.768 kHz ±5 x 10^{-6} all-inclusive frequency stability
- ●Smallest TCXO Footprint: 1.2mm^2
  - ・1.5 x 0.8 mm CSP / ・No external bypass cap required
- ●Ultra-low power: +4.5 µA
- ●In-system auto-calibration enables overmold
- ●In-system auto-calibration:
  - ・Compensates for board-level stress-induced frequency errors
  - ・Improves all-inclusive frequency stability

■Applications

- ●Smart Watches, Health and wellness monitors
- ●Smart utility meters
- ●Internet of Things (IoT)



■Standard Specification

Conditions: Min/Max limits are over temperature, Vdd = +1.8V±10%, unless otherwise stated. Typicals are at +25°C and Vdd = +1.8V.

Item	symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency	Fout		32.768		kHz	
Operating Supply Voltage	Vdd	+1.62	+1.8	+1.98	V	
Operating Temperature Range	Op_Temp		-20~+70 / -40~+85		°C	
Total Frequency Stability after Overmold[1]	F_stab	-5.0	-	+5.0	x 10^{-6}	All inclusive, after overmold, post in-system calibration.
		-25	-	+25		All inclusive, after overmold, before in-system calibration.
Total Frequency Stability without Overmold or Calibration[1]		-5.0	-	+5.0		All inclusive, under influence of up to 5°C/sec temp gradient and board-level underfill.
Allan Dviation	AD	-	1e-8	4e-8	-	1 second averaging time
First Year Frequency Aging	F_aging	-	±1.0	-	x 10^{-6}	T_A = +25°C, Vdd = +1.8V, with overmold.
Supply Current	Idd	-	+4.5	+5.3	µA	No load
Start-up Time at Power-up	t_start	-	-	300	ms	Measured when supply reaches 90% of final Vdd to the first output pulse.
Output Clock Duty Cycle	DC	45	-	55	%	
Output Voltage Low	V_{OL}	-	-	Vdd x 0.1	V	I_{OL} = +1.0 µA
Output Voltage High	V_{OH}	Vdd x 0.9	-	-		I_{OH} = -1.0 µA
Output Rise/Fall Time	tr,tf	-	9.0	20	ns	10-90% (Vdd), 15 pF Load
Integrated Phase Jitter	IPJ	-	1.8	2.5	ns_{RMS}	Integration bandwidth = 100 Hz to 16.384 kHz. Inclusive of +50mV peak-to-peaks inusoidal noise on Vdd. Noise frequency 100 Hz to 20 MHz.
RMS Period Jitter	PJ_{RMS}	-	2.5	4	ns_{RMS}	10,000 samples, per JEDEC standard 65B
Peak-to-Peak Period Jitter	PJ_{p-p}	-	20	35	ns_{p-p}	
Dynamic Temperature Frequency Response	-	-0.5	-	+0.5	10^{-6}/sec	Under temp ramp up to +1.5°C/sec

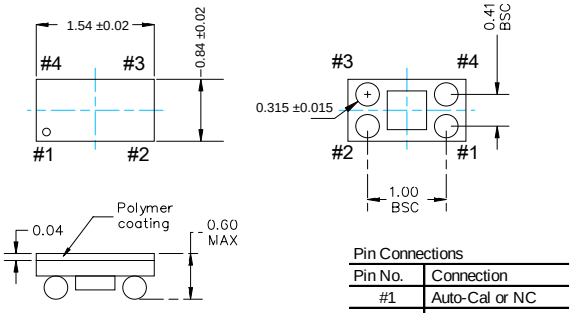
[1]. Contact Factory for specific overmold conditions. Relative to 32.768kHz, includes initial tolerance, over temp, Vdd, load, hysteresis, board-level underfill, and, 3x reflow. Tested with Keysight 53132A frequency counter. Measured with 100ms gate time for accurate frequency measurement.

Consult our sales representative for other specifications.

■Dimensions and Patterns

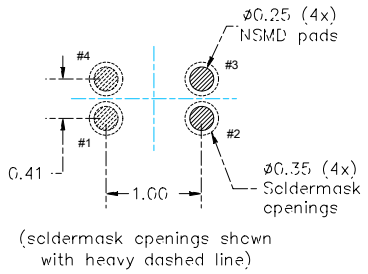
Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)

1.55 x 0.85 mm CSP



Pin Connections

Pin No.	Connection
#1	Auto-Cal or NC
#2	CLK Output
#3	Vdd
#4	GND



Recommend 4-mil (0.1mm) stencil thickness