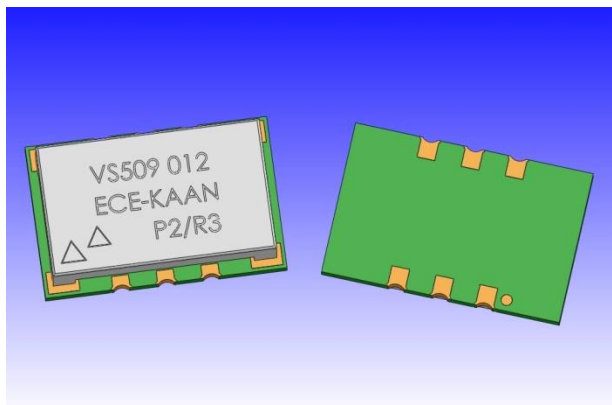




## VS-509 Dual Frequency VCSO



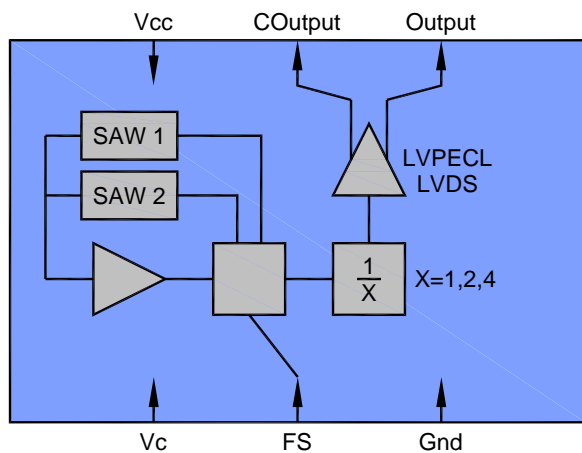
### Features

- Industry Standard Package, 9.1 x 13.8 x 3.1 mm
- 5<sup>th</sup> Generation ASIC Technology for Ultra Low Jitter  
125 fs-rms ( $f_N = 622.08$  MHz, 12 kHz to 20 MHz)  
120 fs-rms ( $f_N = 622.08$  MHz, 50 kHz to 80 MHz)
- Output Frequencies from 150 MHz to 1000 MHz
- Spurious Suppression, 90 dBc Typical
- 3.3V Supply Voltage
- LVPECL or LVDS Output Configurations
- Tri-State Frequency Select (F1, OD, F2)
- Compliant to EC RoHS6 Directive

### Applications

PLL circuits for Clock Smoothing and Frequency Translation

| Description                       | Standard           |
|-----------------------------------|--------------------|
| • SONET / SDH                     | GR-253-CORE        |
| • OTN (Optical Transport Network) | ITU-T G.709/Y.1331 |
| • 10 GbE (Gigabit Ethernet)       | IEEE 802.3ae       |
| • 10 GFC (Gigabit Fibre Channel)  | INCITS 364-2003    |
| • 40 GbE & 100 GbE                | IEEE 802.3ba       |
| • Synchronous Ethernet            | ITU-T G.8261       |
| • WiMax                           | IEEE 802.16        |



### Description

The VS-509 is a Voltage Controlled SAW Oscillator that operates at the fundamental frequency from one of the two internal SAW filters. The SAW filters are high-Q Quartz devices that enable the circuit to achieve low phase jitter performance over a wide operating temperature range. A divider circuit is deployed for output frequencies less than 600 MHz. The selectable dual oscillator is housed in a hermetically sealed leadless surface mount package and offered on tape and reel. It has a tri-state Frequency Select function that provides one of three conditions: Frequency 1, Output Disable, or Frequency 2.

## VS-509 Dual Frequency VCSO

| Electrical Performance: 3.3V LV-PECL |            |                  |              |              |             |         |
|--------------------------------------|------------|------------------|--------------|--------------|-------------|---------|
| Parameter                            | Symbol     | Minimum          | Typical      | Maximum      | Units       | Notes   |
| <b>Frequency</b>                     |            |                  |              |              |             |         |
| Nominal Frequency                    | $f_N$      | 150              |              | 1000         | MHz         | 1,2,3   |
| Absolute Pull Range                  | APR        | $\pm 50$         |              |              | ppm         | 1,2,3,9 |
| Linearity                            | Lin        |                  | $\pm 7$      |              | %           | 2,4,9   |
| Gain Transfer (Low / Standard)       | $K_V$      |                  | +300 / +365  |              | ppm/V       | 2,9     |
| Temperature Stability                | $f_{STAB}$ |                  | $\pm 100$    |              | ppm         | 1,7     |
| <b>Supply</b>                        |            |                  |              |              |             |         |
| Voltage ( $\pm 10\%$ )               | $V_{CC}$   | 2.97             | 3.3          | 3.63         | V           | 2,3     |
| Current (Typical 50 $\Omega$ Load)   | $I_{CC}$   |                  | 73           |              | mA          | 3       |
| Current (No Load)                    | $I_{CC}$   |                  | 60           | 75           | mA          | 3       |
| <b>Outputs</b>                       |            |                  |              |              |             |         |
| Mid Level                            |            | $V_{CC}-1.5$     | $V_{CC}-1.3$ | $V_{CC}-1.1$ | mV          | 2,3     |
| Single Ended Swing                   |            |                  | 750          |              | mV-pp       | 2,3     |
| Differential Swing                   |            |                  | 1.5          |              | V-pp        | 2,3     |
| Current                              | $I_{OUT}$  |                  |              | 20           | mA          | 7       |
| Rise Time                            | $t_R$      |                  | 180          | 250          | ps-pp       | 6,7     |
| Fall Time                            | $t_F$      |                  | 180          | 250          | ps-pp       | 6,7     |
| Symmetry                             | SYM        | 45               | 50           | 55           | %           | 2,3     |
| Spurious Suppression                 |            | 85               | 90           |              | dBc         | 7       |
| Jitter ( $600 \leq f_N \leq 1000$ )  | $\phi_J$   |                  | 150          |              | fs-rms      | 7,8     |
| Jitter ( $300 \leq f_N \leq 500$ )   | $\phi_J$   |                  | 190          |              | fs-rms      | 7,8     |
| Jitter ( $150 \leq f_N \leq 250$ )   | $\phi_J$   |                  | 280          |              | fs-rms      | 7,8     |
| <b>Control Voltage</b>               |            |                  |              |              |             |         |
| Input Impedance (F1 or F2 Enabled)   | $Z_C$      |                  | 167          |              | k $\Omega$  | 7       |
| Input Impedance (Output Disabled)    | $Z_C$      |                  | 472          |              | k $\Omega$  | 7       |
| Modulation Bandwidth                 | BW         |                  | 200          |              | kHz         | 7       |
| <b>Operating Temperature</b>         |            |                  |              |              |             |         |
|                                      | $T_{OP}$   | -40              |              | +85          | $^{\circ}C$ | 1,3     |
| <b>Package Size</b>                  |            |                  |              |              |             |         |
|                                      |            | 9.1 x 13.8 x 3.1 |              |              | mm          |         |

- See Standard Frequencies and Ordering Information (Pg 8).
- Parameters are tested with production test circuit (Pg 3).
- Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
- Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
- The  $V_C$  Model is described below (Fig 1).
- Parameters are described with waveform diagram below (Fig 2).
- Not tested in production, guaranteed by design, verified at qualification.
- For Frequencies > 600 MHz, Jitter is integrated across 50 kHz to 80 MHz.  
For Frequencies < 600 MHz, Jitter is integrated across 12 kHz to 20 MHz. (Both per GR-253-CORE Issue3).
- Tested with  $V_C = 0.3V$  to  $3.0V$ .

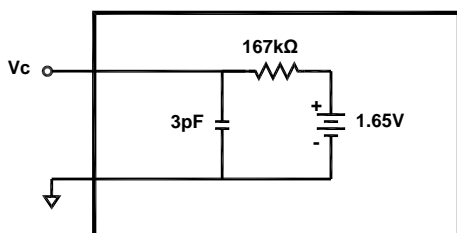


Figure 1.  $V_C$  Model – F1 or F2 Enabled

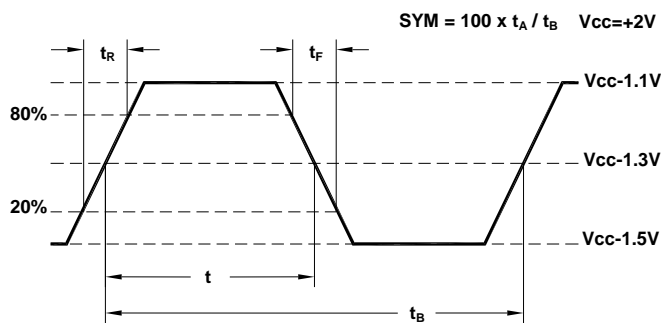


Figure 2. 10K LV-PECL Waveform

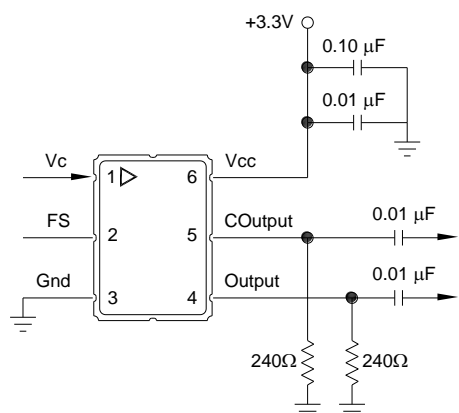
# VS-509 Dual Frequency VCSO

## Absolute Maximum Ratings

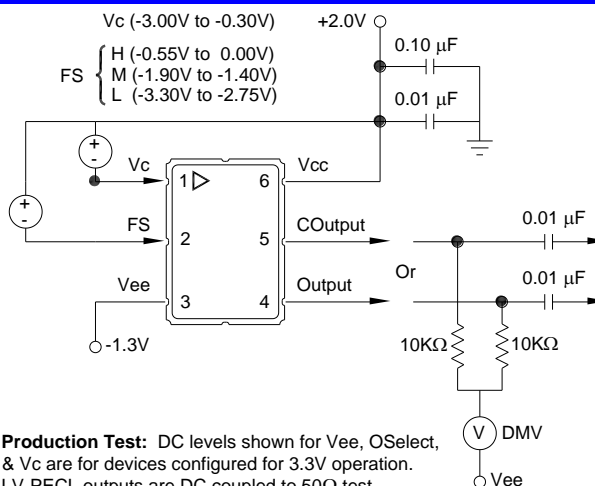
| Parameter                        | Symbol           | Ratings       | Unit     |
|----------------------------------|------------------|---------------|----------|
| Power Supply                     | $V_{CC}$         | 0 to 6        | V        |
| Input Current                    | $I_{IN}$         | 100           | mA       |
| Output Current                   | $I_{OUT}$        | 25            | mA       |
| Voltage Control Range            | $V_C$            | 0 to $V_{CC}$ | V        |
| Frequency Select                 | FS               | 0 to $V_{CC}$ | V        |
| Storage Temperature              | $T_{STR}$        | -55 to 125    | °C       |
| Soldering Temperature / Duration | $T_{PEAK} / t_P$ | 260 / 40      | °C / sec |

Stresses in excess of the absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods may adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this datasheet. Permanent damage is also possible if any device input ( $V_C$  or FS) draws >100 mA.

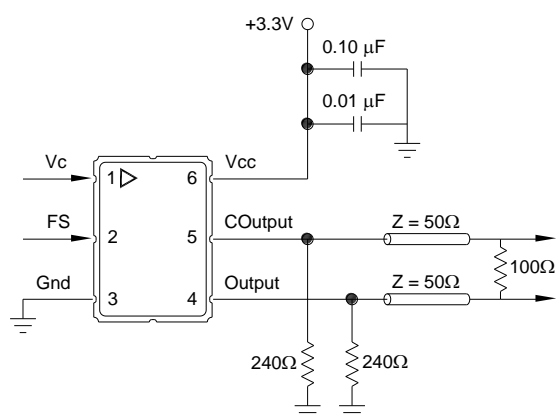
## Test Circuits & Output Load Configurations



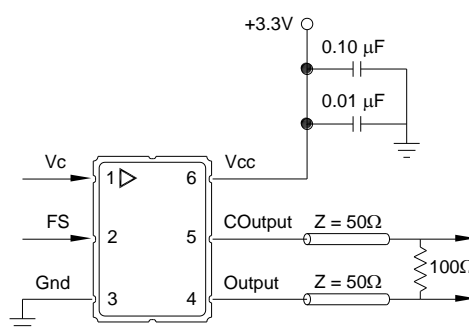
**Functional Test:** Allows use of standard power supply biasing configuration. Pull down resistors are used for LV-PECL outputs and are removed for with LVDS outputs. Since the LVDS outputs are AC coupled, the output DC levels cannot be measured.



**Production Test:** DC levels shown for Vee, OSelect, &  $V_C$  are for devices configured for 3.3V operation. LV-PECL outputs are DC coupled to 50Ω test equipment. LVDS outputs are connected to a digital volt meter, then AC coupled to the test equipment. The digital volt meter allows for Mid Level & Swing measurements.



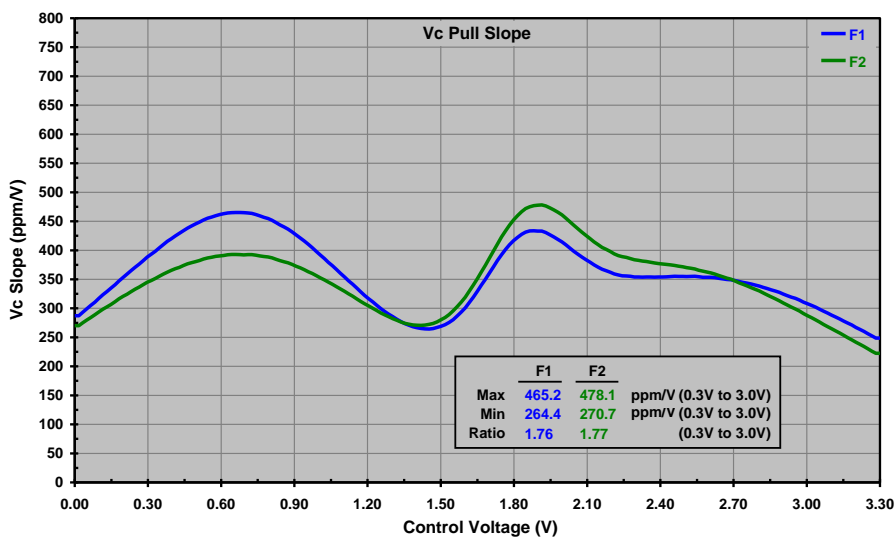
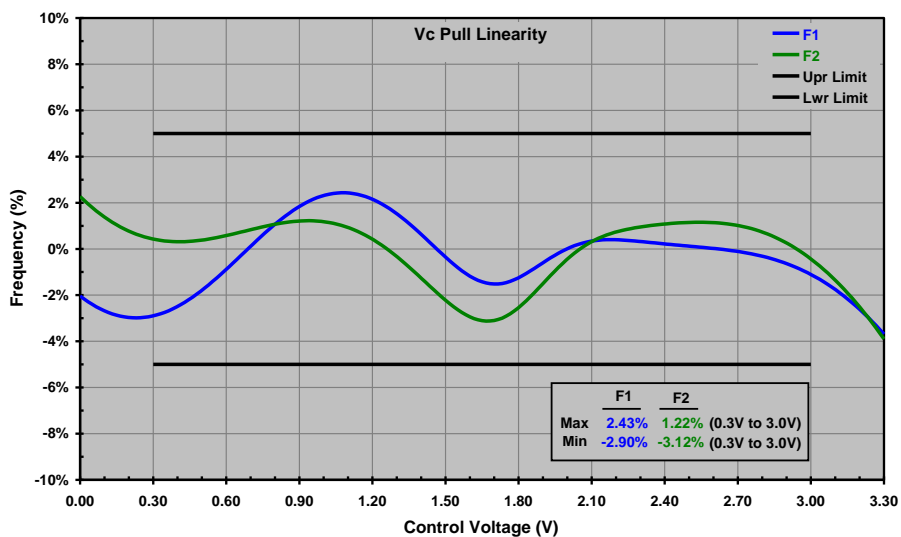
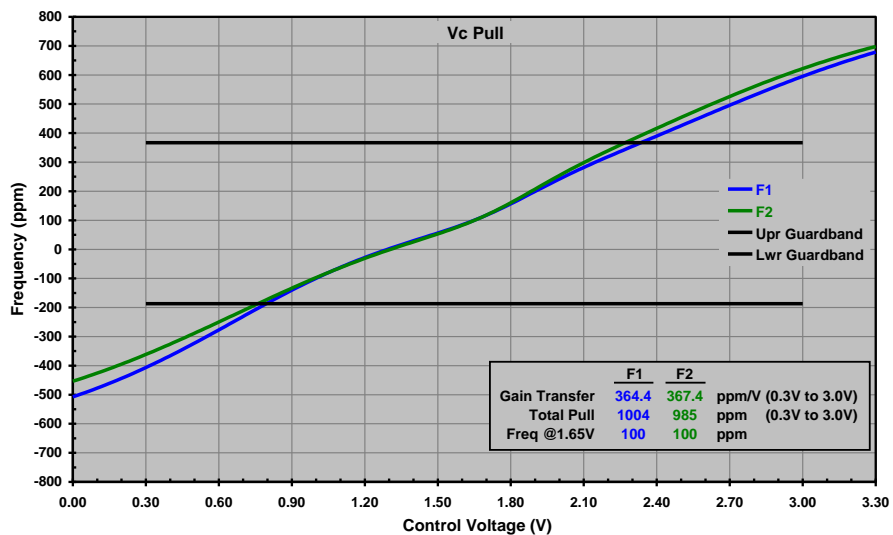
**LV-PECL to LV-PECL:** For short transmission lengths, the pull down resistor values shown provide reasonable power consumption and waveform performance.



**LVDS to LVDS:** The 100Ω resistor should be removed if this load is provided internally within the LVDS receiver.

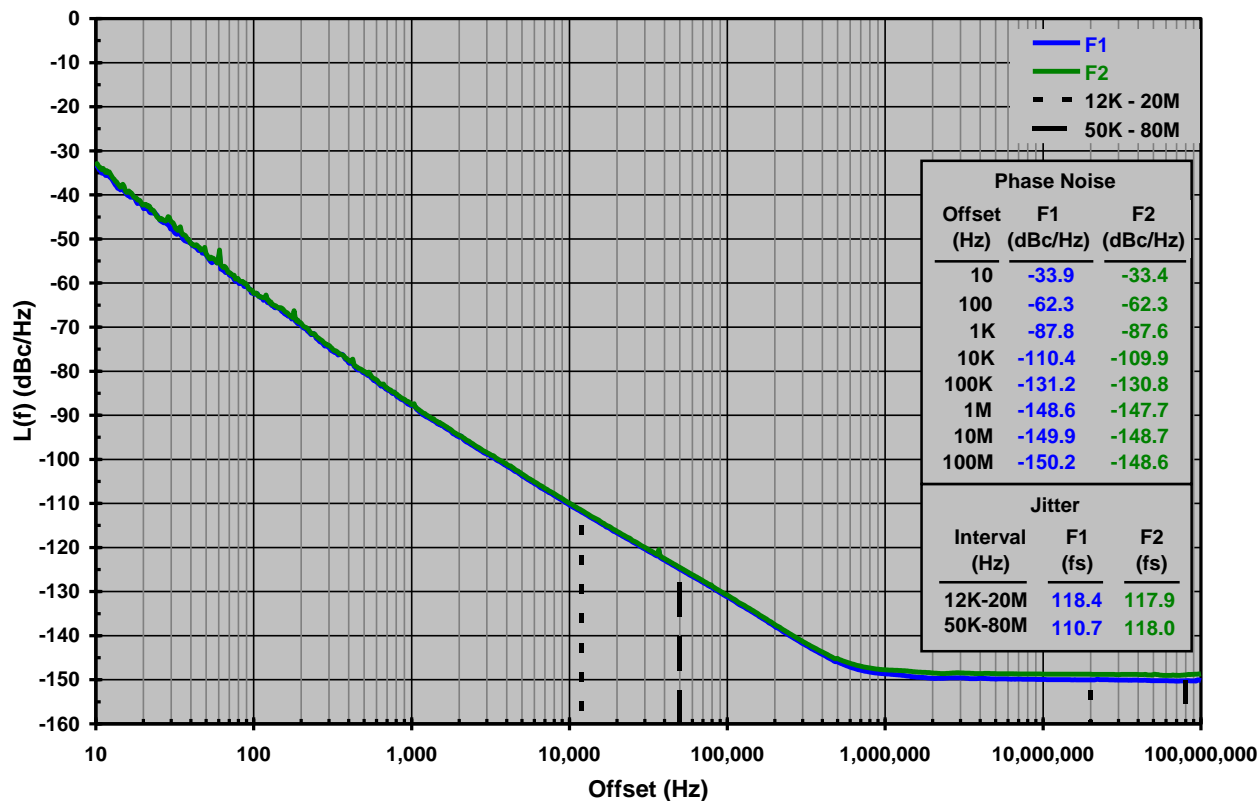
# VS-509 Dual Frequency VCSO

## Typical Characteristics: Vc Pull, Vc Pull Linearity, & Vc Pull Slope



# VS-509 Dual Frequency VCSO

## Typical Characteristics: Phase Noise & Jitter



## VS-509 Dual Frequency VCSO

### Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-509 family is capable of meeting the following qualification tests:

### Environmental Compliance

| Parameter                  | Conditions                 |
|----------------------------|----------------------------|
| Mechanical Shock           | MIL-STD-883, Method 2002 B |
| Mechanical Vibration       | MIL-STD-883, Method 2007 A |
| Solderability              | MIL-STD-883, Method 2003   |
| Gross and Fine Leak        | MIL-STD-883, Method 1014   |
| Resistance to Solvents     | MIL-STD-883, Method 2016   |
| Moisture Sensitivity Level | IPC/JEDEC J-STD-020, MSL1  |

### Handling Precautions

Although ESD protection circuitry has been designed into the VS-509 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

### ESD Ratings

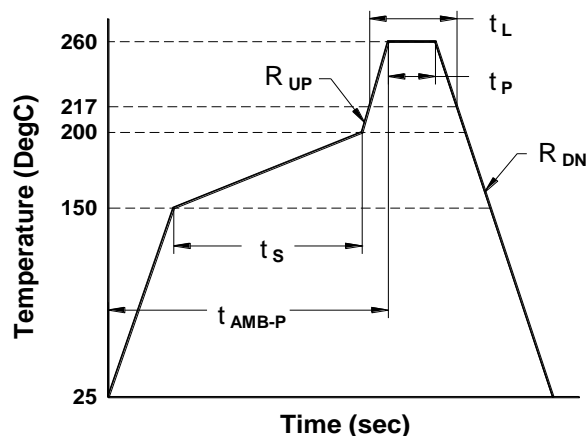
| Model                | Minimum | Conditions               |
|----------------------|---------|--------------------------|
| Human Body Model     | 2000 V  | MIL-STD 883, Method 3015 |
| Charged Device Model | 1000 V  | JEDEC, JESD22-C101       |
| Machine Model        | 200 V   | JEDEC, JESD22-A115-A     |

### Reflow Profile (IPC/JEDEC J-STD-020)

| Parameter                | Symbol      | Value                   |
|--------------------------|-------------|-------------------------|
| PreHeat Time             | $t_s$       | 60 sec Min, 180 sec Max |
| Ramp Up                  | $R_{UP}$    | 3 °C/sec Max            |
| Time Above 217 °C        | $t_L$       | 60 sec Min, 150 sec Max |
| Time To Peak Temperature | $t_{AMB-P}$ | 480 sec Max             |
| Time At 260 °C           | $t_P$       | 20 sec Min, 40 sec Max  |
| Ramp Down                | $R_{DN}$    | 6 °C/sec Max            |

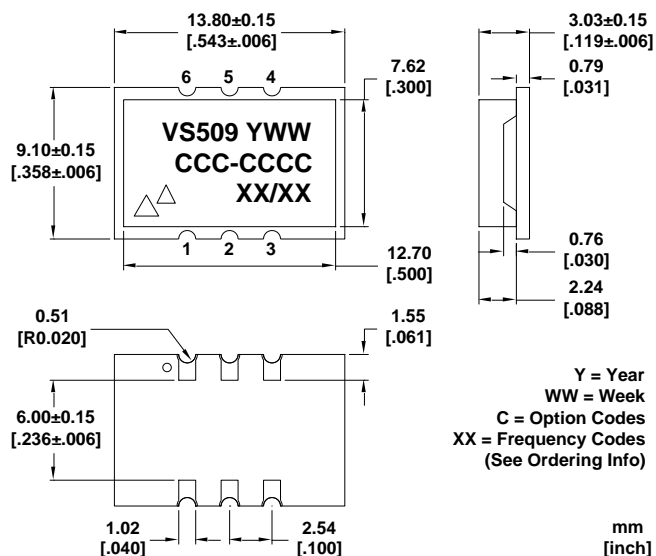
The VS-509 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The VS-509 should not be subjected to a wash process that will immerse it in solvents. NO CLELAN is the recommended procedure. The VS-509 is designed for pick and place soldering. It should be reflowed once on topside position only.

Terminal Plating: ENIG per IPC-4552  
 Electroless Ni = 3 - 6  $\mu$ m  
 Immersion Au = 0.05  $\mu$ m Min

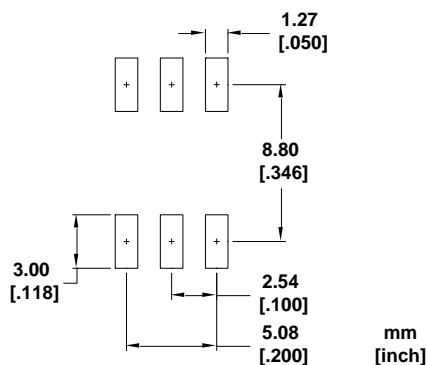


# VS-509 Dual Frequency VCSO

## Outline & Marking Diagram



## Suggested Pad Layout



## Pin Out

| Pin | Symbol          | Function                   |
|-----|-----------------|----------------------------|
| 1   | V <sub>c</sub>  | Control Voltage            |
| 2   | FS              | Frequency Select           |
| 3   | GND             | Case and Electrical Ground |
| 4   | Output          | Output                     |
| 5   | COutput         | Complementary Output       |
| 6   | V <sub>cc</sub> | Power Supply Voltage       |

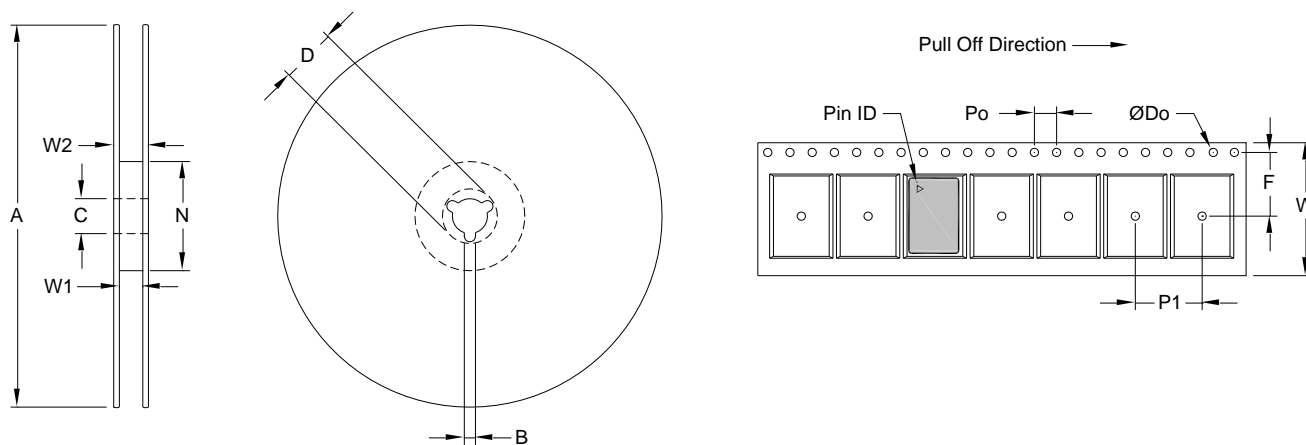
## Frequency Select (Tri-State LV-CMOS)

| FS | Voltage Range                                    | Result |
|----|--|--------|
| H  | (5V <sub>cc</sub> / 6) to V <sub>cc</sub>        | F2     |
| M  | (V <sub>cc</sub> / 2) ± 15%(V <sub>cc</sub> / 2) | OD     |
| L  | Gnd to (V <sub>cc</sub> / 6)                     | F1     |

LV-CMOS Tri-State Control

Floating FS Results in F2 (VS550 Compatibility) or in OD (VS709 Compatibility), See Order Options

## Tape and Reel (EIA-481-2-A)



## Tape Dimensions (mm)

## Reel Dimensions (mm)

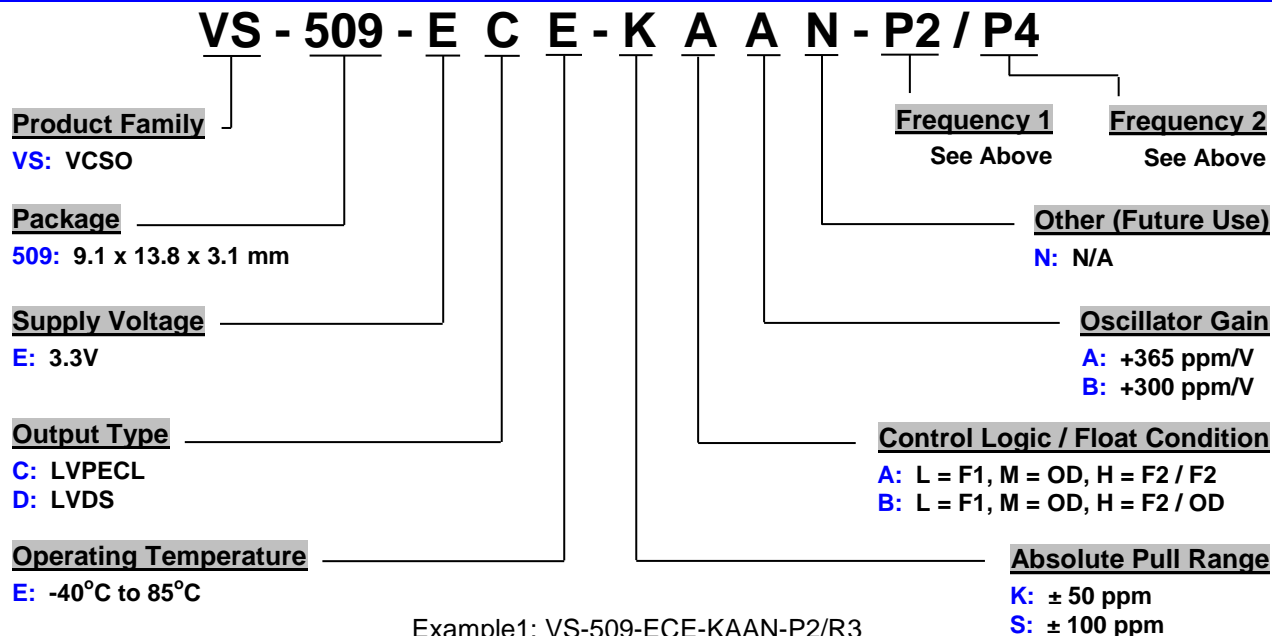
| Dimension | W   | F    | Do  | Po  | P1  | A   | B   | C   | D    | N   | W1   | W2   | # Per Reel |
|-----------|-----|------|-----|-----|-----|-----|-----|-----|------|-----|------|------|------------|
| Tolerance | Typ | Typ  | Typ | Typ | Typ | Typ | Min | Typ | Min  | Min | Typ  | Max  | Reel       |
| VS-509    | 24  | 11.5 | 1.5 | 4   | 12  | 330 | 1.5 | 13  | 20.2 | 100 | 24.4 | 30.4 | 200        |

# VS-509 Dual Frequency VCSO

| Standard Frequencies (MHz) |                      |                      |                      |                      |                      |
|----------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| 155.520000 <b>M2</b>       | 156.250000 <b>M3</b> | 161.132813 <b>M4</b> | 166.628572 <b>M5</b> | 167.331646 <b>N2</b> | 168.040678 <b>N3</b> |
| 173.370748 <b>ND</b>       | 184.320000 <b>NH</b> | 307.200000 <b>RX</b> | 311.040000 <b>P1</b> | 368.640000 <b>RY</b> | 614.400000 <b>RG</b> |
| 622.080000 <b>P2</b>       | 625.000000 <b>P3</b> | 644.531250 <b>P4</b> | 657.421875 <b>PB</b> | 666.514286 <b>P5</b> | 669.326582 <b>R3</b> |
| 672.162712 <b>R5</b>       | 690.569196 <b>R4</b> | 693.482991 <b>R6</b> | 696.421478 <b>V1</b> | 696.614900 <b>V8</b> | 707.352650 <b>TC</b> |
| 718.863800 <b>V6</b>       | 737.280000 <b>TL</b> | 905.499558 <b>V7</b> |                      |                      |                      |
|                            |                      |                      |                      |                      |                      |
|                            |                      |                      |                      |                      |                      |

Other Frequencies Available Upon Request.  
 Frequency F1 Must Be Lower Than Frequency F2.  
 Frequencies F1 & F2 Must Be Selected Within One Frequency Range: (150 - 250),(300 - 500),(600 - 1000)

## Ordering Information



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## VS-509 Dual Frequency VCSO

### Revision History

| Date      | Approved | Description   |
|-----------|----------|---|
| 11Mar2010 | JM, BW   | Preliminary Release   |
| 18Mar2010 | JM       | Corrected Pin1 ID on Outline and Changed Floating FS to F2                            |
| 04May2010 | JM       | Changed Pin1 ID on Cover and Increased Outline Height (24 Mil Pcb to 31 Mil Pcb)      |
| 30Jul2010 | JM       | Added Typ Low Gain on pg2, Float Condition Text on pg7 and its Ordering Option on pg8 |
| 16Aug2010 | JM       | Changed Standard Gain to +365 ppm/V, Removed Vc Pull Plots                            |
| 29Oct2010 | JM       | Removed 2.5V option, Added Vc Pull & Phase Noise Plots                                |
| 30Mar2011 | BW       | Official Release  |
| 02Mar2014 | MK       | Vectron Logo changed, Vectron Address Shanghai changed                                |