YSO1552MK

扬兴晶振

给您一颗快乐的"芯"！

Features

- 32.768 kHz ±5, ±10, ±20 ppm frequency stability options over temp
- World's smallest TCXO in a 1.5 x 0.8 mm CSP
- Operating temperature ranges: 0°C to +70°C , -40°C to +85°C
- Ultra-low power: <1 µA
- Vdd supply range: 1.5V to 3.63V
- Improved stability reduces system power with fewer network timekeeping updates
- NanoDrive™ programmable output swing for lowest power and direct XTAL SoC input interface
- Internal filtering eliminates external Vdd bypass cap and saves space

Applications

- Smart Meters (AMR), Health and Wellness Monitors
- Pulse-per-Second (pps) Timekeeping, RTC Reference Clock

TempFlat
MEMS™

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	Fout		32.768		kHz	
Frequency Stability Over Temperature [1] (without Initial Offset [2])	F_stab	-5.0		5.0	ppm	
		-10		10		
		-20		20		
Frequency Stability Over Temperature (with Initial Offset [2])	F_stab	-10		10	ppm	
		-13		13		
		-22		22		
Frequency Stability vs Voltage	F_vdd	-0.75		0.75	ppm	1.8V ±10%
		-1.5		1.5	ppm	1.5V – 3.63V
First Year Frequency Aging	F_aging	-1.0		1.0	ppm	T_A = 25°C, Vdd = 3.3V
Jitter Performance (T_A = over temp)						
Long Term Jitter				2.5	μs_{pp}	81920 cycles (2.5 sec), 100 samples
Period Jitter			35		ns_{RMS}	Cycles = 10,000, T_A = 25°C, Vdd = 1.5V – 3.63V
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.5		3.63	V	T_A = -40°C to +85°C
Core Supply Current [3]	Idd		0.99		µA	T_A = 25°C, Vdd = 1.8V, LVCMOS Output configuration, No Load
				1.52		T_A = -40°C to +85°C, Vdd = 1.5V – 3.63V, No Load
Power-Supply Ramp	t_Vdd_Ramp			100	ms	Vdd Ramp-Up 0 to 90% Vdd, T_A = -40°C to +85°C
Start-up Time at Power-up	t_start		180	300	ms	T_A = -40°C +60°C, valid output
				350		T_A = +60°C to +70°C, valid output
				380		T_A = +70°C to +85°C, valid output

Notes:

1. No board level underfill. Measured as peak-to-peak/2. Inclusive of 3x-reflow and ±20% load variation. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.

2. Initial offset is defined as the frequency deviation from the ideal 32.768 kHz at room temperature, post reflow.

3. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + output driver operating current, which is a function of the output voltage swing. See the description titled, **Calculating Load Current.**

YSO1552MK

Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Temperature Range						
Commercial Temperature	Op_Temp	0		70	°C	
Industrial Temperature		-40		85	°C	
LVCMOS Output						
Output Rise/Fall Time	tr, tf		100	200	ns	10-90% (Vdd), 15 pF Load
				50		10-90% (Vdd), 5 pF Load, Vdd ≥ 1.62V
Output Clock Duty Cycle	DC	48		52	%	
Output Voltage High	VOH	90%			V	Vdd: 1.5V – 3.63V. I_{OH} = -1 µA, 15 pF Load
Output Voltage Low	VOL			10%	V	Vdd: 1.5V – 3.63V. I_{OL} = 1 µA, 15 pF Load
NanoDrive™ Reduced Swing Output						
Output Rise/Fall Time	tf, tf			200	ns	30-70% (V_{OL}/V_{OH}), 10 pF Load
Output Clock Duty Cycle	DC	48		52	%	
AC-coupled Programmable Output Swing	V_sw		0.20 to 0.80		V	YSO1552MK does not internally AC-couple. This output description is intended for a receiver that is AC-coupled. Vdd: 1.5V – 3.63V, 10 pF Load, I_{OH} / I_{OL} = ±0.2 µA
DC-Biased Programmable Output Voltage High Range	VOH		0.6 to 1.225		V	Vdd: 1.5V – 3.63V. I_{OH} = -0.2 µA, 10 pF Load
DC-Biased Programmable Output Voltage Low Range	VOL		0.35 to 0.80		V	Vdd: 1.5V – 3.63V. I_{OL} = 0.2 µA, 10 pF Load
Programmable Output Voltage Swing Tolerance		-0.055		0.055	V	T_A = -40°C to +85°C, Vdd = 1.5V to 3.63V.

Pin Configuration

CSP Pin	Symbol	I/O	Functionality
1, 4	GND	Power Supply Ground	Connect to ground. All GND pins must be connected to power supply ground. The GND pins can be connected together, as long as both GND pins are connected ground.
2	CLK Out	OUT	Oscillator clock output. When interfacing to an MCU's XTAL, the CLK Out is typically connected to the receiving IC's X IN pin. The YSO1552MK oscillator output includes an internal driver. As a result, the output swing and operation is not dependent on capacitive loading. This makes the output much more flexible, layout independent, and robust under changing environmental and manufacturing conditions.
3	Vdd	Power Supply	Connect to power supply 1.5V ≤ Vdd ≤ 3.63V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). For more information about the internal power-supply filtering, see *Power-Supply Noise Immunity* section in the detailed description.. Contact factory for applications that require a wider operating supply voltage range.

CSP Package (Top View)

GND [1] [4] GND

CLK Out [2] [3] Vdd
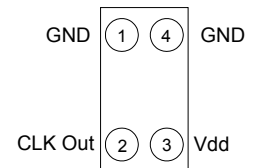
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)

1.55 x 0.85 mm CSP

1.54 ±0.02
0.84 ±0.02
#4 #3
#1 #2
0.04
Polymer coating
0.60 MAX

0.315 ±0.015
#3 #4
#2 #1
0.41 BSC
1.00 BSC

∅0.25 (4x) NSMD pads
#4 #3
#1 #2
0.41
1.00
∅0.35 (4x) Soldermask openings
(soldermask openings shown with heavy dashed line)

Recommend 4-mil (0.1mm) stencil thickness

PART Number Guide

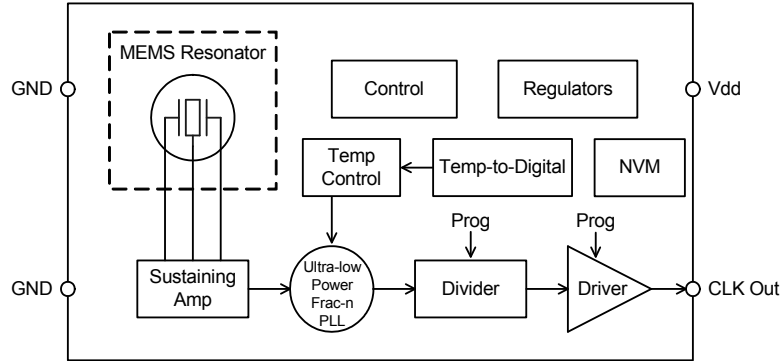| Quartz Crystal Oscillator	Dimensions	Frequency (Hz)	Frequency Stability Overall (ppm)	Output	Pin	Material	Operating Temp. Range
O	1508	32768K	S	D14	4	M	I

YSO1552MK

System Block Diagram

Figure 1.

Absolute Maximum

Attempted operation outside the absolute maximum ratings cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	≤30 minutes	4.0	V
Continuous Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V	105	°C
Short Duration Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V, ≤30 mins	125	°C
Human Body Model (HBM) ESD Protection	JESD22-A114	3000	V
Charge-Device Model (CDM) ESD Protection	JESD22-A115	750	V
Machine Model (MM) ESD Protection	JESD22-C101	300	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	g
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
1508 CSP Junction Temperature		150	°C
Storage Temperature		-65°C to 150°C	

YSO1552MK

TCXO Frequency Stability

The YSO1552MK is factory calibrated (trimmed) over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover pointwith a 0.04 ppm/C^2 temperature coefficient, the YSO1552MK temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range. When measuring the YSO1552MK output frequency with a frequency counter, it is important to make sure the counter's gate time is >100 ms. The slow frequency of a 32kHz clock will give false readings with faster gate times.

Power Supply Noise Immunity

In addition to eliminating external output load capacitors common with standard XTALs, this device includes special power supply filtering and thus, eliminates the need for an external Vdd bypass-decoupling capacitor to keep the footprint as small as possible. Internal power supply filtering is designed to reject more than ±150 mV noise and frequency components from low frequency to more than 10 MHz.

Start-up and Steady-State Supply Current

The YSO1552MK TCXO starts-up to a valid output frequency within 300 ms (180 ms typ). To ensure the device starts-up within the specified limit, make sure the power-supply ramps-up in approximately 10 - 20 ms (to within 90% of Vdd). During initial power-up, the YSO1552MK power-cycles internal blocks, as shown in the power-supply start-up and steady state plot in the *Typical Operating Curves* section. Power-up and initialization is typically 200 ms, and during that time, the peak supply current reaches 28 μA as the internal capacitors are charged, then sequentially drops to its 990 nA steady-state current. During steady-state operation, the internal temperature compensation circuit turns on every 350 ms for a duration of approximately 10 ms.

Output Voltage

The YSO1552MK has two output voltage options. One option is a standard LVCMOS output swing. The second option is the NanoDrive reduced swing output. Output swing is customer specific and Factory programmed between 200 mV and 800 mV. For DC-coupled applications, output V_{OH} and V_{OL} are individually factory programmed to the customers' requirement. V_{OH} programming range is between 600 mV and 1.225V in 100 mV increments. Similarly, V_{OL} programming range is between 350 mV and 800 mV. For example; a PMIC or MCU is internally 1.8V logic compatible, and requires a 1.2V V_{IH} and a 0.6V V_{IL}. Simply select YSO1552MK NanoDrive factory programming code to be "D14" and the correct output thresholds will match the downstream PMIC or MCU input requirements. Interface logic will vary by manufacturer and we recommend that you review the input voltage requirements for the input interface.

For DC-biased NanoDrive output configuration, the minimum V_{OL} is limited to 350mV and the maximum allowable swing ($V_{OH} - V_{OL}$) is 750mV. For example, 1.1V V_{OH} and 400mV V_{OL} is acceptable, but 1.2V V_{OH} and 400 mV V_{OL} is not acceptable.

When the output is interfacing to an XTAL input that is internally AC-coupled, the YSO1552MK output can be Factory programmed to match the input swing requirements. For example, if a PMIC or MCU input is internally AC-coupled and requires an 800mV swing, then simply choose the YSO1552MK NanoDrive programming code "AA8" in the part number. It is important to note that the YSO1552MK does not include internal AC-coupling capacitors.

SiT1552 NanoDrive™

Figure 2 shows a typical output waveform of the YSO1552MK (intoa 10 pF load) when factory programmed for a 0.70V swing andDC bias (V_{OH}/V_{OL}) for 1.8V logic:

Example:
- NanoDrive part number coding: D14. Example part number: O150832768KAD144MI
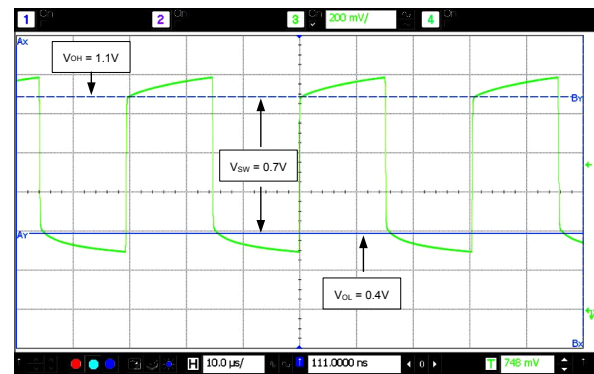- V_{OH} = 1.1V, V_{OL} = 0.4V ($V_{\_sw}$ = 0.70V)

Figure 2. O150832768KAD144MI
Output Waveform (10 pF Load)

Table 1 shows the supported NanoDrive V_{OH}, V_{OL} factory programming options.

Table 1. Acceptable V_{OH}/V_{OL} NanoDrive Levels

V_{OL}/V_{OH}	1.225	1.100	1.000	0.900	0.800	0.700	0.600
0.800	D28	D18	D08				
0.700	D27	D17	D07	D97			
0.525	D26	D16	D06	D96	D86		
0.500	D25	D15	D05	D95	D85	D75	
0.400		D14	D04	D94	D84	D74	D64
0.350		D13	D03	D93	D83	D73	D63

Table 2 shows the supported AC coupled Swing levels. The "AC-coupled" terminology refers to the programming description for applications where the downstream chipsets includes an internal AC-coupling capacitor, and therefore, only the output swing is important and V_{OH}/V_{OL} is not relevant. For these applications, refer to Table 2 for the acceptable voltage swing options.

YSO1552MK

Table 2. Acceptable NanoDrive Voltage Swing Options (for downstream AC-coupled receivers)

Swing	0.800	0.700	0.600	0.500	0.400	0.300	0.250	0.200
Output Code	AA8	AA7	AA6	AA5	AA4	AA3	AA2	AA1

Example:

- NanoDrive part number coding: AA2. Example part number: YSO150832768KAAA24MI
- Output voltage swing: 0.250V

The values listed in Tables 1 and -2 are nominal values at 25°C and will exhibit a tolerance of ±55 mV across Vdd and -40°C to 85°C operating temperature range.

SiT1552 Full Swing LVCMOS Output
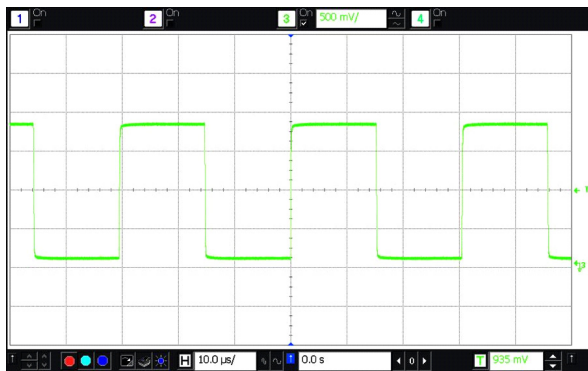
Figure 3. LVCMOS Waveform (Vdd = 1.8V) into 15 pF Load

Example:

- LVCMOS output part number coding is always **DCC**
- Example part number:O150832768KADCC4MI

Calculating Load Current

No Load Supply Current

When calculating no-load power for the YSO1552MK, the core and output driver components need to be added. Since the output voltage swing can be programmed to minimize load current,the output driver current is variable. Therefore, no-load operating supply current is broken into two sections; core and output driver. The equation is as follows:

Total Supply Current (no load) = Idd Core + Idd Output Driver

Example 1: Full-swing LVCMOS

- Vdd = 1.8V
- Idd Core = 990nA (typ)
- $Vout_{pp}$ = 1.8V
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(1.8V)(32768Hz) = 206nA

Supply Current = 990nA + 206nA = 1.2µA

Example 2: NanoDrive Reduced Swing

- Vdd = 1.8V
- Idd Core = 990nA (typ)
- $Vout_{pp}$ (Programmable) = $V_{OH} - V_{OL}$ = 1.1V - 0.6V = 500mV
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(0.50V)(32768Hz) = 57nA

Supply Current = 990nA + 57nA = 1.05µA

Total Supply Current with Load

To calculate the total supply current, including the load, follow the equation listed below. Note the 30% reduction in power with NanoDrive.

Total Current = Idd Core + Idd Output Driver + Load Current

Example 1: Full-swing LVCMOS

- Vdd = 1.8V
- Idd Core = 990nA
- Load Capacitance = 10pF
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(1.8V)(32768Hz) = 206nA
- Load Current: (10pF)(1.8V)(32768Hz) = 590nA
- Total Current = 990nA + 206nA + 590nA = 1.79µA

Example 2: NanoDrive Reduced Swing

- Vdd = 1.8V
- Idd Core = 990nA
- Load Capacitance = 10pF
- $Vout_{pp}$ (Programmable): $V_{OH} - V_{OL}$ = 1.1V - 0.6V = 500mV
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(0.5V)(32768Hz) = 57nA
- Load Current: (10pF)(0.5V)(32768Hz) = 164nA
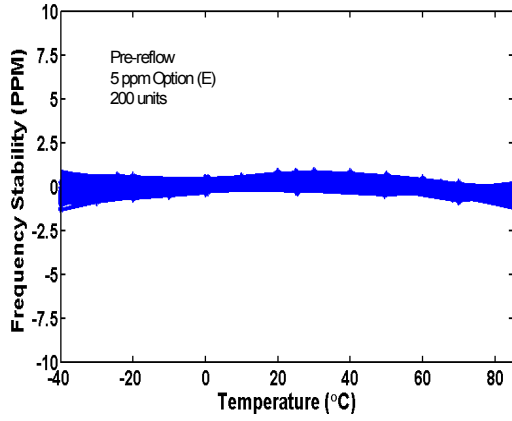- Total Current = 990nA + 57nA + 164nA = 1.2µA

YSO1552MK

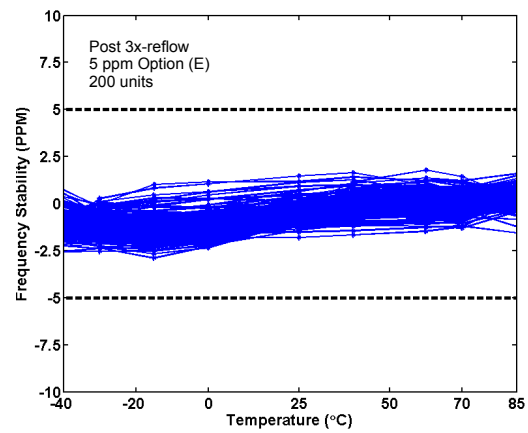## Typical Operating Curves

(T_A = 25°C, Vdd = 1.8V, unless otherwise stated)

Frequency Stability Over Temperature (Pre-Reflow)
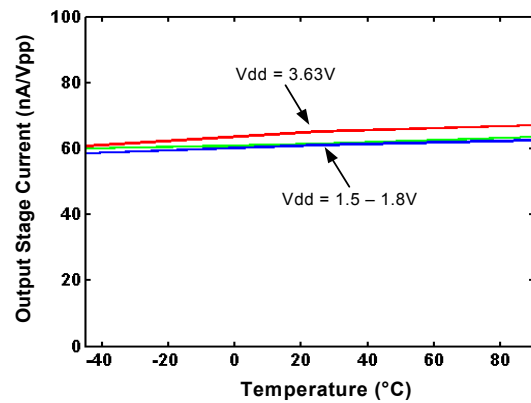

Pre-reflow
5 ppm Option (E)
200 units

Frequency Stability Over Temperature (Post-Reflow)

Post 3x-reflow
5 ppm Option (E)
200 units

Core Current Over Temperature

Vdd = 3.63V

Vdd = 1.5 – 1.8V
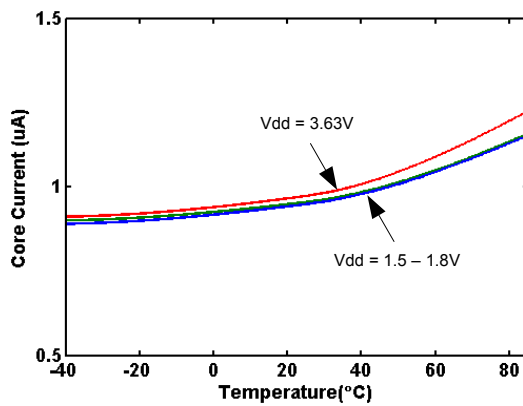
Output Stage Current Over Temperature (NanoDrive Output)

Vdd = 3.63V

Vdd = 1.5 – 1.8V

Total Supply Current Over Temperature, LVCMOS (Core + LVCMOS Output Driver, No Load)

Vdd = 3.63V

Vdd = 1.5 – 1.8V
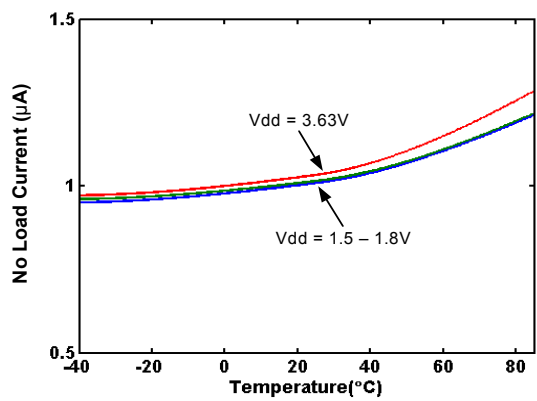
Start-up and Steady-State Current Profile

Internal Caps Charging (28µA Max)

Logic Start-up

NVM Read

Osc Start-up

Temperature Compensation (6µA)

350ms

Steady State

YSO1552MK
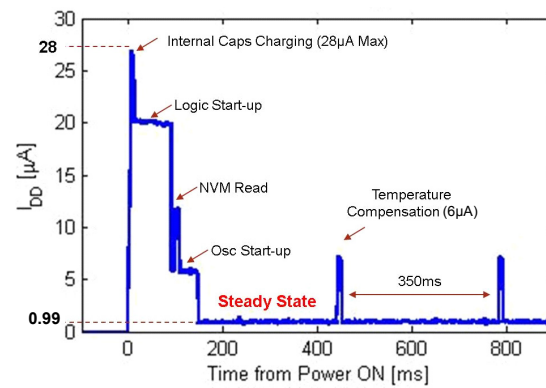
给您一颗快乐的"芯"！

Power Supply Noise Rejection
(±150mV Noise)

Vdd 1.8V

Vdd 3.3V

Frequency Error (ppm)

Noise Injection Frequency (Hz)
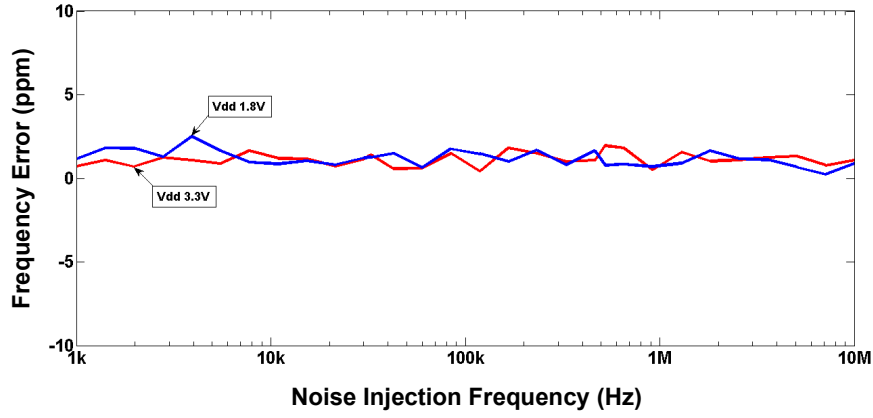
Temperature Ramp Response

Temperature (°C)

1.5°C/s

Temperature Ramp

Time (s)

TCXO Response

Frequency Stability (ppm)

Time (s)
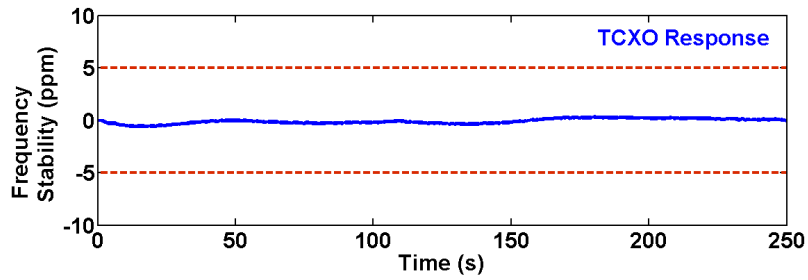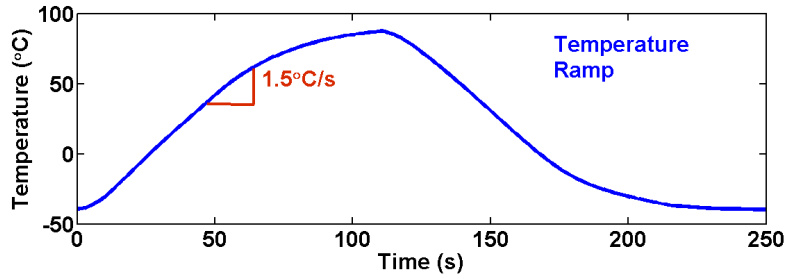
NanoDrive™ Output Waveform
(V_{OH} = 1.2V, V_{OL} = 0.4V, 10 pF Load; O150832768KAD144MI)

V_{OH} = 1.1V

V_{SW} = 0.7V

V_{OL} = 0.4V
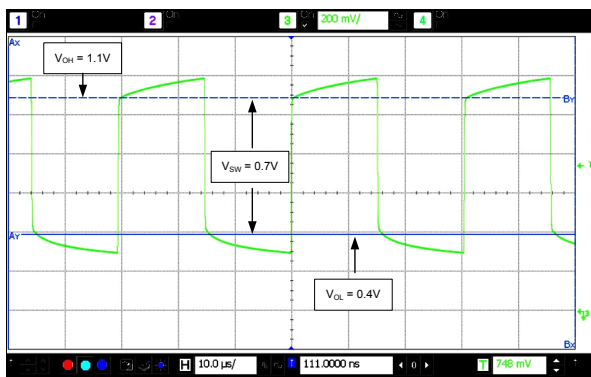
LVCMOS Output Waveform
(Vswing = 1.8V, O150832768KADCC4MI)