F10010 • F10016

BCD DECADE COUNTER/4-BIT BINARY COUNTER

GENERAL DESCRIPTION — The F10010 is a high-speed synchronous, presettable, cascadable BCD Decade Counter and the F10016 is a high-speed synchronous, presettable, cascadable 4-Bit Binary Counter. They are multifunction MSI building blocks useful for a large number of counting, digital integration, and conversion applications. Up to nine devices can be cascaded with no speed degradation using standard 10K gates. A multidecade synchronous counter up to 150 MHz can be built. Typical count frequency is 200 MHz.

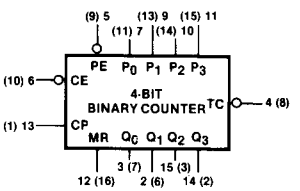
Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

- **HIGH SPEED COUNT . . . 200 MHz TYPICAL COUNT FREQUENCY**
- **INTERNAL COUNT ENABLE—FOR HIGHEST SPEED EXPANSION**
- **ASYNCHRONOUS MASTER RESET**
- **50 Ω DRIVE CAPABILITY**
- **WIRED-OR CAPABILITY**
- **SEPARATE V_{CC} PINS—ELIMINATE NOISE COUPLING**
- **INTERNAL 50 kΩ INPUT PULL DOWNS**
- **SINGLE −5.2 V POWER SUPPLY**

PIN NAMES

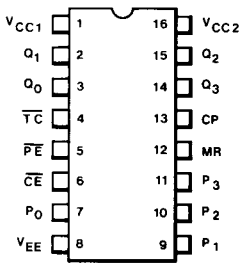
$\overline{PE}$	Parallel Load Enable (Active LOW)
P_n	Parallel Inputs
CP	Clock Input (Clocks on Positive Transition)
$\overline{CE}$	Count Enable (LOW to Count)
MR	Master Reset (HIGH Forces all Q Outputs LOW)
$\overline{TC}$	Terminal Count (10010, LOW at HLLH; 10016 LOW at HHHH)
Q_n	Counter Outputs

LOGIC SYMBOL

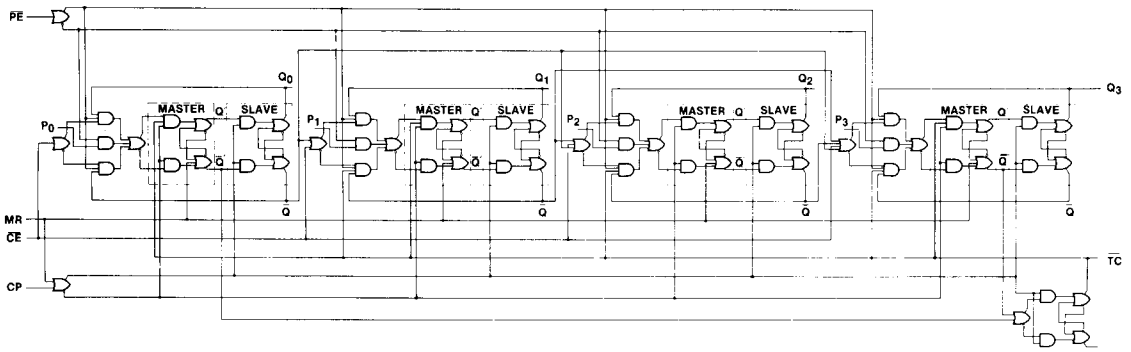


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

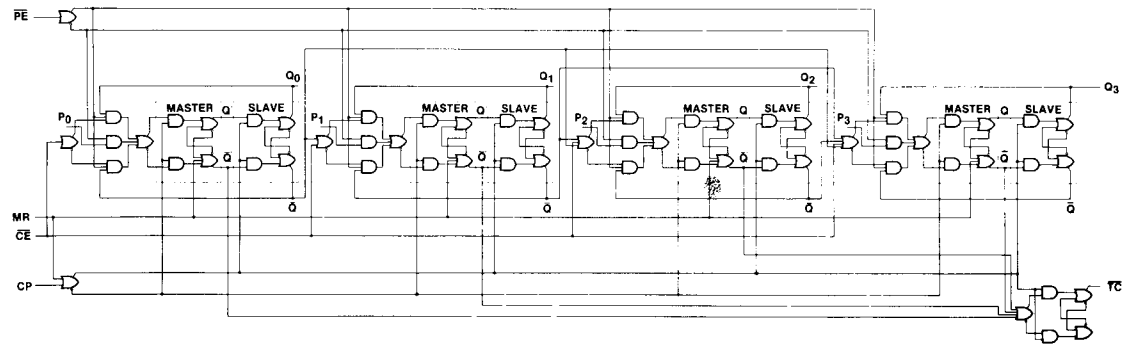
CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



LOGIC DIAGRAM F10010



LOGIC DIAGRAM F10016



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

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FUNCTIONAL DESCRIPTION — The F10010 is a high-speed BCD Decade Counter and the F10016 is a high-speed Binary Counter. The four master/slave flip-flops are fully synchronous and are driven in parallel through a clock driver. The masters are loaded during the LOW period of the clock pulse. During the LOW to HIGH transition of the clock, the master is disabled from the input and data is transferred to the slaves and then to the outputs. When the clock is HIGH, the masters are inhibited from changing and the master/slave data path remains open. During the HIGH to LOW transition of the clock, the master/slave data path is inhibited, followed by the enabling of the masters for the acceptance of inputs from the counting logic, parallel entry, or count hold logic.

The Terminal Count ($\overline{TC}$) is generated at count 9 (HLLH) on the 10010 and at count 15 (HHHH) on the 10016.

The $\overline{TC}$ output is available simultaneously with the Q outputs through the use of unique lookahead logic and a fifth slave which is loaded during the LOW portion of the clock cycle. This feature, in conjunction with the triggered Count Enable ($\overline{CE}$) and the Parallel Enable ($\overline{PE}$) select the mode of operation as shown in the table next page. The status of these control lines is sampled only during the LOW to HIGH transition of the clock.

The Master Reset (MR) function is asynchronous. When HIGH, it overrides all other commands and forces all Q outputs LOW and the $\overline{TC}$ HIGH.

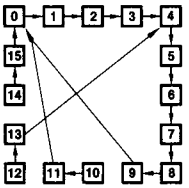
TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	Z	Load Parallel (P_n to Q_n)
H	L	L	Z	Load Parallel (P_n to Q_n)
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Masters Respond; Slaves Hold
X	X	H	X	Reset (Q_n = LOW, $\overline{TC}$ = HIGH)

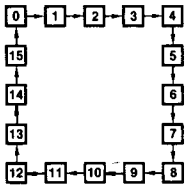
L = LOW
H = HIGH Voltage Level
X = Don't Care
Z = Clock Pulse (LOW to HIGH)
ZZ = Clock Pulse (HIGH to LOW)

STATE DIAGRAMS

F10010



F10016



NOTE: The 10010 can be preset to any state, but will not count beyond 9 (HLLH). If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

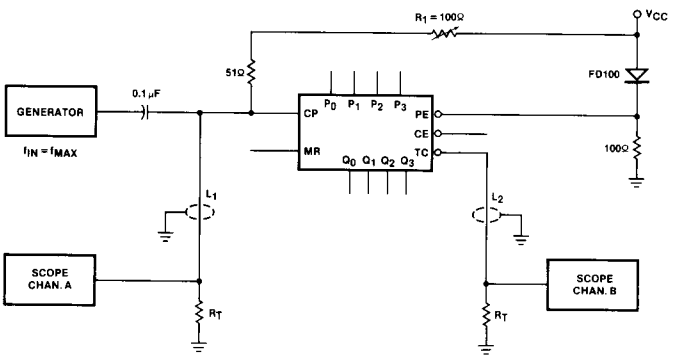
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

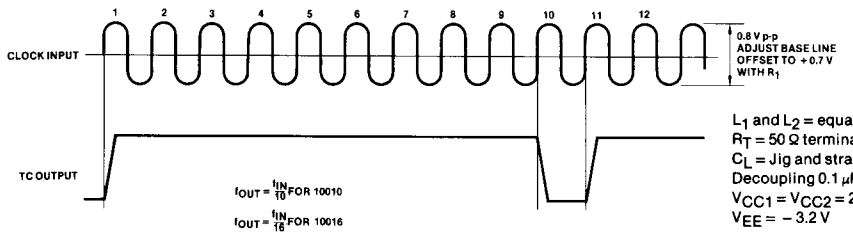
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH MR (Pin 12)			265 700	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−115	−80		mA	25°C	Outputs Open, Pin 12 Tied to V_{IH}

SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
f_{count}	Count Frequency	140	200		MHz	See Figure 1
t_{PLH}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	See Figure 2
t_{PHL}	Propagation Delay Clock to Output (Q_n or $\overline{TC}$)	2.0	3.6	5.0	ns	
t_{PHL}	Propagation Delay Master Reset to Output		4.0		ns	See Figure 3
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)	1.3	2.5	3.3	ns	See Figure 2
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)	1.3	2.5	3.3	ns	
t_w	Clock Pulse Width		2.3		ns	See Figure 2
t_w	MR Pulse Width		2.8		ns	See Figure 3
t_s	Set-Up Time Prior to Clock P_n to CP	2.0			ns	
t_h	Hold Time After Clock P_n to CP	1.0			ns	
t_s	Set-Up Time Prior to Clock PE or CE to CP	2.5			ns	
t_h	Hold Time After Clock PE or CE to CP	0.5			ns	

SWITCHING CIRCUITS AND WAVEFORMS

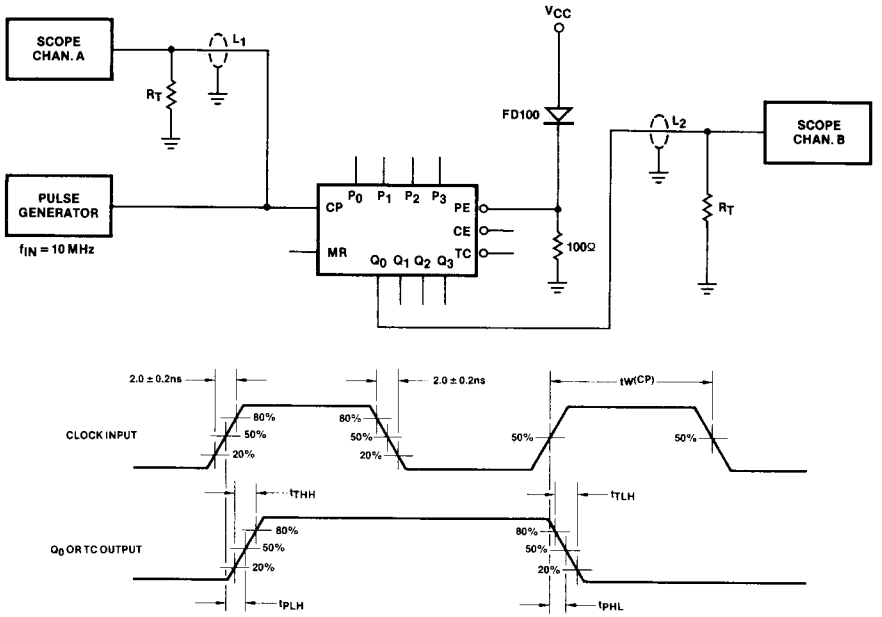




L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

Fig. 1. Maximum Count Frequency

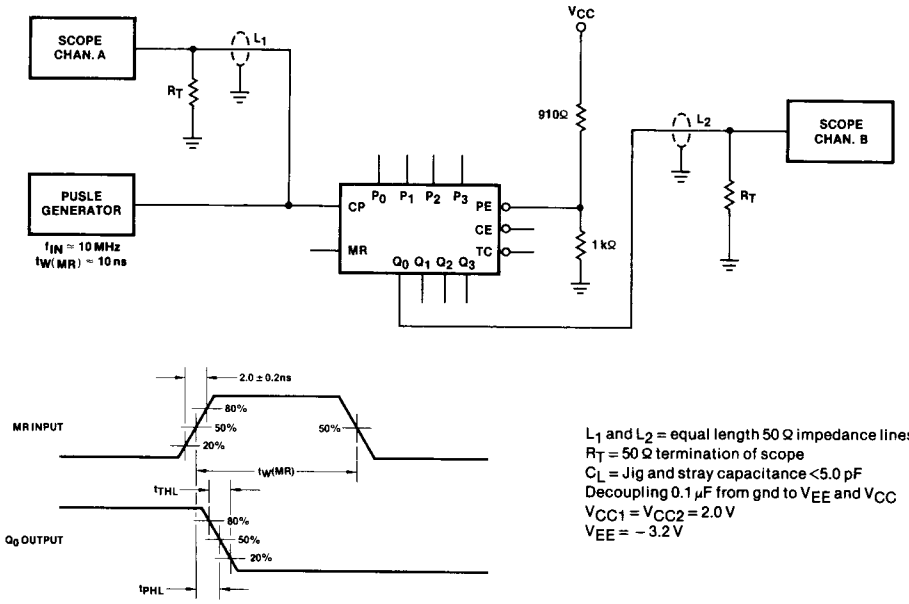
SWITCHING CIRCUITS AND WAVEFORMS (Cont'd)



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF

Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

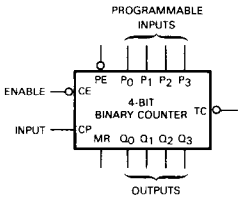
Fig. 2. Clock to Output



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V

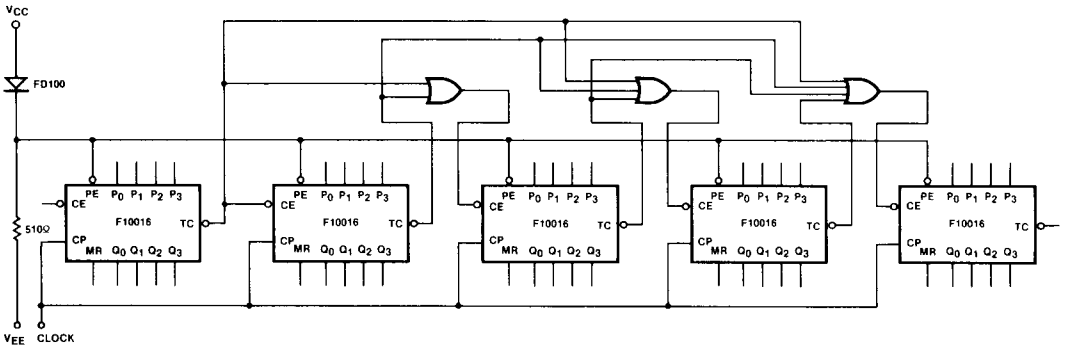
Fig. 3. Master Reset to Output

APPLICATION INFORMATION



DIVIDE RATIO	INPUT REQUIRED			
	P_0	P_1	P_2	P_3
2	L	H	H	H
3	H	L	H	H
4	L	L	H	H
5	H	H	L	H
6	L	H	L	H
7	H	L	L	H
8	L	L	L	H
9	H	H	H	L
10	L	H	H	L
11	H	L	H	L
12	L	L	H	L
13	H	H	L	L
14	L	H	L	L
15	H	L	L	L
16	L	L	L	L

The F10016 may be connected to divide by any modulo from 2 to 16. The table illustrates the inputs required for each modulo. The terminal count output is utilized to load the parallel data, this in turn determines the number of clock pulses which will occur before $\overline{TC}$ goes LOW again.



CASCADE COUNTERS USING OR GATES FOR CARRY PROPAGATION

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