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ECL Products	

100165

Universal Priority Encoder

FEATURES

- **Typical propagation delay: 2.5ns**
- **Typical supply current ($-I_{EE}$): 125mA**

DESCRIPTION

100165 is a Universal Priority Encoder with latches on the inputs. A Mode Control line (M) determines one of two possible modes of operation: When M is High, the device functions as an 8–bit priority encoder. When M is Low, the device operates as two independent 4–bit priority encoders.

In the 8–bit encoder mode, the priority of the data input decreases in going from D_0 to D_7. Thus, D_0 has the high priority and D_7 has the lowest. The bit–pattern on the data outputs ($Q_0 - Q_2$, $\overline{Q}_0 - \overline{Q}_2$) identifies the highest priority data input at a High logic level. For expansion, the Group Signal output GS_0 can be connected to the Output Enable $\overline{OE}$ of another, lower priority 100165. Outputs Q_3, $\overline{Q}_3$ and GS_1 are not used in this mode.

In the dual 4–bit encoder mode, $D_0 - D_3$, Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$, and GS_0 are associated with one encoder; $D_4 - D_7$, Q_2, Q_3, $\overline{Q}_2$, $\overline{Q}_3$, and GS_1 are associated with the other. The priority of the data input decreases in going from D_0 to D_3 (or from D_4 to D_7). A bit–pattern on the data outputs Q_0 and Q_1 (or Q_2 and Q_3) identifies the highest priority data input at a High logic level. For expansion, GS_0 (GS_1) can be connected to the $\overline{OE}$ of another, lower priority 100165.

There is one latch at each data input (D_n). When the Enable input $\overline{E}$ is Low, these latches are transparent. When $\overline{E}$ goes High, the data at the inputs are latched. $\overline{E}$ functions the same way for both modes of operation.

When the Output Enable $\overline{OE}$ is High, $Q_0 - Q_3$ are forced to a Low logic level and GS_n are forced High. $\overline{OE}$ functions the same way for both modes of operation.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

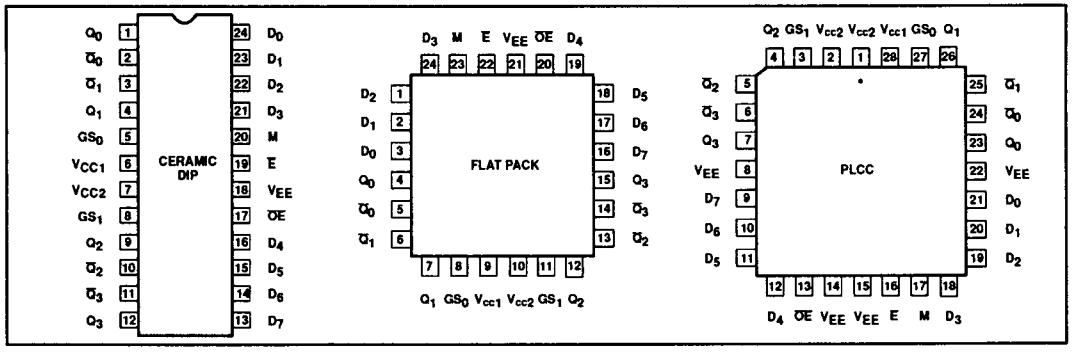
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_7$	Data Inputs
M	Mode Control Input
$\overline{E}$	Latch Enable Input (Active Low)
$\overline{OE}$	Output Enable Input (Active Low)
GS_0, GS_1	Group Signal Outputs
$Q_0 - Q_3$	True Data Outputs
$\overline{Q}_0 - \overline{Q}_3$	Complementary Data Outputs

ORDERING INFORMATION

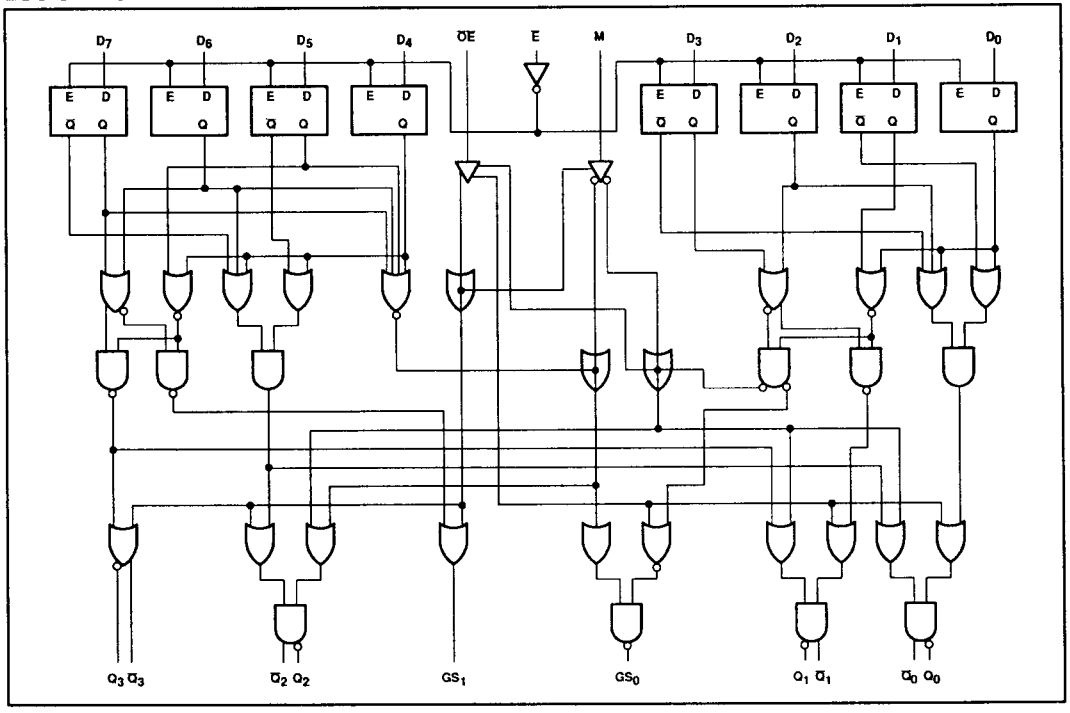
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100165F
24–Pin Ceramic Flat Pack	100165Y
28–Pin PLCC	100165A

PIN CONFIGURATIONS



Encoder | 100165

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS											OUTPUTS					
E	$\overline{OE}$	M	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_0	Q_1	Q_2	Q_3	GS_0	GS_1
L	L	L	H	X	X	X					L	L			H	
L	L	L	L	H	X	X					H	L			H	
L	L	L	L	L	H	X					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	X	X	X			L	L		H
L	L	L					L	H	X	X			H	L		H
L	L	L					L	L	H	X			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	X	X	X	X	X	X	X	L	L	L	L	H	H
L	L	H	L	H	X	X	X	X	X	X	H	L	L	L	H	H
L	L	H	L	L	H	X	X	X	X	X	L	H	L	L	H	H
L	L	H	L	L	L	H	X	X	X	X	H	H	L	L	H	H
L	L	H	L	L	L	L	H	X	X	X	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	X	X	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	X	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
H	L	L	X	X	X	X	X	X	X	X	Determined by $D_0 - D_7$ when $\overline{E}$ was Low and M = L					
H	L	H	X	X	X	X	X	X	X	X	Determined by $D_0 - D_7$ when $\overline{E}$ was Low and M = H					

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care
Blank = Not Applicable

ABSOLUTE MAXIMUM RATINGS

$V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	−7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	−55	mA
T_S	Storage temperature range	−65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		−4.8	−4.5	−4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		−5.7			V
V_{IH}	High level input voltage	V_{EE} = −4.2V	−1150		−880	mV
		V_{EE} = −4.5V	−1165			
		V_{EE} = −4.8V	−1165			
V_{IL}	Low level input voltage	V_{EE} = −4.2V	−1810		−1475	mV
		V_{EE} = −4.5V			−1475	mV
		V_{EE} = −4.8V			−1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (−4.2V, −4.5V, −4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
				V_{EE} = –4.5V	–1025	–955	–880	mV
				V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
				V_{EE} = –4.5V	–1035			mV
				V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage		Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
				V_{EE} = –4.5V			–1610	mV
				V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage		Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
				V_{EE} = –4.5V	–1810	–1705	–1620	mV
				V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					230	µA
I_{IL}	Low level input current	One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current	All inputs at V_{IHMAX}			77	125	200	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.10 1.10	4.10 4.10	1.10 1.10	4.10 4.10	1.10 1.10	4.60 4.60	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to GS_n		1.10 1.10	4.10 4.10	1.10 1.10	4.10 4.10	1.10 1.10	4.60 4.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n, $\overline{Q}_n$	Waveform 2	1.00 1.00	3.30 3.30	1.00 1.00	3.30 3.30	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to GS_n		1.00 1.00	3.30 3.30	1.00 1.00	3.30 3.30	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.90 0.90	3.60 3.60	1.00 1.00	3.60 3.60	1.00 1.00	3.80 3.80	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n, $\overline{Q}_n$, GS_n	Waveforms 1,2	1.40 1.40	4.70 4.70	1.40 1.40	4.60 4.60	1.40 1.40	5.00 5.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to $\overline{E}$	Waveform 3	1.10		1.00		1.10		ns
t_h	Hold time $\overline{E}$ to D_n		1.30		1.30		1.30		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.10 1.10	4.10 4.10	1.10 1.10	4.10 4.10	1.10 1.10	4.60 4.60	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to GS_n		1.10 1.10	4.10 4.10	1.10 1.10	4.10 4.10	1.10 1.10	4.60 4.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n, $\overline{Q}_n$	Waveform 2	1.00 1.00	3.30 3.30	1.00 1.00	3.30 3.30	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to GS_n		1.00 1.00	3.30 3.30	1.00 1.00	3.30 3.30	1.00 1.00	3.40 3.40	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.90 0.90	3.60 3.60	1.00 1.00	3.60 3.60	1.00 1.00	3.80 3.80	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n, $\overline{Q}_n$, GS_n	Waveforms 1,2	1.40 1.40	4.70 4.70	1.40 1.40	4.60 4.60	1.40 1.40	5.00 5.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to $\overline{E}$	Waveform 3	1.10		1.00		1.10		ns
t_h	Hold time $\overline{E}$ to D_n		1.30		1.30		1.30		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.10 1.10	3.90 3.90	1.10 1.10	3.90 3.90	1.10 1.10	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to GS_n		1.10 1.10	3.90 3.90	1.10 1.10	3.90 3.90	1.10 1.10	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n, $\overline{Q}_n$	Waveform 2	1.00 1.00	3.10 3.10	1.00 1.00	3.10 3.10	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to GS_n		1.00 1.00	3.10 3.10	1.00 1.00	3.10 3.10	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.90 0.90	3.40 3.40	1.00 1.00	3.40 3.40	1.00 1.00	3.60 3.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n, $\overline{Q}_n$, GS_n	Waveforms 1,2	1.40 1.40	4.50 4.50	1.40 1.40	4.40 4.40	1.40 1.40	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to $\overline{E}$	Waveform 3	0.90		0.80		0.90		ns
t_h	Hold time $\overline{E}$ to D_n		1.10		1.10		1.10		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

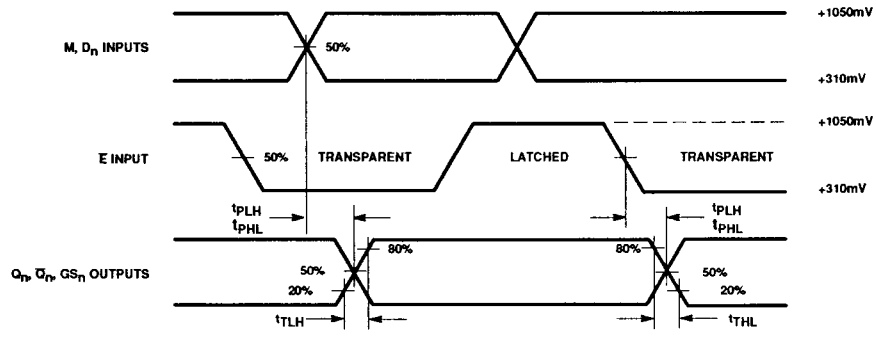
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 5%

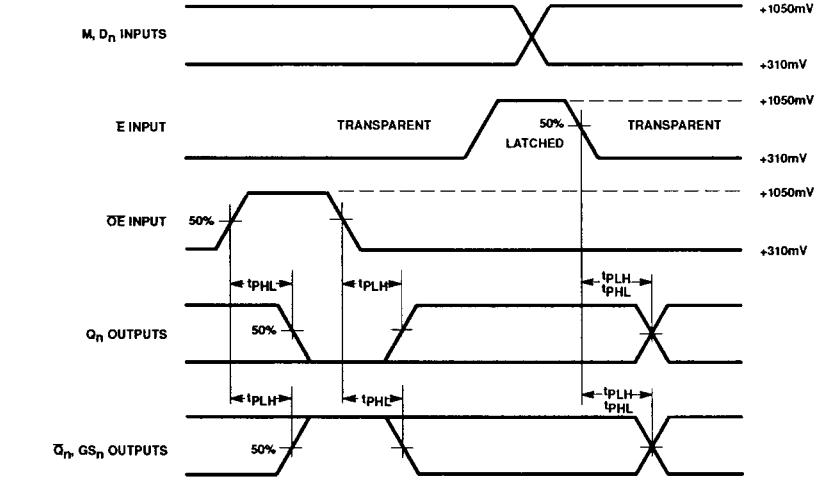
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX	MIN.	MAX	MIN.	MAX	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.10 1.10	3.90 3.90	1.10 1.10	3.90 3.90	1.10 1.10	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to GS_n		1.10 1.10	3.90 3.90	1.10 1.10	3.90 3.90	1.10 1.10	4.40 4.40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n, $\overline{Q}_n$	Waveform 2	1.00 1.00	3.10 3.10	1.00 1.00	3.10 3.10	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to GS_n		1.00 1.00	3.10 3.10	1.00 1.00	3.10 3.10	1.00 1.00	3.20 3.20	ns ns
t_{PLH} t_{PHL}	Propagation delay M to Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.90 0.90	3.40 3.40	1.00 1.00	3.40 3.40	1.00 1.00	3.60 3.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n, $\overline{Q}_n$, GS_n	Waveforms 1,2	1.40 1.40	4.50 4.50	1.40 1.40	4.40 4.40	1.40 1.40	4.80 4.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n, $\overline{Q}_n$, GS_n	Waveform 1	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	0.45 0.45	1.40 1.40	ns ns
t_s	Setup time D_n to $\overline{E}$	Waveform 3	0.90		0.80		0.90		ns
t_h	Hold time $\overline{E}$ to D_n		1.10		1.10		1.10		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

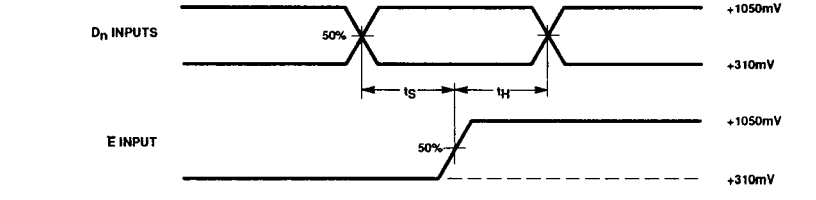
AC WAVEFORMS



Waveform 1. Propagation Delays and Transition Times



Waveform 2. Output Enable Timing



Waveform 3. Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.