Freescale Semiconductor
Advance Information

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RoHS

Power Management and User Interface IC

The 13892 is a Power Management and User Interface components for Freescale's i.MX51, i.MX37, i.MX35 and i.MX27 application processors, targeting personal media players and personal navigation devices.

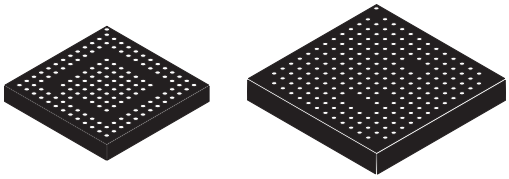
Features

- Battery charger system for wall charging and USB charging
- 10 bit ADC for monitoring battery and other inputs, plus a coulomb counter support module
- 4 adjustable output buck converters for direct supply of the processor core and memory
- 12 adjustable output LDOs with internal and external pass devices
- 2 boost converters for supplying LCD backlight and RGB LEDs
- Serial backlight drivers for displays and keypad, plus RGB LED drivers
- Power control logic with processor interface and event detection
- Real time clock and crystal oscillator circuitry, with coin cell backup and support for external secure real time clock on a companion system processor IC
- Touch screen interface
- SPI/I^{2}C bus interface for control and register access.
- Two package offering in 7 x 7mm and 12 x 12mm.

13892

Sample Parts Not Yet Available

POWER MANAGEMENT IC



VK SUFFIX
98ASA10820D
139-PIN 7X7 BGA

VL SUFFIX
98ASA10849D
186-PIN 12X12 BGA

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PC13892VK/R2*	-30°C to 85°C	7x7
PC13892VL/R2*		12x12
PC13892JVK/R2		7x7
PC13892JVL/R2		12x12
* ITC effected products		

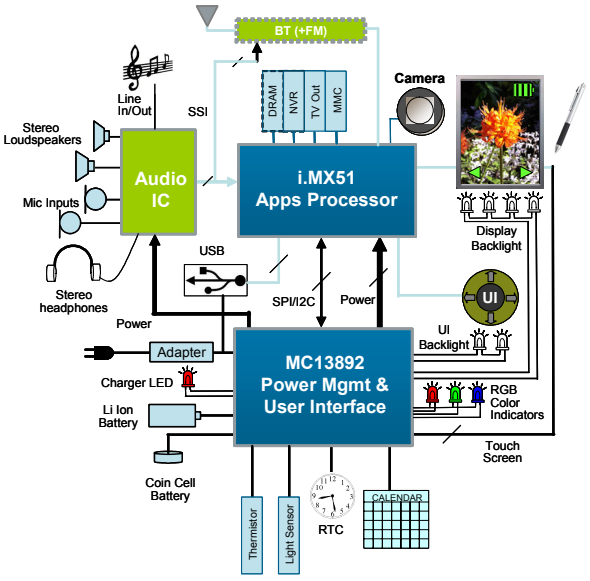


Figure 1. 13892 Typical Operating Circuit

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DEVICE VARIATIONS

Table 1. Device Variations

Parameter	Condition	Value for 13982VK	Value for 13982VL	Unit
Package size		7x7	12x12	mm
Pitch		0.5	0.8	mm
Pinout		See Pin Connections		
Junction to Ambient Natural Convection	Single layer board (1s)	104	65	°C/W
Junction to Ambient Natural Convection	Single layer board (1s)	54	42	°C/W
Junction to Ambient (@ 200 ft/min)	Single layer board (1s)	88	55	°C/W
Junction to Ambient (@ 200 ft/min)	Single layer board (1s)	49	38	°C/W
Junction to Board		32	28	°C/W
Junction to Case		29	22	°C/W
Junction to Package Top	Natural Convection	7.0	5.0	°C/W

INTERNAL BLOCK DIAGRAM

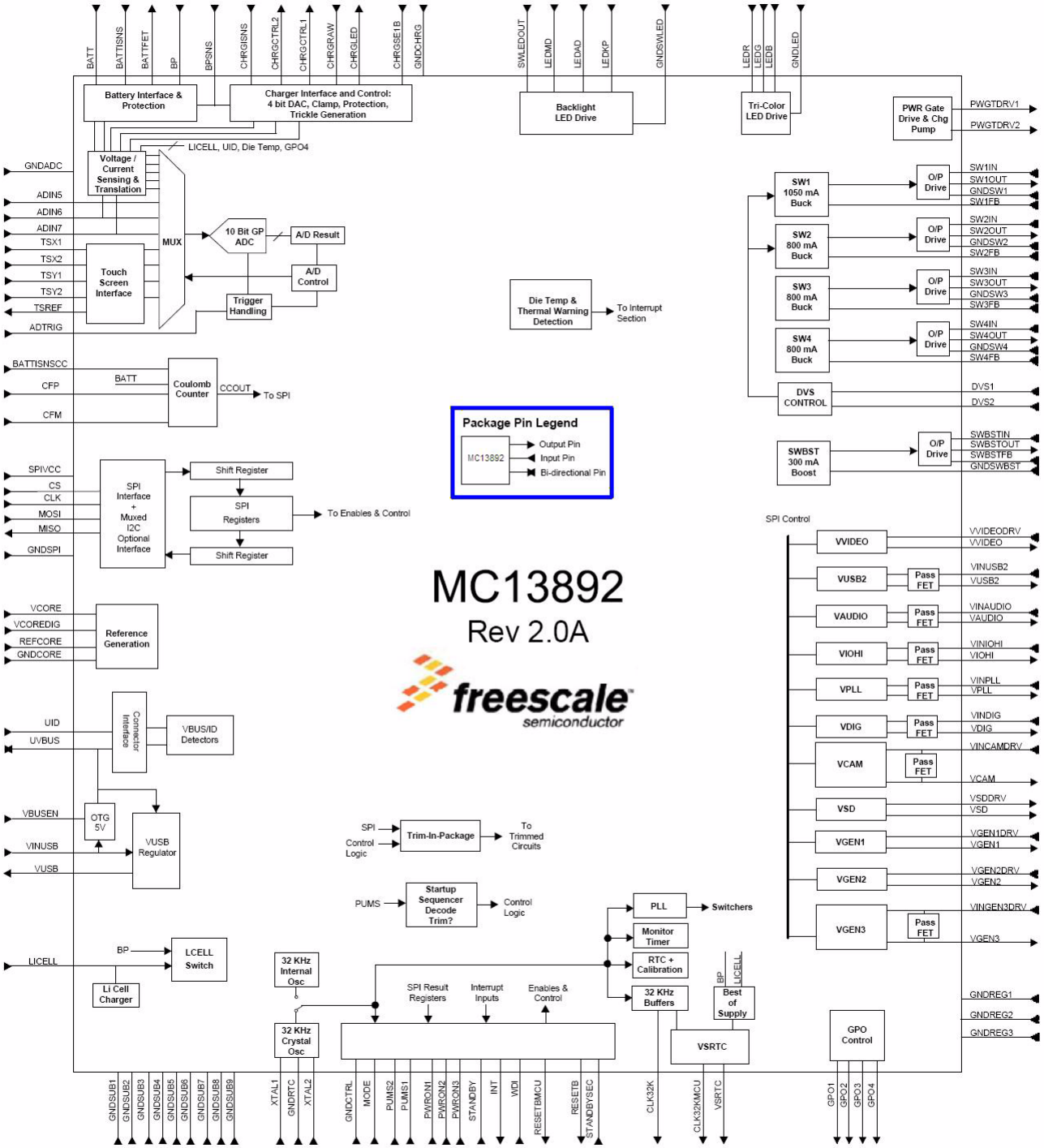


Figure 2. 13892 Simplified Internal Block Diagram

PIN CONNECTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VUSB2	VUSB2	VINUSB2	SWBSTIN	GNDSWBST	GNDSWLED	SWLEDOUT	MODE	VCORE	BATT	CHRGRAW	CHRGCTRL2	CHRGCTRL2
B	VUSB2	GPO1	DVS2	SWBSTOUT	LEDB	LEDKP	LEDR	GNDCORE	VCOREDIG	BP	CHRGCTRL1	BATTISNSCC	CHRGCTRL2
C	VINPLL	VSDDRV										CHRGISNS	BATTISNS
D	VUSB	VSD		SWBSTFB	LEDMD	DVS1	REFCORE	CHRGSE1B	LICELL	BATTFET		BPSNS	PWRON1
E	UVBUS	VPLL		LEDG	GNDLED	UID	PUMS2	GNDCHRG	CHRGLED	PWRON2	ADTRIG	INT	GNDSW1
F	GNDSW3	VBUSEN		SW3FB	LEDAD	GNDSUB	GNDSUB	GNDSUB	GPO3	GPO2	RESETBMCU	RESETB	SW1OUT
G	SW3OUT	VINUSB		SW4FB	GNDREG2	GNDSUB	GNDSUB	GNDSUB	PUMS1	WDI		GPO4	SW1IN
H	SW3IN	MISO		GNDSPI	GNDREG3	GNDSUB	GNDSUB	GNDSUB	GNDCTRL	SW1FB		STANDBYSEC	SW2IN
J	SW4IN	MOSI		CLK32KMCU	STANDBY	GNDADC	GNDREG1	PWRON3	TSX1	SW2FB		TSX2	SW2OUT
K	SW4OUT	SPIVCC		PWGTDRV1	CLK32K	VCAM	CFP	CFM	ADIN5	ADIN6		VVIDEODRV	GNDSW2
L	GNDSW4	CS										TSY2	VVIDEO
M	VGEN3	CLK	VGEN2	VSRTC	GNDRTC	VINCAMDRV	PWGTDRV2	VDIG	VINDIG	VGEN1DRV	ADIN7	TSY1	TSREF
N	VGEN3	VGEN3	VINGEN3DRV	VGEN2DRV	XTAL2	XTAL1	VINAUDIO	VAUDIO	VIOHI	VINIOHI	VGEN1	TSREF	TSREF

Regulators
Switchers
Backlights
Control Logic
Charger
RTC
Grounds
USB
ADC
SPI/I2C

Figure 3. 13892VK Pin Connections

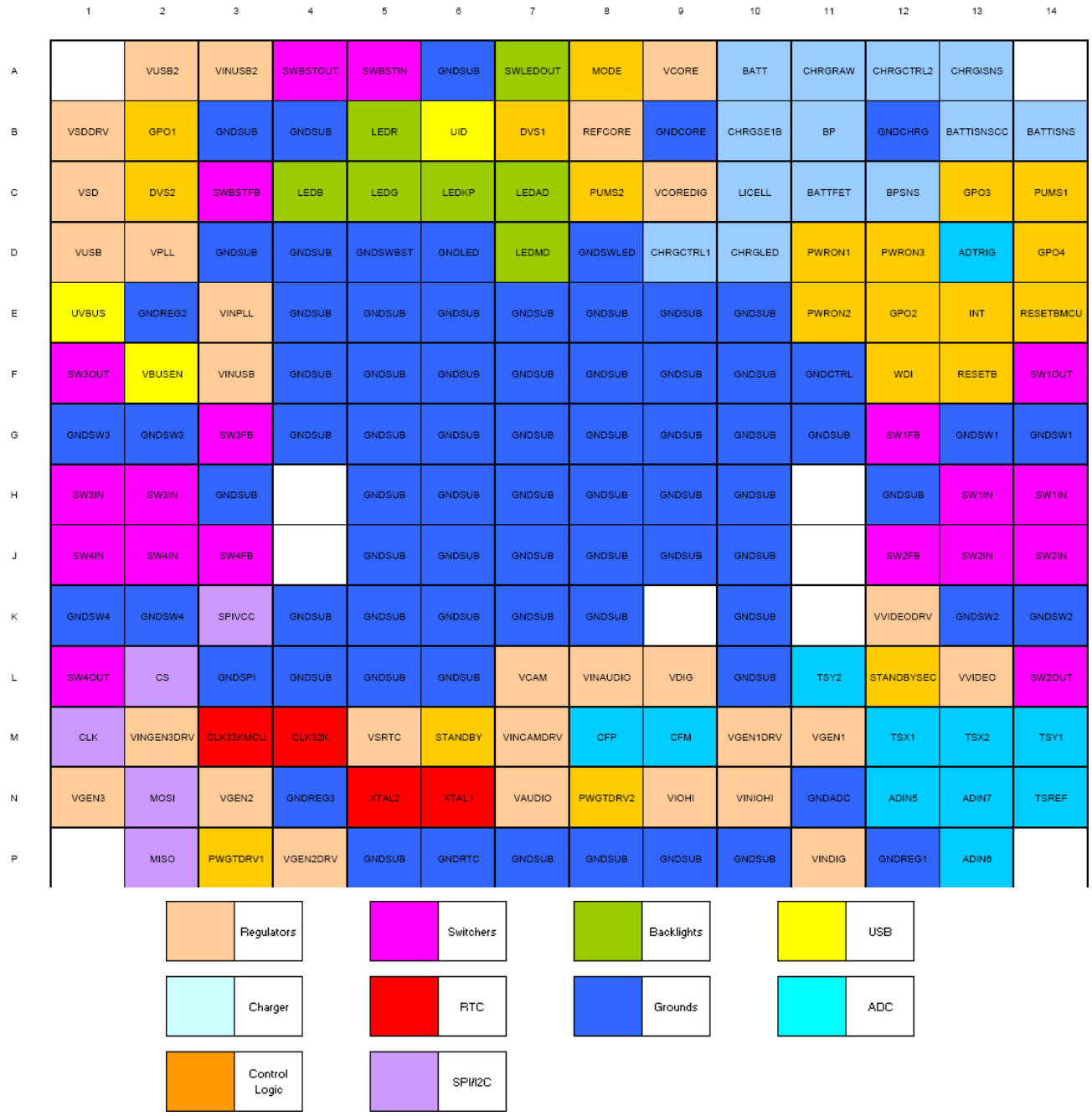


Figure 4. 13892VL Pin Connections

Table 2. 13892 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 39.

Pin Number on the 13982VK	Pin Number on the 13982VL	Pin Name	Pin Function	Formal Name	Definition
A1, A2, B1	A2	VUSB2	Output	USB 2 Supply	Output regulator for USB PHY
A3	A3	VINUSB2	Power	USB 2 Supply Input	Input regulator VUSB2
A4	A5	SWBSTIN	Power	Switcher Boost Power Input	Switcher BST input

Table 2. 13892 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 39.

Pin Number on the 13982VK	Pin Number on the 13982VL	Pin Name	Pin Function	Formal Name	Definition
A5	D5	GNDSWBST	Ground	Switcher Boost Ground	Ground for switcher BST
A6	D8	GNDSWLED	Ground	Switcher LED Ground	Ground for boost converter for serial LED drive
A7	A7	SWLEDOUT	Output	Switcher LED Output	Boost converter output for serial LED drive
A8	A8	MODE	Input	Mode Configuration	USB LBP mode, normal mode, test mode selection & anti-fuse bias
A9	A9	VCORE	Output	Core Supply	Regulated supply output for the IC analog core circuitry
A10	A10	BATT	Input	Battery Connection	1. Battery positive terminal 2. Battery current sensing point 2 3. Battery supply voltage sense
A11	A11	CHRGRAW	I/O	Charger Input	1. Charger input 2. Output to battery supplied accesories
A12, A13, B13	A12	CHRGCTRL2	Output	Charger Control 2	Driver output for charger path FETs M2
B2	B2	GPO1	Output	General Purpose Output 1	General purpose output 1
B3	C2	DVS2	Input	Dynamic Voltage Scaling Control 2	Switcher 2 DVS input pin
B4	A4	SWBSTOUT	Power	Switcher Boost Output	Switcher BST BP supply
B5	C4	LEDB	Output	LED Driver	General purpose LED driver output Blue
B6	C6	LEDKP	Output	LED Driver	Keypad lighting LED driver output
B7	B5	LEDR	Output	LED Driver	General purpose LED driver output Red
B8	B9	GNDCORE	Ground	Core Ground	Ground for the IC core circuitry
B9	C9	VCOREDIG	Output	Digital Core Supply	Regulated supply output for the IC digital core circuitry
B10	B11	BP	Power	Battery Plus	1. Application supply point 2. Input supply to the IC core circuitry 3. Application supply voltage sense
B11	D9	CHRGCTRL1	Output	Charger Control 1	Driver output for charger path FETs M1
B12	B13	BATTISNSCC	Input	Battery Current Sense	Accumulated current counter current sensing point
C1	E3	VINPLL	Power	PLL Supply Input	Input regulator processor PLL
C2	B1	VSDDRV	Output	VSD Driver	Drive output regulated SD card
C12	A13	CHRGISNS	Input	Charger Current Sense	Charge current sensing point 1
C13	B14	BATTISNS	Input	Battery Current Sense	Battery current sensing point 1
D1	D1	VUSB	Output	USB Supply	USB transceiver regulator output
D2	C1	VSD	Output	SD Card Supply	Output regulator SD card
D4	C3	SWBSTFB	Input	Switcher Boost Feedback	Switcher BST feedback
D5	D7	LEDMD	Output	LED Driver	Main display backlight LED driver output

Table 2. 13892 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 39.

Pin Number on the 13982VK	Pin Number on the 13982VL	Pin Name	Pin Function	Formal Name	Definition
D6	B7	DVS1	Input	Dynamic Voltage Scaling Control 1	Switcher 1DVS input pin
D7	B8	REFCORE	Output	Core Reference	Main bandgap reference
D8	B10	CHRGSE1B	Input	Charger Select	Charger forced SE1 detection input
D9	C10	LICELL	I/O	Coin Cell Connection	1. Coin cell supply input 2. Coin cell charger output
D10	C11	BATTFET	Output	Battery FET Connection	Driver output for battery path FET M3
D12	C12	BPSNS	Input	Battery Plus Sense	1. BP sense point 2. Charge current sensing point 2
D13	D11	PWRON1	Input	Power On 1	Power on/off button connection 1
E1	E1	UVBUS	I/O	USB Bus	1. USB transceiver cable interface 2. VBUS & OTG supply output
E2	D2	VPLL	Output	Voltage Supply for PLL	Output regulator processor PLL
E4	C5	LEDG	Output	PWM Driver for Green LED	General purpose LED driver output Green
E5	D6	GNDLED	Ground	LED Ground	Ground for LED drivers
E6	B6	UID	Input	USB ID	USB OTG transceiver cable ID
E7	C8	PUMS2	Input	Power Up Mode Select 2	Power up mode supply setting 2
E8	B12	GNDCHRG	Ground	Charger Ground	Ground for charger interface
E9	D10	CHRGLED	Output	Charger LED	Trickle LED driver output 1
E10	E11	PWRON2	Input	Power On 2	Power on/off button connection 2
E11	D13	ADTRIG	Input	ADC Trigger	ADC trigger input
E12	E13	INT	Output	Interrupt Signal	Interrupt to processor
E13	G13, G14	GNDSW1	Ground	Switcher 1 Ground	Ground for switcher 1
F1	G1, G2	GNDSW3	Ground	Switcher 3 Ground	Ground for switcher 3
F2	F2	VBUSEN	Input	VBUS Enable	External VBUS enable pin for OTG supply
F4	G3	SW3FB	Input	Switcher 3 Feedback	Switcher 3 feedback
F5	C7	LEDAD	Output	Auxiliary Display LED	Auxiliary display backlight LED driver output
F6	A6, B3, B4, D3, D4, E4, E5, E6	GNDSUB1	Ground	Ground 1	Non critical signal ground and thermal heat sink
F7	E7, E8, E9, E10, F4, F5, F6	GNDSUB2	Ground	Ground 2	Non critical signal ground and thermal heat sink
F8	F7, F8, F9, F10, G4, G5, G6, G7, G8	GNDSUB3	Ground	Ground 3	Non critical signal ground and thermal heat sink
F9	C13	GPO3	Output	General Purpose Output 3	General purpose output 3

Table 2. 13892 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 39.

Pin Number on the 13982VK	Pin Number on the 13982VL	Pin Name	Pin Function	Formal Name	Definition
F10	E12	GPO2	Output	General Purpose Output 2	General purpose output 2
F11	E14	$\overline{\text{RESETBMCU}}$	Output	MCU Reset	Reset output for processor
F12	F13	$\overline{\text{RESETB}}$	Output	Peripheral Reset	Reset output for peripherals
F13	F14	SW1OUT	Output	Switcher 1 Output	Switcher 1 output
G1	F1	SW3OUT	Output	Switcher 3 Output	Switcher 3 output
G2	F3	VINUSB	Input	VUSB Supply Input	Input option for UVUSB; tie to SWBST at top level
G4	J3	SW4FB	Input	Switcher 4 Feedback	Switcher 4 feedback
G5	E2	GNDREG2	Ground	Regulator 2 Ground	Ground for regulators 2
G6	G9, G10, G11, H3, H5, H6, H7, H8	GNDSUB4	Ground	Ground 4	Non critical signal ground and thermal heat sink
G7	H9, H10, H12, J5, J6, J7	GNDSUB5	Ground	Ground 5	Non critical signal ground and thermal heat sink
G8	J8, J9, J10, K4, K5, K6, K7	GNDSUB6	Ground	Ground 6	Non critical signal ground and thermal heat sink
G9	C14	PUMS1	Input	Power Up Mode Select 1	Power up mode supply setting 1
G10	F12	WDI	Input	Watchdog Input	Watchdog input
G12	D14	GPO4	Output	General Purpose Output 4	General purpose output 4
G13	H13, H14	SW1IN	Input	Switcher 1 Input	Input voltage for switcher 1
H1	H1, H2	SW3IN	Power	Switcher 3 Input	Switcher 3 input
H2	P2	MISO	I/O	Master In Slave Out	Primary SPI read output
H4	L3	GNDSPI	Ground	SPI Ground	Ground for SPI interface
H5	N4	GNDREG3	Ground	Regulator 3 Ground	Ground for regulators 3
H6	K8, K10, L4, L5, L6, L10	GNDSUB7	Ground	Ground 7	Non critical signal ground and thermal heat sink
H7	P5, P7, P8, P9, P10	GNDSUB8	Ground	Ground 8	Non critical signal ground and thermal heat sink
H8		GNDSUB9	Ground	Ground 9	Non critical signal ground and thermal heat sink
H9	F11	GNDCTRL	Ground	Logic Control Ground	Ground for control logic
H10	G12	SW1FB	Input	Switcher 1 Feedback	Switcher 1 feedback
H12	L12	STANDBYSEC	Input	Secondary Standby Signal	Standby input signal from peripherals
H13	J13, J14	SW2IN	Input	Switcher 2 Input	Input voltage for Switcher 2
J1	J1, J2	SW4IN	Power	Switcher 4 Input	Switcher 4 input
J2	N2	MOSI	Input	Master Out Slave In	Primary SPI write input

Table 2. 13892 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 39.

Pin Number on the 13982VK	Pin Number on the 13982VL	Pin Name	Pin Function	Formal Name	Definition
J4	M3	CLK32KMCU	Output	32 kHz Clock for MCU	32 kHz clock output for processor
J5	M6	STANDBY	Input	Standby Signal	Standby input signal from processor
J6	N11	GNDADC	Ground	ADC Ground	Ground for A to D circuitry
J7	P12	GNDREG1	Ground	Regulator 1 Ground	Ground for regulators 1
J8	D12	PWRON3	Input	Power On 3	Power on/off button connection 3
J9	M12	TSX1	Input	Touch Screen Interface X1	Touch screen interface X1
J10	J12	SW2FB	Input	Switcher 2 Feedback	Switcher 2 feedback
J12	M13	TSX2	Input	Touch Screen Interface X2	Touch screen interface X2
J13	L14	SW2OUT	Output	Switcher 2 Output	Switcher 2 output
K1	L1	SW4OUT	Output	Switcher 4 Output	Switcher 4 output
K2	K3	SPIVCC	Input	Supply Voltage for SPI	Supply for SPI bus and audio bus
K4	P3	PWGTDRV1	Output	Power Gate Driver 1	Power gate driver 1
K5	M4	CLK32K	Output	32 kHz Clock	32 kHz clock output for peripherals
K6	L7	VCAM	Output	Camera Supply	Output regulator camera
K7	M8	CFP	Passive	Current Filter Positive	Accumulated current filter cap plus terminal
K8	M9	CFM	Passive	Current Filter Negative	Accumulated current filter cap minus terminal
K9	N12	ADIN5	Input	ADC Channel 5 Input	ADC generic input channel 5
K10	P13	ADIN6	Input	ADC Channel 6 Input	ADC generic input channel 6
K12	K12	VVIDEODRV	Output	VVIDEO Driver	Drive output regulator VVIDEO
K13	K13, K14	GNDSW2	Ground	Switcher 2 Ground	Ground for switcher 2
L1	K1, K2	GNDSW4	Ground	Switcher 4 Ground	Ground for switcher 4
L2	L2	CS	Input	Chip Select	Primary SPI select input
L12	L11	TSY2	Input	Touch Screen Interface Y2	Touch screen interface Y2
L13	L13	VVIDEO	Output	Video Supply	Output regulator TV DAC
M1, N1, N2	N1	VGEN3	Output	General Purpose Regulator 3	Output GEN3 regulator
M2	M1	CLK	Input	Clock	Primary SPI clock input
M3	N3	VGEN2	Output	General Purpose Regulator 2	Output GEN2 regulator
M4	M5	VSRTC	Output	SRTC Supply	Output regulator for SRTC module on processor
M5	P6	GNDRTC	Ground	Real Time Clock Ground	Ground for the RTC block
M6	M7	VINCAMDRV	I/O	Camera Regulator Supply Input and Driver Output	1. Input regulator camera using internal PMOS FET. 2. Drive output regulator for camera voltage using external PNP device.

Table 2. 13892 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 39.

Pin Number on the 13982VK	Pin Number on the 13982VL	Pin Name	Pin Function	Formal Name	Definition
M7	N8	PWGTDRV2	Output	Power Gate Driver 2	Power gate driver 2
M8	L9	VDIG	Output	Digital Supply	Output regulator digital
M9	P11	VINDIG	Input	VDIG Supply Input	Input regulator digital
M10	M10	VGEN1DRV		5.5	Drive output gen1 regulator
M11	N13	ADIN7	Input	ADC Channel 7 Input	ADC generic input channel 7, group 1
M12	M14	TSY1	Input	Touch Screen Interface Y1	Touch screen interface Y1
M13, N12, N13	N14	TSREF	Output	Touch Screen Reference	Touch screen reference
N3	M2	VINGEN3DRV	Power/ Output	VGEN3 Supply Input and Driver Output	1. Input VGEN3 regulator 2. Drive VGEN3 output regulator
N4	P4	VGEN2DRV	Output	VGEN2 Driver	Drive output GEN2 regulator
N5	N5	XTAL2	Input	Crystal Connection 2	32.768 kHz oscillator crystal connection 2
N6	N6	XTAL1	Input	Crystal Connection 1	32.768 kHz oscillator crystal connection 1
N7	L8	VINAUDIO	Power	Audio Supply Input	Input regulator VAUDIO
N8	N7	VAUDIO	Output	Audio Supply	Output regulator for audio
N9	N9	VIOHI	Output	High Voltage IO Supply	Output regulator high voltage IO, efuse
N10	N10	VINIOHI	Input	High Voltage IO Supply Input	Input regulator high voltage IO
N11	M11	VGEN1	Output	General Purpose Regulator 1	Input GEN1 regulator

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Charger and USB Input Voltage(1)	V_{CHRGR}	-0.3 to 20	V
Serial LED Circuitry Voltages	V_{SWLED}	-0.3 to 28	V
MODE pin Voltage	V_{MODE}	-0.3 to 9.0	V
Battery Voltage	V_{BATT}	-0.3 to 4.8	V
Coin Cell Voltage	V_{LICELL}	-0.3 to 3.6	V
ESD Voltage(2) Human Body Model - HBM with Mode pin excluded	V_{ESD}	±1500	V
THERMAL RATINGS			
Ambient Operating Temperature Range	T_A	-30 to +85	°C
Operating Junction Temperature Range	T_J	-30 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
THERMAL RESISTANCE			
Peak Package Reflow Temperature During Reflow(3), (4)	T_{PPRT}	Note 4	°C

Notes

1. USB Input Voltage applies to UVBUS pin only
2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
3. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions -30°C ≤ T_A ≤ 85°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted. Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT CONSUMPTION					
RTC Mode					µA
All blocks disabled, no main battery attached, coin cell is attached to LICELL					
VSRTC	I_{SRTC}	-	0.80	1.00	
CLK32KMCU (20 pF load)	$I_{CLK32KMCU}$	-	1.00	1.10	
RTC	I_{RTC}	-	2.00	5.00	
RTC Calibration module (optional)	I_{RTCMOD}	-	1.00	2.00	
OFF Mode (All blocks disabled, main battery attached)	I_{OFF}				µA
13892 core and RTC module		-	10	20	
Power Cut Mode (All blocks disabled, no main battery attached, coin cell is attached and valid)	I_{PCUT}				µA
13892 core and RTC module		-	3.0	6.0	
ON Standby mode - Low power mode					µA
13892 core and RTC module	$I_{CORESTBY}$	-	10	20	
Trimmed references	$I_{TREFSTBY}$	-	20	30	
4 buck switches in low power mode	I_{SWSTBY}	-	60	120	
3 regulators[5]	$I_{REGSTBY}$	-	24	31.5	
Total	I_{STBY}	-	114	200	
ON Mode - Typical use case					µA
13892 core and RTC module	I_{COREON}	-	10	20	
Trimmed references	I_{TREFON}	-	20	30	
4 buck switches in PWMPS mode	I_{SWON}	-	345	610	
5 Regulators[6]	I_{REGON}	-	84	121.5	
Total	I_{ON}	-	459	1000	

Notes
5. VPLL, VIOHI, VGEN2
6. VPLL, VIOHI, VGEN2, VAUDIO, VVIDEO

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
32X CRYSTAL OSCILLATOR					
Operating Voltage Oscillator and RTC Block from BP	V_{XTAL}	1.2	-	4.65	V
Coincell Disconnect Threshold At LICELL	V_{LCD}	1.8	-	2.0	V
Operating Current XTAL Oscillator and RTC Module RTC Mode: All blocks disabled, no main battery attached, coin cell is attached to LICELL Calibration system	 $I_{XTALRTC}$ I_{XTALC}	 - -	 2.0 1.0	 5.0 2.0	µA
Output Low CLK32K, CLK32KMCU Output sink 100 µA	V_{CLKLO}	0	-	0.2	V
Output High CLK32K Output source 100 µA CLK32KMCU Output source 100 µA	 V_{CLKHI} $V_{CLKMCUHI}$	 $SPIV_{CC}$-0.2 V_{SRTC}-0.2	 - -	 $SPIV_{CC}$ V_{SRTC}	V
VSRTC GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} Valid Coin Cell range Or valid BP	 V_{LICELL} BP	 1.8 UVDET	 - -	 3.6 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{SRTC}	0	-	50	µA
Bypass Capacitor Value	C_{SRTC}	-	1.0	-	µF
VSRTC ACTIVE MODE – DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{SRTC}	1.15	1.20	1.25	V
Active Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	I_{RTCQS}	-	0.8	1.0	µA
CLK AND MISO					
Input Low CS, MOSI, CLK	V_{INCSLO} $V_{INMOSILO}$ $V_{INCLKLO}$	0	-	0.3*$SPIV_{CC}$	V
Input High CS, MOSI, CLK	V_{INCSHI} $V_{INMOSIHI}$ $V_{INCLKHI}$	0.7*$SPIV_{CC}$	-	$SPIV_{CC}$+0.3	V
Output Low MISO, INT Output sink 100 µA	$V_{OMISOLO}$ V_{OINTLO}	0	-	0.2	V
Output High MISO, INT Output source 100 µA	$V_{OMISOHI}$ V_{OINTHI}	$SPIV_{CC}$-0.2	-	$SPIV_{CC}$	V
SPIVCC Operating Range	$SPIV_{CC}$	1.75	-	3.1	V

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK CONVERTERS					
Operating Input Voltage	V_{SWIN}				V
PWM operation, 0 < IL < I_{MAX}		3.0	-	4.65	
PFM operation, 0 < IL < I_{MAX}		2.8	-	4.65	
Extended PWM or PFM operation[7]		UVDET	-	4.65	
Output Voltage Range	V_{SW1}				V
Switcher 1		0.6	-	1.375	
Switchers 2, 3, and 4		0.6	-	1.850	
Output Accuracy					mV
PWM mode including ripple, load regulation, and transients [8]	V_{SWLOPP}	Nom-50	Nom	Nom+50	
PFM Mode, including ripple, load regulation, and transients	$V_{SWLIPPI}$	Nom-50	Nom	Nom+50	
SW1-SW2 Output Delta Voltage	ΔV_{SW}				mV
SW1 and SW2 both programmed for 1.250 V, PWM mode, IL = 0.5*IL_{MAX}		-	-	25	
Maximum Continuous Load Current, I_{MAX}, V_{INMIN}<BP<4.65 V[11]			-		mA
SW1 in PWM mode	I_{SW1}			-	
with SWILIMB=0		900			
with SWILIMB=1[10]		1050			
SW2 in PWM mode	I_{SW2}	800	-	-	
SW3 in PWM mode	I_{SW3}	800	-	-	
SW4 in PWM mode	I_{SW4}	800	-	-	
SW1, SW2, SW3, SW4 in PFM mode	$I_{SW1, 2, 3, 4}$	-	50	-	
Current Limiter Peak Current Detection, V_{IN} = 3.6 V, Current through inductor[9]	I_{SWPK}				mA
SW1		920	-	1700	
SW2-4		850	-	1700	
Start-up Overshoot, IL = 0		-	-	25	mV
Effective Quiescent Current Consumption[11]	I_{SWQS}				µA
PWM Mode, IL=0 mA; device not switching		-	50	100	
PFM Mode, IL=0 mA; device not switching		-	15	30	
Automatic Mode Change Threshold, Switchover between PFM and PWM modes	AMC_{TH}	-	50	-	mA
Efficiency					%
PFM, 0.9 V, 1.0 mA		-	75	-	
PFM, 01.8 V, 1.0 mA		-	85	-	
PWM Pulse Skipping, 1.25 V, 50 mA		-	78	-	
PWM Pulse Skipping, 1.8 V, 50 mA		-	82	-	
PWM, 1.25 V, 500 mA		-	78	-	
PWM, 1.8 V, 500 mA		-	82	-	

Notes
7. In the extended operating range the performance may be degraded
8. Transient loading for load steps of ILmax/2
9. No current limiter interaction for SW1 up to 920 mA and for SW2-4 up to 850 mA .
10. In this mode, current limit protection is disabled. Therefore, the load on SW1 should not exceed 1.05 A
11. Guaranteed by design.

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK CONVERTERS (CONTINUED)					
External Components, Used as a condition for all other parameters					
Inductor for SW2, SW3, SW4[11]	L_{SW234}	-20%	2.2	+20%	µH
Inductor for SW1[11]	L_{SW1}	-20%	1.5	+20%	µH
Inductor Resistance	R_{WSW}	-	-	0.16	Ω
Bypass Capacitor for SW2, SW3, SW4[13]	C_{OSW234}	-35%	10	+35%	µF
Bypass Capacitor for SW1[14]	C_{OSW1}	-35%	2x22	+35%	µF
Bypass Capacitor ESR	ESR_{SW}	5.0	-	50	mΩ
Input Capacitor[15]		1.0	4.7	-	µF
SWBST					
Average Output Voltage[16] 3.0 V < V_{IN} < 4.65 (1), 0 < IL < IL_{MAX}[17]	V_{BST}	Nom-5%	5.0	Nom+5%	V
Output Ripple[11] 3.0 V < V_{IN} < 4.65, 0 < IL < IL_{MAX}, Excluding reverse recovery of Schottky diode	V_{BSTPP}	-	-	120	mVpp
Average Load Regulation V_{IN} = 3.6 V, 0 < IL < IL_{MAX}	V_{BSTLOR}	-	-	0.5	mV/mA
Average Line Regulation 3.0 V < V_{IN} < 4.65 V, IL = IL_{MAX}	V_{BSTLIR}	-	-	50	mV

Notes

12. Preferred device TDK VLS252012 series at 2.5x2.0 mm footprint and 1.2 mm max height
13. Preferably 0603 style 6.3 V rated X5R/X7R type at 35% total make tolerance, temperature spread and DC bias derating such as TDK C1608X5R0J106M
14. Preferably 0805 style 6.3 V rated X5R/X7R type at 35% total make tolerance, temperature spread and DC bias derating such as TDK C2012X5R0J226M
15. Preferably 0603 style 6.3 V rated X5R/X7R type at 35% total make tolerance, temperature spread and DC bias derating such as TDK C1608X5R0J475
16. Output voltage when configured to supply VBUS in OTG mode can be as high as 5.75 V
17. Vin is the low side of the inductor that is connected to BP.

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
SWBST (CONTINUED)					
Maximum Continuous Load Current IL_{MAX} 3.0 V < V_{IN} < 4.65, V_{OUT} = 5.0 V	I_{BST}	300	-	-	mA
Peak Current Limit(11) At SWBSTIN; V_{IN} = 3.6 V	BST_{PK}	700	-	1500	mA
Start-up Overshoot IL = 0 mA	V_{BSTOS}	-	-	500	mV
Efficiency, IL = IL_{MAX}	SWB_{STEFF}	65	80	-	%
Bias Current Consumption(11)	$I_{BSTBIAS}$	-	390	1200	µA
External Components - Used as a condition for all other parameters					
Inductor(18)	L_{BST}	-20%	2.2	+20%	µH
Inductor Resistance	R_W_{BST}	-	-	0.2	Ω
Inductor saturation current at 30% loss in inductance value	IL_{SAT}	1.0	-	-	A
Bypass Capacitor(19)	CO_{BST}	-60%	10	+35%	µF
Bypass Capacitor ESR at resonance	ESR_{BST}	1.0	-	10	mΩ
Input Capacitor	C_{BSTD}	1.0	4.7	-	µF
Diode current capability	I_{BSTDPK}	850	-	-	mAdc
Diode current capability	I_{BSTDPK}	1500	-	-	mApk
NMOS Off Leakage, SWBSTIN = 4.5 V, SWBSTEN = 0(11)	I_{BSTIK}	-	1.0	5.0	µA
SWLEDOUT					
Output Voltage Range at VSWLED(11)	VSW_{LED}	BP	-	25.5	V
Current Load capability(11) VSWLED = 25.5 V	I_{LED}	30	-	60	mA
LED Driver Headroom 8.0 V< VSWLED < 25.5 V	V_{LEDHR}	0.3	-	0.6	V
External Components					
Inductor	L_{LED}	-	3.3	-	µH
Capacitor(20)	CO_{LED}	-	4.7 (30 V) Or 2x10 (16 V) in series	-	µF
Input Capacitor		2.2	4.7	-	

Notes
18. Preferred device TDK VLS252012 series at 2.5x2.0 mm footprint and 1.2 mm max height
19. Applications of SWBST should take into account impact of tolerance and voltage derating on the bypass capacitor at the output level.
20. The typical value represents the nominal rated value of the capacitor and takes into account the strong derating as a function of DC voltage.

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
VVIDEO					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}	$V_{INVIDEO}$	V_{NOM}+0.25	-	4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} (Not exceeding PNP max power)	I_{VIDEO}	0	--	250/350	mA
Extended input voltage range (performance may be out of specification)		UVDET	-	4.65	V
Minimum Bypass Capacitor Value Used as a condition for all other parameters	CO_{VIDEO}	1.1	2.2	-	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{VIDEO}	20	-	100	mΩ
VVIDEO ACTIVE MODE DC					
Output Voltage V_{OUT} Vinmin < V_{IN} < V_{INMAX}, IL_{MIN} < IL < IL_{MAX}	ΔV_{VIDEO}	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, For any V_{INMIN} < V_{IN} < V_{INMAX}	$V_{VIDEOLOPP}$	-	-	0.20	mV/mA
Line Regulation V_{INMIN} < V_{IN} < V_{INMAX}, For any IL_{MIN} < IL < IL_{MAX}	$V_{VIDEOLIPP}$	-	5.0	8.0	mV
Short-circuit Protection Threshold V_{INMIN} < V_{IN} < V_{INMAX}, Short-circuit V_{OUT} to GND	$I_{VIDEOSHT}$	IL_{MAX}+20%	-	-	mA
Active Mode Quiescent Current V_{INMIN} < V_{IN} < V_{INMAX}, IL = 0	$I_{VIDEOQS}$	-	30	45	µA
VVIDEO LOW POWER MODE DC - VVIDEOMODE=1					
Output Voltage V_{OUT} V_{INMIN} < V_{IN} < V_{INMAX}, IL_{MINLP} < IL < IL_{MAXLP}	$\Delta V_{VIDEOLO}$	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Current Load Range ILminlp to IL_{MAXLP}	$I_{VIDEOLO}$	0.0	-	3.0	mA
Low Power Mode Quiescent Current V_{INMIN} < V_{IN} < V_{INMAX}, IL = 0	$I_{VIDEOQSLO}$	-	8.0	10.5	µA
VAUDIO					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}	V_{AUDIO}	V_{NOM}+0.25	-	4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{AUDIO}	0	-	150	mA
Extended input voltage range (performance may be out of specification)		UVDET	-	4.65	V
Minimum Bypass Capacitor Value	C_{OAUDIO}	0.65	2.2	-	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{AUDIO}	0	-	0.1	Ω

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
VAUDIO ACTIVE MODE DC					
Output Voltage V_{OUT} ($V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < ILmax$)	V_{AUDIO}	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation (1.0 mA < IL < IL_{MAX}, For any $V_{INMIN} < V_{IN} < V_{INMAX}$)	$V_{AUDIOLOR}$	-	-	0.25	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, For any $IL_{MIN} < IL < IL_{MAX}$	$V_{AUDIOLIR}$	-	5.0	8.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short circuit V_{OUT} to GND	$I_{AUDIOSHT}$	IL_{MAX}+20 %	-	-	mA
Active Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	$I_{AUDIOQS}$	-	8.0	10.5	µA
VPLL AND VDIG					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} VDIG, VPLL all settings, BP biased VPLL, VDIG [1:0] = 00,01 VPLL, VDIG [1:0] = 10, 11, External Switcher	V_{INPLL}, V_{INDIG}	 UVDET 1.75 2.15	 - SW4 = 1.8 2.2	 4.65 4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{PLL}, I_{DIG}	0	-	50	mA
Minimum Bypass Capacitor Value Used as a condition for all other parameters	C_{OPLL}, C_{ODIG}	0.65	2.2	-	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{PLL}, ESR_{DIG}	0	-	0.1	Ω
VPLL AND VDIG ACTIVE MODE DC (ONLY FOR 2.475, 2.7, AND 2.775 STEPS)					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{PLL}, V_{DIG}	V_{NOM} – 0.05	V_{NOM}	V_{NOM} + 0.05	V
Load Regulation 1.0 mA < IL < IL_{MAX} for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{PLLLOR}, V_{DIGLOR}	-	-	0.35	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$ for any $IL_{MIN} < IL < IL_{MAX}$	V_{PLLLIR}, V_{DIGLIR}	-	5.0	8.0	mV
Active Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	I_{PLLLQS}, I_{DIGLQS}	-	8.0	10.5	µA
VIOHI					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} V_{NOM} = 2.775 V	V_{INIOHI}	V_{NOM}+0.25	-	4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{IOHI}	0	-	100	mA
Extended Input Voltage Range (Performance may be out of specification)	$V_{INIOHIEXT}$	UVDET	-	4.65	V
Minimum Bypass Capacitor Value	C_{OIOHI}	0.65	2.2	-	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{IOHI}	0	-	100	mΩ

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
VIOHI ACTIVE MODE DC					
Output Voltage V_{OUT} - (V_{NOM} = 2.775) $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{IOH}	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{IOHLOR}	-	-	0.35	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	V_{IOHLIR}	-	5.0	8.0	mV
Active Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	I_{IOHQS}	-	8.0	10.5	µA
VCAM					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}	V_{INCAM}	V_{NOM} +0.25	-	4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{CAM}				mA
Internal pass FET		0	-	65	
External PNP		0	-	250	
Extended Input Voltage Range Performance may be out of specification	$V_{INCAMEXT}$	UVDET	-	4.65	
Minimum Bypass Capacitor Value	C_{OCAM}				µF
Internal pass device		0.65	2.2	-	
External PNP (not exceeding PNP max power)		1.1	2.2	-	
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{CAM}	20	-	100	mΩ
VCAM ACTIVE MODE DC					
Output Voltage V_{OUT} (V_{NOM} = 2.775) $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{CAM}	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{CAMLOR}	-	-	0.25	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	V_{CAMLIR}	-	5.0	8.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND	I_{CAMSHT}	IL_{MAX}+20 %	-	-	mA
Active Mode Quiescent Current	I_{CAMQS}				µA
$V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0, Internal PMOS configuration		-	25	35	
$V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0, External PNP configuration		-	30	45	

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
VCAM LOW POWER MODE DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MINLP} < IL < IL_{MAXLP}$	V_{CAMLO}	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{CAMLO}	0	-	3.0	mA
Low Power Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	$I_{CAMQSLO}$	-	8.0	10.5	µA
VSD					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} VSD[2:0]=010 to 111 VSD[2:0]=010 to 111, Extended Operation VSD[2:0]=000, 001 [000] BP Supplied VSD[2:0]=000 External Switcher Supplied	V_{INSD}	 V_{NOM}+0.25 UVDET UVDET 2.15	 - - - 2.20	 4.65 4.65 4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} Not exceeding PNP max power	I_{SD}	0	-	250	mA
Extended Input Voltage Range Performance may be out of specification for output levels VSD[2:0]=010 or greater	$V_{INSDEXT}$	UVDET	-	4.65	V
Minimum Bypass Capacitor Value	C_{OSD}	1.1	2.2	-	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{SD}	20	-	100	mΩ
VSD ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{SD}	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{SDLOR}	-	-	0.25	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	V_{SDLIR}	-	5.0	8.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND	I_{SDSHT}	IL_{MAX}+20%	-	-	mA
Active Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	I_{SDQS}	-	30	45	µA

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
VSD LOW POWER MODE DC - VSDMODE=1					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MINLP} < IL < IL_{MAXLP}$	V_{SDLO}	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{SDLO}	0	-	3.0	mA
Low Power Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	I_{SDQSLO}	-	8.0	10.5	µA
VUSB GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} Supplied by VBUS Supplied by SWBST	V_{INUSB}	 4.4 -	 5.0 -	 5.25 5.75	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{USB}	0	-	100	mA
Bypass Capacitor Value Range	C_{OUSB}	0.65	2.2	-	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{USB}	0	-	0.1	Ω
VUSB ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{USB}	V_{NOM} – 4%	3.3	V_{NOM} + 4%	V
Load Regulation $0 < IL < IL_{MAX}$ from DM/DP for any $V_{INMIN} < V_{IN} < V_{INMAX}$	V_{USBLOR}	-	-	1.0	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	V_{USBLIR}	-	-	20	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND	V_{USBSHT}	IL_{MAX}+20 %	-	-	mA
VUSB2					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} Extended operation	V_{INUSB2}	V_{NOM} +0.25 UVDET	- -	4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{USB2}	0	-	50	mA
Minimum Bypass Capacitor Value Used as a condition for all other parameters	C_{OUSB2}	0.65	2.2	-	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{USB2}	0	-	0.1	Ω

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
VUSB2 ACTIVE MODE DC					
Output Voltage V_{OUT} $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{USB2}	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	$V_{USB2LOR}$	-	-	0.35	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	$V_{USB2LIR}$	-	5.0	8.0	mV
Active Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	I_{USB2QS}	-	8.0	13	µA
UVBUS					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} (11) UREGIN supplied by SWBST	$V_{INUVBUS}$	4.75	5.0	5.25	V
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{UVBUS}	0	-	100	mA
Minimum Bypass Capacitor Value	C_{OUVBUS}	(21)	(21)	6.5 (22)	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	$V_{INUVBUS}$	(21)	(21)	(22)	Ω
UVBUS ACTIVE MODE DC					
Output Voltage Vout - (V_{NOM} = 2.775) $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$	V_{UVBUS}	4.4	5.0	5.25	V
VGEN1					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} All settings, BP biased VGEN1=00,01, External switcher supplied	V_{INGEN1}	UVDET < V_{NOM} +0.25 1.75	- SW4 = 1.8	4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} (not exceeding PNP max power)	I_{GEN1}	0	-	200	mA
Extended input voltage range (BP biased, performance may be out of specification for output levels VGEN1[1:0]=10 to 11)		UVDET	-	4.65	V
Minimum Bypass Capacitor Value	C_{OGEN1}	0.65	2.2	+35%	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{GEN1}	20	-	100	mΩ

Notes

21. Filtering is shared with CHRGRAW (shorted at board level). 2.2 µF is typically included at the CHRGRAW pin.
22. 6.5 µF is the maximum allowable capacitance on VBUS including all tolerances of filtering capacitance on VBUS and CHRGRAW (which are shorted at the board level).

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN1 ACTIVE MODE DC					
Output Voltage V_{OUT} VGEN1=00, 01, $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$ VGEN1=10, 11, $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$	V_{GEN1}	 V_{NOM} – 0.05 V_{NOM} – 3%	 V_{NOM} V_{NOM}	 V_{NOM} + 0.05 V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, for any $V_{INMIN} < V_{IN} < V_{INMAX}$	$V_{GEN1LOR}$	-	-	0.25	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, for any $IL_{MIN} < IL < IL_{MAX}$	$V_{GEN1LIR}$	-	5.0	8.0	mV
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND	$V_{GEN1SHT}$	IL_{MAX}+20 %	-	-	mA
Active Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	I_{GEN1QS}	-	20	45	µA
VGEN1 LOW POWER MODE DC - VGEN1MODE=1					
Output Voltage V_{OUT} - $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MINLP} < IL < IL_{MAXLP}$ VGEN1=00, 01 VGEN1=10, 11	V_{GEN1LO}	 V_{NOM} – 0.05 V_{NOM} – 3%	 V_{NOM} V_{NOM}	 V_{NOM} + 0.05 V_{NOM} + 3%	V
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{GEN1LO}	0	-	3.0	mA
Low Power Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	$I_{GEN1QSLO}$	-	8.0	10.5	µA
VGEN2 GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX} All settings, BP biased VGEN2=000,001, External switcher supplied	V_{INGEN2}	 UVDET< V_{NOM}+0.25 2.15	 - 2.2	 4.65 4.65	V
Operating Current Load Range IL_{MIN} to IL_{MAX} (Not exceeding PNP max power)	I_{GEN2}	0	-	350	mA
Extended input voltage range (BP biased, performance may be out of specification for output levels VGEN2[2:0]=100 to 111)		UVDET	-	4.65	V
Minimum Bypass Capacitor Value	C_{OGEN2}	1.1	2.2	+35%	µF
Bypass Capacitor ESR 10 kHz -1.0 MHz	ESR_{GEN2}	20	-	100	mΩ

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN2 ACTIVE MODE DC					
Output Voltage V_{OUT}	V_{GEN2}				V
VGEN2=000, 001, 010, $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$		V_{NOM} – 0.05	V_{NOM}	V_{NOM} + 0.05	
VGEN2=011, 100, 101, 110, 111, $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$		V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	
Load Regulation	$V_{GEN2LOR}$				mV/mA
1.0 mA < IL < IL_{MAX}, For any $V_{INMIN} < V_{IN} < V_{INMAX}$		-	-	0.20	
Line Regulation	$V_{GEN2LIR}$				mV
$V_{INMIN} < V_{IN} < V_{INMAX}$, For any $IL_{MIN} < IL < IL_{MAX}$		-	5.0	8.0	
Short-circuit Protection Threshold	$V_{GEN2SHT}$				mA
$V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to GND		IL_{MAX}+20 %	-	-	
Active Mode Quiescent Current	I_{GEN2QS}				uA
$V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0		-	35	45	
VGEN2 LOW POWER MODE DC - VGEN2MODE=1					
Output Voltage V_{OUT} - $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MINLP} < IL < IL_{MAXLP}$	V_{GEN2LO}				V
VGEN2=000 to 010		V_{NOM} – 0.05	V_{NOM}	V_{NOM} + 0.05	
VGEN2=011 to 111		V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{GEN2LO}	0	-	3.0	mA
Low Power Mode Quiescent Current	$I_{GEN2QSLO}$				µA
$V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0		-	8.0	10.5	
VGEN3 GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}	V_{INGEN3}				V
VGEN3CONFIG, VGEN3=01, 11		V_{NOM}+0.2	-	4.65	
VGEN3CONFIG, VGEN3=00, 10		UVDET	-	4.65	
Operating Current Load Range IL_{MIN} to IL_{MAX}	I_{GEN3}				mA
Internal Pass FET		0	-	50	
External PNP (Not exceeding PNP max power)		0	-	200	
Minimum Bypass Capacitor Value	C_{OGEN3}				µF
Internal pass device		0.65	2.2	-	
External pass device		1.1	2.2	-	
Bypass Capacitor ESR	ESR_{GEN3}				mΩ
10 kHz -1.0 MHz		20	-	100	

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN3 ACTIVE MODE DC					
Output Voltage V_{OUT} VGEN2=000, 001, 010, $V_{INMIN} < V_{IN} < V_{INMAX}$ $IL_{MIN} < IL < IL_{MAX}$	V_{GEN3}	V_{NOM} – 3%	V_{NOM}	V_{NOM} + 3%	V
Load Regulation 1.0 mA < IL < IL_{MAX}, For any $V_{INMIN} < V_{IN} < V_{INMAX}$	$V_{GEN3LOR}$	-	-	0.40	mV/mA
Line Regulation $V_{INMIN} < V_{IN} < V_{INMAX}$, For any $IL_{MIN} < IL < IL_{MAX}$	$V_{GEN3SHT}$	-	5.0	8.0	mV
VGEN3 ACTIVE MODE DC (CONTINUED)					
Short-circuit Protection Threshold $V_{INMIN} < V_{IN} < V_{INMAX}$, Short circuit V_{OUT} to GND	$V_{GEN3SHT}$	IL_{MAX}+20 %	-	-	mA
Active Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0, Internal PMOS configuration $V_{INMIN} < V_{IN} < V_{INMAX}$, IL=0, external PNP configuration	I_{GEN3QS}	- -	25 30	35 45	µA
VGEN3 LOW POWER MODE DC					
Output Voltage V_{OUT} - (Accuracy) $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MINLP} < IL < IL_{MAXLP}$	V_{GEN3LO}	V_{NOM}-3%	V_{NOM}	V_{NOM}+3%	V
Current Load Range IL_{MINLP} to IL_{MAXLP}	I_{GEN3LO}	0	1.0	3.0	mA
Low Power Mode Quiescent Current $V_{INMIN} < V_{IN} < V_{INMAX}$, IL = 0	$I_{GEN3QSLO}$	-	8.0	10.5	µA
CHARGE PATH REGULATOR					
Input Operating Voltage - CHRGRAW	V_{INCHRG}	$BATT_{MIN}$	-	20	V
Output Voltage Trimming Accuracy VCHRG[2:0]=011, Charge current 50 mA at T=25°C	BP_{TRIM}	-	-	0.35	%
Output Voltage Spread - VCHRG[2:0]=011, 1XX Charge current 1.0 mA to 100 mA Charge current 100 mA and above	BP_{SP}	 -1.0 -3.0	 - -	 1.0 1.0	%
Current Limit Tolerance (23) ICHRG[3:0]=0001 ICHRG[3:0]=0100 ICHRG[3:0]=0110 All other settings	ΔI_{LIM}	 68 360 500 -	 80 400 560 -	 92 440 620 15	 mA mA mA %
Start-up Overshoot - Unloaded	$BP_{OS-START}$	-	-	2.0	%

Notes

23. Excludes spread and tolerance due to board and 100 mOhm sense resistor tolerances.

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
CHARGE PATH REGULATOR (CONTINUED)					
Transient Overshoot Charge current 1.0 mA to 1.0 A, Rise time 5.0 us	BP_{OS}	-	-	2.0	%
Configuration					
Input Capacitance - CHRGRAW[24]	C_{INCHRG}	-	2.2	-	µF
Load Capacitor - BPSNS[24]	C_{BP}	10	-	47	µF
Cable length	L_C	-	-	3	m
THERMAL					
Thermal Warning Lower Threshold	T_{WL}	95	100	105	°C
Thermal Warning Higher Threshold	T_{WH}	115	120	125	°C
Thermal Warning Hysteresis[25]	TWH_Y	2.0	-	4.0	°C
Thermal Protection Threshold	TPT	130	140	150	°C
BACKLIGHT LED DRIVERS					
Absolute Accuracy - All current settings		-	-	15	%
Matching - At 400 mV, 21 mA		-	-	3	%
Leakage - LEDxDC[5:0]=000000		-	-	1	µA
SIGNALING LED DRIVERS					
Absolute Accuracy - All current settings		-	-	15	%
Matching - At 400 mV, 21 mA		-	-	3	%
Leakage - LEDxDC[5:0]=000000		-	-	1	µA
UVBUS - GENERAL					
Operating Input Voltage Range V_{INMIN} to V_{INMAX}[26] VINUSB supplied by SWBST		4.75	5	5.25	V
Operating Current Load Range IL_{MIN} to IL_{MAX}		0		100	mA
Minimum Bypass Capacitor Value		(27)	(27)	6.5 (28)	µF
Bypass Capacitor ESR - 10 kHz-1.0 MHz		(27)	(27)	(28)	W
ACTIVE MODE DC					
Output Voltage V_{OUT} - (V_{NOM} = 2.775), $V_{INMIN} < V_{IN} < V_{INMAX}$, $IL_{MIN} < IL < IL_{MAX}$		4.4	5.0	5.25	V
Short-circuit Protection Threshold ** - $V_{INMIN} < V_{IN} < V_{INMAX}$, Short-circuit V_{OUT} to ground		IL_{MAX}+20 %	-	-	mA

Notes
24. An additional derating of 35% is allowed.
25. Equivalent to approx. 30 mW min, 60 mW max
26. Guaranteed by design.
27. Filtering is shared with CHRGRAW (shorted at board level). 2.2 uF is typically included at the CHRGRAW pin.
28. 6.5 uF is the maximum allowable capacitance on VBUS including all tolerances of filtering capacitance on VBUS and CHRGRAW (which are shorted at the board level).

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
ADC					
Conversion Current			1		mA
Converter Core Input Range Single ended voltage readings Differential readings		 0 -1.2		 2.4 1.2	V
Maximum Input Voltage[29] Channels ADIN5, ADIN6 and ADIN7				BP	V
Integral Nonlinearity				3	LSB
Differential Nonlinearity				1	LSB
Zero Scale Error (Offset) Before auto calibration After auto calibration				 10 1	LSB
Full Scale Error (Gain) Before auto calibration After auto calibration				 25 5	LSB
Drift Over-temperature [30] - Including scaling				1	LSB
Source Impedance No bypass capacitor at input Bypass capacitor at input 10 nF				 5 30	KΩ
Input Buffer Offset - BUFFEN=1		-5		5	mV
Input Buffer Range - BUFFEN=1		0.02		2.4	V

Notes
29. ADIN5, 6 and 7 inputs must not exceed BP voltage.
30. Guaranteed by design.

Table 5. Static Electrical Characteristics (Continued)

Currents valid over entire operating temperature range, except at 25°C only. Current in RTC Mode is from LICELL = 2.5 V, in all other modes from BP = 3.6 V. External loads are not included.

Characteristic	Symbol	Min	Typ	Max	Unit
TOUCH SCREEN					
Plate Maximum Voltage X, Y[32]				VCORE	V
Plate Resistance X, Y		100		1000	Ω
Resistance Between Plates Setting Time - Contact Position measurement		180 3		1200 5.5	Ω µs
Capacitance Between Plates		0.5	2		nF
Contact Resistance Current Source			100		uA
Interrupt Current Source			20		uA
Interrupt Threshold for Pressure Application		40	50	60	KΩ
Interrupt Threshold for Pressure Removal		60	80	95	KΩ
Current Source Inaccuracy - Over-temperature				20	%
Touch Screen					
Quiescent Current - Active Mode			20		µA
Max Load Current - Active Mode				20	mA
Output Voltage - 0<IL<20 mA		-3%	1.20	+3%	V
Load Regulation - 0<IL<20 mA				0.8	mV/mA
PSRR [33] - IL=15 mA		40			dB
Bypass Capacitor ESR		0		0.1	Ω
Bypass Capacitance		0.65	2.2	+35%	µF
Discharge Resistor - Regulator disable			100		Ω

Notes

31. All characteristics in this table are applicable only for non touch screen operation
32. TS[xy][1,2] inputs must not exceed BP or VCORE
33. Guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.8 V, --30 ≤ T_A ≤ 85°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
32X CRYSTAL OSCILLATOR					
RTC oscillator start-up time Upon application of power	t_{RTCST}	 -	 -	 1.0	Sec
CLK32K Rise and Fall Time - CL=50 pF CLK32KDRV[1:0]=00 (default) CLK32KDRV[1:0]=01 CLK32KDRV[1:0]=10 CLK32KDRV[1:0]=11	$t_{CLK32KET}$	 - - - -	 22 11 High Z 44	 - - - -	ns
CLK32KMCU Rise and Fall Time CL=12 pF	$t_{CLK32KMCUET}$	 -	 22	 -	ns
CLK32K and CLK32KMCU Output Duty Cycle Crystal on XTAL1, XTAL2 pins	$t_{CLK32KDC}$, $t_{CLK32KMCUDC}$	 45	 -	 55	%
RMS Output Jitter[34] 1.0 Sigma for Gaussian distribution	t_{CLKJ}	 -	 -	 30	ns RMS
CLK AND MISO					
MISO Rise and Fall Time, CL=50 pF, SPIVCC=1.8 V SPIDRV [1:0]=00 (default) SPIDRV [1:0]=01 SPIDRV [1:0]=10 SPIDRV [1:0]=11	t_{MISOET}	 - - - -	 11 6.0 High Z 22	 - - - -	ns
BUCK CONVERTERS					
Turn-on Time, Enable to 90% of end value, IL=0	t_{ONPWM}	-	-	500	µs
SWBST					
Turn-on Time Enable to 90% of V_{OUT}, IL=0	t_{ONBST}	 -	 -	 2.0	ms
Transient Load Response, IL from 1.0 mA to 100 mA in 1.0 µs steps Maximum transient Amplitude Time to settle 80% of transient	A_{TMAX}	 - -	 - -	 300 500	 mV µs
Transient Load Response, IL from 100 mA to 1.0 mA Maximum transient Amplitude Time to settle 80% of transient	A_{TMAX}	 - -	 - -	 300 20	 mV µs

Notes

34. Output jitter exhibits a Gaussian distribution

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.8 V, --30 ≤ T_A ≤ 85°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SWLEDOUT					
Switching Frequency[35] PLLx[2:0] = 100	f_{SWLED}	- -	 2.097	 -	MHz
Start-up Time	t_{ST}	-	100	-	µs
VVIDEO ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV V_{IN} = V_{NOM} + 1.0 V	VVIDEOPSSR	 35 50	 40 60	 - -	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 75% of IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 10 kHz >10 kHz – 1.0 MHz	VVIDEOON	 - - -	 - - -	 -114 -124 -129	dBV/√Hz
Spurs 32.768 kHz and harmonics	VVIDEOSP	 -	 -	 -120	dB
Turn-on Time Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	VVIDEOt_{ON}	 -	 -	 1.0	ms
Turn-off Time Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	VVIDEOt_{OFF}	 0.1	 -	 10	ms
Start-up Overshoot V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$V_{VIDEOOS}$	 -	 1.0	 2.0	%
Transient Load Response V_{IN} = V_{INMIN}, V_{INMAX}	$V_{VIDEOTLOR}$	 -	 1.0	 2.0	%

Notes

35. The switcher runs at 2/3 of the buck switcher PLL frequency and follows the PLL[2:0] programming.

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.8 V, --30 ≤ T_A ≤ 85°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VVIDEO ACTIVE MODE - AC (CONTINUED)					
Transient Line Response IL = 75% of IL_{MAX}	$V_{VIDEOTLIR}$	- 	5.0	8.0	mV
Mode Transition Time From low power to active, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VVIDEOt_{MOD+}$	-	-	100	µs
Mode Transition Response[36] From low power to active and from active to low power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{VIDEOMTR}$	-	1.0	2.0	%
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV, > UVDET V_{IN} = V_{NOM} + 1.0 V, > UVDET	VAUDIOPSSR	 35 50	 40 60	 - -	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*ILmax 100 Hz – 1.0 kHz >1.0 kHz – 10 kHz >10 kHz – 1.0 MHz	VAUDIOON	 - - -	 - - -	 -114 -124 -129	dBV/√Hz
Spurs 32.768 kHz and harmonics	VAUDIOSP	 -	 -	 -120	dB
Turn-on Time Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VAUDIOt_{ON}$	-	-	1.0	ms
Turn-off Time Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VAUDIOt_{OFF}$	0.1	-	10	ms
Start-up Overshoot V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$V_{AUDIOOS}$	-	1.0	2.0	%
Transient Load Response - See Transient Response Waveforms on page 56, V_{IN} = V_{INMIN}, V_{INMAX}	$V_{AUDIOTLOR}$	-	1.0	2.0	%
Transient Line Response - See Transient Response Waveforms on page 56 IL = 75% of IL_{MAX}	$V_{AUDIOTLIR}$	-	5.0	8.0	mV
VPLL AND VDIG ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = UVDET V_{IN} = V_{NOM} + 1.0 V, > UVDET	VPLLPSSR	 35 50	 40 60	 - -	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX} 100 Hz – 1.0 kHz >1 kHz – 1.0 MHz	VPLLON	 - -	 20 -	 - 2.5	 dB/dec µV/√Hz
Spurs 32.768 kHz and harmonics	VPLLSP	 -	 -	 -85	dB

Notes

36. Guaranteed by design.

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.8 V, --30 ≤ T_A ≤ 85°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VPLL AND VDIG ACTIVE MODE - AC (CONTINUED)					
Turn-on Time Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VPLLt_{ON}$	-	-	100	µs
Turn-off Time Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VPLLt_{OFF}$	0.1	-	10	ms
Start-up Overshoot V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$V_{PLLOS,}$	-	1.0	2.0	%
	V_{DIGOS}	-	2.0	4.0	%
Transient Load Response - See Transient Response Waveforms on page 56 V_{IN} = V_{INMIN}, V_{INMAX}	$V_{PLLTLOR,}$ $V_{DIGTLOR}$	-	50	70	mV
Transient Line Response - See Transient Response Waveforms on page 56 IL = 75% of IL_{MAX}	$V_{PLLTLIR,}$ $V_{DIGTLIR}$	-	5.0	8.0	mV
VIOHI ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV, > UVDET V_{IN} = V_{NOM} + 1.0 V, > UVDET	VIOHIPSSR	35 50	40 60	- -	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 1.0 MHz	VIOHION	- -	20 -	- 1.0	dB/dec µV/√Hz
Spurs 32.768 kHz and harmonics	VIOHISP	-	-	-100	dB
Turn-on Time Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VIOHIt_{ON}$	-	-	1.0	ms
Turn-off Time Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VIOHIt_{OFF}$	0.1	-	10	ms
Start-up Overshoot V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	V_{IOHIOS}	-	1.0	2.0	%
Transient Load Response - See Transient Response Waveforms on page 56 V_{IN} = V_{INMIN}, V_{INMAX}	$V_{IOHITLOR}$	-	1.0	2.0	%
Transient Line Response - See Transient Response Waveforms on page 56 IL = 75% of IL_{MAX}	$V_{IOHITLIR}$	-	5.0	8.0	mV
Mode Transition Time - See Transient Response Waveforms on page 56 From low power to active, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VIOHI_{MTR}$	-	-	10	µs
Mode Transition Response From low power to active and from active to low power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{IOHIMTR}$	-	1.0	2.0	%

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.8 V, --30 ≤ T_A ≤ 85°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VCAM ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz	VCAMPSSR				dB
V_{IN} = V_{INMIN} + 100 mV		35	40	-	
V_{IN} = V_{NOM} + 1.0 V		50	60	-	
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX}	VCAMON				
100 Hz – 1.0 kHz		-	20	-	dB/dec
>1.0 kHz – 1.0 MHz		-	-	1.0	µV/√Hz
Spurs	VCAMSP				dB
32.768 kHz and harmonics		-	-	-100	
Turn-on Time (Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	$VCAMt_{ON}$	-	-	1.0	ms
Turn-off Time (Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	$VCAMt_{OFF}$	0.1	-	10	ms
Start-up Overshoot (V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	V_{CAMOS}	-	1.0	2.0	%
Transient Load Response - See Transient Response Waveforms on page 56	V_{CAMLOR}				
V_{IN} = V_{INMIN}, V_{INMAX}					
VCAM=01, 10, 11		-	1.0	2.0	%
VCAM=00		-	50	70	mV
Transient Line Response - See Transient Response Waveforms on page 56	V_{CAMLIR}				mV
IL = 75% of IL_{MAX}		-	5.0	8.0	
Mode Transition Time - See Transient Response Waveforms on page 56	$VCAMt_{MOD}$				µs
From low power to active, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}		-	-	100	
Mode Transition Response	V_{CAMMTR}				%
From low power to active and from, active to low power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}		-	1.0	2.0	
VSD ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz	VSDPSSR				dB
V_{IN} = V_{INMIN} + 100 mV		35	40	-	
V_{IN} = V_{NOM} + 1.0 V		50	60	-	
Output Noise - V_{IN} = V_{INMIN}, IL = 75% of IL_{MAX}	VSDON				dBV/√Hz
100 Hz – 1.0 kHz		-	-	-115	
>1.0 kHz – 10 kHz		-	-	-126	
>10 kHz – 1.0 MHz		-	-	-132	
Spurs (32.768 kHz and harmonics)	VSDSP	-	-	-100	dB
Turn-on Time (Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	$VSDt_{ON}$	-	-	1.0	ms
Turn-off Time (Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	$VSDt_{OFF}$	0.1	-	10	ms
Start-up Overshoot	V_{SDOS}				%
V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0		-	1.0	2.0	

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.8 V, --30 ≤ T_A ≤ 85°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VSD ACTIVE MODE - AC (CONTINUED)					
Transient Load Response - See Transient Response Waveforms on page 56 V_{IN} = V_{INMIN}, V_{INMAX} - VSD[2:0]=010 to 111 - VSD[2:0]=000 to 001	V_{SDTLOR}	 - -	 1.0 -	 2.0 70	 % mV
Transient Line Response - See Transient Response Waveforms on page 56 IL = 75% of IL_{MAX}	V_{SDTLIR}	 -	 5.0	 8.0	mV
Mode Transition Time - See Transient Response Waveforms on page 56 From low power to active, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VSDt_{MOD}$	 -	 -	 100	µs
Mode Transition Response - See Transient Response Waveforms on page 56 From low power to active and from active to low power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	V_{SDMTR}	 -	 1.0	 2.0	%
VUSB ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV	VUSBPSSR	 35	 40	 -	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 75% of IL_{MAX} 100 Hz – 50 kHz >50 kHz – 1.0 MHz	VUSBON	 - -	 - -	 1.0 0.2	µV/√Hz
VUSB2 ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = V_{INMIN} + 100 mV V_{IN} = V_{NOM} + 1.0 V	VUSB2PSSR	 35 50	 40 60	 - -	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 1.0 MHz	VUSB2ON	 - -	 20 -	 - 0.2	 dB/dec µV/√Hz
Spurs 32.768 kHz and harmonics	VUSB2SP	 -	 -	 -100	dB
Turn-on Time[37] Enable to 90% of end value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VUSB2t_{ON}$	 -	 -	 100	µs
Turn-off Time[37] Disable to 10% of initial value, V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VUSBt_{OFF}$	 0.1	 -	 10	ms
Start-up Overshoot V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	V_{USB2OS}	 -	 1.0	 2.0	%
Transient Load Response - See Transient Response Waveforms on page 56 V_{IN} = V_{INMIN}, V_{INMAX}	$V_{USB2TLOR}$	 -	 1.0	 2.0	%
Transient Line Response - See Transient Response Waveforms on page 56 IL = 75% of IL_{MAX}	$V_{USB2TLIR}$	 -	 5.0	 8.0	mV

Notes
37. Guaranteed by design.

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.8 V, --30 ≤ T_A ≤ 85°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
UVBUS ACTIVE MODE DC					
Turn-on Time[38] VBUS Rise Time per USB OTG with max loading of 6.5 µF+10 µF	$UVBUSt_{ON}$	-	-	100	ms
Turn-off Time[38] Disable to 0.8 V, per USB OTG specification parameter VA_SESS_VLD, V_{IN} = V_{INMIN}, V_{INMAX}, IL=0	$UVBUSt_{OFF}$	-	-	1.3	sec
VGEN1 ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz V_{IN} = UVDET V_{IN} = V_{NOM} + 1.0 V, > UVDET	VGEN1PSSR	 35 50	 40 60	 - -	dB
Output Noise - V_{IN} = V_{INMIN}, IL = 0.75*IL_{MAX} 100 Hz – 1.0 kHz >1.0 kHz – 10 kHz >10 kHz – 1.0 MHz	VGEN1ON	 - - -	 - - -	 -115 -126 -132	dBV/√Hz
Spurs 32.768 kHz and harmonics	VGEN1SP	-	-	-100	dB
Turn-on Time Enable to 90% of end value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VGEN1t_{ON}$	-	-	1.0	ms
Turn-off Time Disable to 10% of initial value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VGEN1t_{OFF}$	0.1	-	10	ms
Start-up Overshoot V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	V_{GEN1OS}	-	1.0	2.0	%
Transient Load Response - See Transient Response Waveforms on page 56 V_{IN} = V_{INMIN}, V_{INMAX} - VGEN1[1:0]=10 to 11 - VGEN[1:0]=00 to 01	$V_{GEN1TLOR}$	 - -	 1.0 -	 2.0 70	 % mV
Transient Line Response - See Transient Response Waveforms on page 56 IL = 75% of IL_{MAX}	$V_{GEN1TLIR}$	-	5.0	8.0	mV
Mode Transition Time - See Transient Response Waveforms on page 56 From low power to active V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VGEN1t_{MOD}$	-	-	100	µs
Mode Transition Response - See Transient Response Waveforms on page 56 From low power to active and from active to low power V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{GEN1MTR}$	-	1.0	2.0	%

Notes

38. Guaranteed by design.

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.8 V, --30 ≤ T_A ≤ 85°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN2 ACTIVE MODE - AC					
PSRR - IL = 75% of IL_{MAX}, 20 Hz to 20 kHz	VGEN2PSSR				dB
V_{IN} = V_{INMIN} + 100 mV		35	40	-	
V_{IN} = V_{NOM} + 1.0 V		50	60	-	
Output Noise - V_{IN} = V_{INMIN}, IL = IL_{MAX}	VGEN2ON				dBV/√Hz
100 Hz – 1.0 kHz		-	-	-115	
>1.0 kHz – 10 kHz		-	-	-126	
>10 kHz – 1.0 MHz		-	-	-132	
Spurs (32.768 kHz and harmonics)	VGEN2SP	-	-	-100	dB
Turn-on Time	VGEN2t_{ON}				ms
Enable to 90% of end value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0		-	-	1.0	
Turn-off Time (Disable to 10% of initial value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0)	VGEN2t_{OFF}	0.1	-	10	ms
VGEN2 ACTIVE MODE - AC					
Start-up Overshoot	V_{GEN2OS}				%
V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0		-	1.0	2.0	
Transient Load Response[39] - See Transient Response Waveforms on page 56	$V_{GEN2TLOR}$				
V_{IN} = V_{INMIN}, V_{INMAX}					
- VGEN2[2:0]=100 to 111		-	1.0	3.0	%
- VGEN2[2:0]=000 to 011		-	-	70	mV
Transient Line Response - See Transient Response Waveforms on page 56	$V_{GEN2TLIR}$				mV
IL = 75% of IL_{MAX}		-	5.0	8.0	
Mode Transition Time - See Transient Response Waveforms on page 56	VGEN2t_{MOD}				µs
From low power to active V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}		-	-	100	
Mode Transition Response - See Transient Response Waveforms on page 56	$V_{GEN2MTR}$				%
From low power to active and from active to low power V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}		-	1.0	2.0	
VGEN3 ACTIVE MODE - AC					
PSRR	VGEN3PSSR				dB
IL = 75% of IL_{MAX}, 20 Hz to 20 kHz, V_{IN} = V_{INMIN} +100 mV		35	40	-	
Vin=Vnom+1V		45	50	-	
Output Noise - V_{IN} = V_{INMIN}, IL = 75% of IL_{MAX}	VGEN3ON				
100 Hz – 1.0 kHz		-	20	-	dB/dec
>1.0 kHz – 1.0 MHz		-	-	1.0	µV/√Hz
Spurs	VGEN3SP				dB
32.768 kHz and harmonics		-	-	-100	

Notes
39. Guaranteed by design.

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 3.1 V ≤ BATT ≤ 4.8 V, --30 ≤ T_A ≤ 85°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VGEN3 ACTIVE MODE - AC (CONTINUED)					
Turn-on Time Enable to 90% of end value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VGEN3t_{ON}$	-	-	1.0	ms
Turn-off Time Disable to 10% of initial value V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	$VGEN3t_{OFF}$	0.1	-	5.0	ms
Start-up Overshoot V_{IN} = V_{INMIN}, V_{INMAX}, IL = 0	V_{GEN3OS}	-	1.0	2.0	%
Transient Load Response V_{IN} = V_{INMIN}, V_{INMAX} - VGEN3=1 - VGEN3=0	$V_{GEN3TLOR}$	 - -	 1.0 -	 2.0 70	 % mV
Transient Line Response (IL = 75% of IL_{MAX})	$V_{GEN3TLIR}$	-	5.0	8.0	mV
Mode Transition Time From low power to active V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$VGEN3t_{MOD}$	-	-	100	µs
Mode Transition Response From low power to active and from active to low power, V_{IN} = V_{INMIN}, V_{INMAX}, IL = IL_{MAXLP}	$V_{GEN3MTR}$	-	1.0	2.0	%
UVBUS - ACTIVE MODE DC					
Turn-On Time [40] - VBUS Rise Time por USB OTG with max loading of 6.5 µF+10 µF		-	-	100	ms
Turn-Off Time [40] - Disable to 0.8 V, per USB OTG specification parameter VA_SESS_VLD V_{IN} = V_{INMIN}, V_{INMAX}, IL=0		-	-	1.3	sec
ADC					
Conversion Time per Channel - PLLX[2:0]=100				10	µs
Turn On Delay If Switcher PLL was active If Switcher PLL was inactive		 - -	 0 5	 - 10	µs
TOUCH SCREEN					
Turn-on Time [40] - 90% of output				500	µs

Notes
40. Guaranteed by design.

TIMING DIAGRAMS

Figure 5 and Table 7 summarize the SPI electrical and timing requirements. The SPI input and output levels are set independently via the SPIVCC pin by connecting it to the desired supply. This would typically be tied to SW4 programmed for 1.80 V. The strength of the MISO driver is programmable through the SPIDRV[1:0] bits.

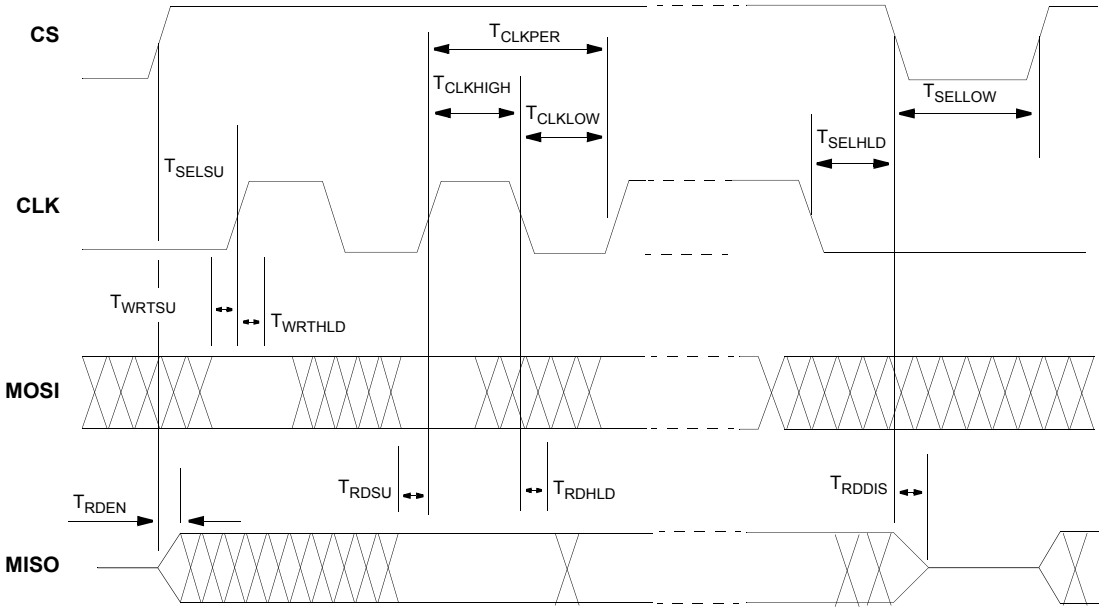


Figure 5. Timing Requirements

Table 7. Timing Parameter Description

PARAMETER	DESCRIPTION	T MIN (NS)
t_{SELSU}	Time CS has to be high before the first rising edge of CLK	15
t_{SELHID}	Time CS has to remain high after the last falling edge of CLK	15
t_{SELLOW}	Time CS has to remain low between two transfers	15
t_{CLKPER}	Clock period of CLK	38
$t_{CLKHIGH}$	Part of the clock period where CLK has to remain high	15
t_{CLKLOW}	Part of the clock period where CLK has to remain low	15
t_{WRTSU}	Time MOSI has to be stable before the next rising edge of CLK	4.0
t_{WRTHLD}	Time MOSI has to remain stable after the rising edge of CLK	4.0
t_{RDSU}	Time MISO will be stable before the next rising edge of CLK	4.0
t_{RDHLD}	Time MISO will remain stable after the falling edge of CLK	4.0
t_{RDEN}	Time MISO needs to become active after the rising edge of CS	4.0
t_{RDDIS}	Time MISO needs to become inactive after the falling edge of CS	4.0

Notes
41. This table reflects a maximum SPI clock frequency of 26 MHz. Slew rate for SPI MISO output driver is programmable from 0.16 to 0.66 V/ns

FUNCTIONAL DESCRIPTION

INTRODUCTION

FUNCTIONAL PIN DESCRIPTION

CHARGER

CHRGRAW

1. Charger input. The charger voltage is measured through an ADC at this pin. The UVBUS pin must be shorted to CHRGRAW in cases where the charger is being supplied from the USB cable. The minimum voltage for this pin depends on BATTMIN threshold value (see Battery Management).

2. Output to battery supplied accessories. The battery voltage can be applied to an accessory by enabling the charge path for the accessory via the CHRGRAW pin. To accomplish this, the charger needs to be configured in reverse supply mode.

CHRGCTRL1

Driver output for charger path FET M1.

CHRGCTRL2

Driver output for charger path FET M2.

CHRGISNS

Charge current sensing point 1. The charge current is read by monitoring the voltage drop over the charge current 100 mΩ sense resistor connected between CHRGISNS and BPSNS.

BPSNS

1. BP sense point. BP voltage is sensed at this pin and compared with the voltage at CHRGRAW.

2. Charge current sensing point 2. The charge current is read by monitoring the voltage drop over the charge current 100 mΩ sense resistor. This resistor is connected between CHRGISNS and BPSNS.

BP

This pin is the application supply point, the input supply to the IC core circuitry. The application supply voltage is sensed through an ADC at this pin.

BATTFET

Driver output for battery path FET M3. If no charging system is required, the pin BATTFET must be floating. When single path is implemented, it must be connected to ground.

BATTISNS

Battery current sensing point 1. The current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATT and BATTISNS.

BATT

Battery positive terminal. Battery current sensing point 2. The supply voltage of the battery is sensed through an ADC on this pin. The current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATT and BATTISNS.

BATTISNSCC

Accumulated current counter current sensing point. This is the coulomb counter current sense point. It should be connected directly to the 0.020 Ω sense resistor via a separate route from BATTISNS. The coulomb counter monitors the current flowing in/out of the battery by integrating the voltage drop over the BATTISNCC and the BATT pin.

CFP AND CFM

Accumulated current filter cap plus and minus terminals respectively. The coulomb counter will require a 10 µF output capacitor connected between these pins to perform a first order filtering of the signal across R1.

CHRGSE1B

An unregulated wall charger configuration can be built in which case this pin must be pulled low. When charging through USB, it can be left open since it is internally pulled up to VCORE. The recommendation is to place an external FET that can pull it low or left it open, depending on the charge method.

CHRGLED

Trickle LED driver output 1. Since normal LED control via the SPI bus is not always possible in the standalone operation, a current sink is provided at the CHRGLED pin. This LED is to be connected between this pin and CHRGRAW.

GNDCHRG

Ground for charger interface.

LED DRIVERS

SWLEDOUT

Boost converter output for serial LED drive. It provides up to 25.5 V for supplying LED strings driven by LEDMD, LEDAD and LEDKP.

GNDSWLED

Ground for boost converter for serial LED drive

LEDMD, LEDAD, AND LEDKP

LEDMD - Main display backlight LED driver output.

LEDAD - Auxiliary display backlight LED driver output.

LEDKP - Keypad lighting LED driver output.

Independent programmable current sink channels. LED strings must be connected from SWLEDOUT (anodes) to these pins (cathodes). When parallel strings are ganged together on a driver channel, ballasting resistance is recommended to help balance the currents in each leg.

LEDR, LEDG AND LEDB

General purpose LED driver output Red, Green and Blue respectively. Each channel provides flexible LED intensity control. These pins can also be used as general purpose open drain outputs for logic signaling, or as generic PWM generator outputs.

GNDLED E5

Ground for LED drivers

IC CORE

VCORE

Regulated supply output for the IC analog core circuitry. It is used to define the PUMS VIH level during initialization. The bandgap and the rest of the core circuitry are supplied from VCORE. Place a 2.2 µF capacitor from this pin to GNDCORE.

VCOREDIG

Regulated supply output for the IC digital core circuitry. No external DC loading is allowed on VCOREDIG. VCOREDIG is kept powered as long as there is a valid supply and/or coin cell. Place a 2.2 µF capacitor from this pin to GNDCORE.

REFCORE

Main bandgap reference. All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at REFCORE. No external DC loading is allowed on REFCORE. Place a 100 nF capacitor from this pin to GNDCORE.

GNDCORE

Ground for the IC core circuitry.

POWER GATING

PWGTDRV1 AND PWGTDRV2

Power Gate Drivers.

PWGTDRV1 is provided for power gating peripheral loads sharing the processor core supply domain(s) SW1, and/or SW2, and/or SW3. In addition, PWGTDRV2 provides support to power gate peripheral loads on the SW4 supply domain.

In typical applications, SW1, SW2, and SW3 will both be kept active for the processor modules in state retention, and SW4 retained for the external memory in self refresh mode. SW1, SW2, and SW3 power gating FET drive would typically be connected to PWGTDRV1 (for parallel NMOS switches). SW4 power gating FET drive would typically be connected to PWGTDRV2. When low power Off mode is activated, the power gate drive circuitry will be disabled, turning off the NMOS power gate switches to isolate the maintained supply domains from any peripheral loading.

SWITCHERS

SW1IN, SW2IN, SW3IN AND SW4IN

Switchers 1, 2, 3, and 4 input. Connect these pins to BP to supply Switchers 1, 2, 3, and 4.

SW1FB, SW2FB, SW3FB AND SW4FB

Switchers 1, 2, 3, and 4 feedback. Switchers 1, 2, 3, and 4 output voltage sense respectively. Connect these pins to the farther point of each of their respective SWxOUT pin, in order to sense and maintain voltage stability.

SW1OUT

Switcher 1 output. Buck switcher for processor core(s).

GNDSW1

Ground for Switcher 1.

SW2OUT

Switcher 2 output. Buck switcher for processor SOG, etc.

GNDSW2

Ground for Switcher 2.

SW3OUT

Switcher 3 output. Buck switcher for internal processor memory and peripherals.

GNDSW3

Ground for switcher 3.

SW4OUT

Switcher 4 output. Buck switcher for external memory and peripherals.

GNDSW4

Ground for switcher 4.

DVS1 AND DVS2

Switcher 1 and 2 DVS input pins. Provided for pin controlled DVS on the buck switchers targeted for processor core supplies. The DVS pins may be reconfigured for Switcher Increment / Decrement (SID) mode control. When transitioning from one voltage to another, the output voltage slope is controlled in steps of 25 mV per time step. These pins must be set high in order for the DVS feature to be enabled for each of switchers 1 or 2, or low to disable it.

SWBSTIN

Switcher BST input. The 2.2 µH switcher BST inductor must be connected here.

SWBSTOUT

Power supply for gate driver for the internal power NMOS that charges SWBST inductor. It must be connected to BP.

SWBSTFB

Switcher BST feedback. When SWBST is configured to supply the UVBUS pin in OTG mode the feedback will be switched to sense the UVBUS pin instead of the SWBSTFB pin.

GNDSWBST

Ground for switcher BST.

REGULATORS

VINIOHI

Input of VIOHI regulator. Connect this pin to BP in order to supply VIOHI regulator.

VIOHI

Output regulator for high voltage IO. Fixed 2.775 V output for high voltage level interface.

VINPLL AND VINDIG

The input of the regulator for processor PLL and Digital regulators respectively. VINDIG and VINPLL can be connected to either BP or a 1.8 V switched mode power supply rail, such as from SW4 for the two lower set points of each regulator (the 1.2 and 1.25 V output for VPLL, and 1.05 and 1.25 V output for VDIG). In addition, when the two upper set points are used (1.50 and 1.8V outputs for VPLL, and 1.65 and 1.8V for VDIG), they can be connected to either BP or a 2.2V nominal external switched mode power supply rail, to improve power dissipation.

VPLL

Output of regulator for processor PLL. Quiet analog supply (PLL, GPS).

VDIG

Output regulator Digital. Low voltage digital (DPLL, GPS).

VVIDEODRV

Drive output for VVIDEO external PNP transistor.

VVIDEO

Output regulator TV DAC. This pin must be connected to the collector of the external PNP transistor of the VVIDEO regulator.

VINAUDIO

Input regulator VAUDIO. Typically connected to BP.

VAUDIO

Output regulator for audio supply.

VINUSB2

Input regulator VUSB2. This pin must always be connected to BP even if the regulators are not used by the application.

VUSB2

Output regulator for powering USB PHY.

VINCAMDRV

1. Input regulator camera using internal PMOS FET. Typically connected to BP.

2. Drive output regulator for camera voltage using external PNP device. In this case, this pin must be connected to the base of the PNP in order to drive it.

VCAM

Output regulator for the camera module. When using an external PNP device, this pin must be connected to its collector.

VSDDRV

Drive output for the VSD external PNP transistor.

VSD

Output regulator for multi-media cards such as micro SD, RS-MMC.

VGEN1DRV

Drive output for the VGEN1 external PNP transistor.

VGEN1

Output of general purpose 1 regulator.

VGEN2DRV

Drive output for the VGEN2 external PNP transistor.

VGEN2

Output of general purpose 2 regulator.

VINGEN3DRV

1. Input for the VGEN3 regulator when no external PNP transistor used. Typically connected to BP.

2. Drive output for VGEN3 in case an external PNP transistor is used on the application. In this case, this pin must be connected the base of the PNP transistor.

VGEN3

Output of general purpose 3 regulator.

VSRTC

Output regulator for the SRTC module on the processor. The VSRTC regulator provides the CLK32KMCU output level (1.2 V). Additionally, it is used to bias the Low Power SRTC domain of the SRTC module integrated on certain FSL processors.

GNDREG1

Ground for regulators 1.

GNDREG2

Ground for regulators 2.

GNDREG3

Ground for regulators 3.

GPO1

General purpose output 1. Intended to be used for battery thermistor biasing. In this case, connect a 10 KΩ resistor from GPO1 to ADIN5, and one from ADIN5 to GND.

GPO2

General purpose output 2.

GPO3

General purpose output 3.

GPO4

General purpose output 4. It can be configured for a muxed connection into Channel 7 of the GP ADC.

CONTROL LOGIC

LICELL

Coin cell supply input and charger output. The LICELL pin provides a connection for a coin cell backup battery or supercap. If the main battery is deeply discharged, removed, or contact-bounced (i.e., during a power cut), the RTC system and coin cell maintained logic will switch over to the LICELL for backup power. This pin also works as a current-limited voltage source for battery charging. A small capacitor should be placed from LICELL to ground under all circumstances.

XTAL1

32.768 kHz Oscillator crystal connection 1.

XTAL2

32.768 kHz Oscillator crystal connection 2.

GNDRTC

Ground for the RTC block.

CLK32K

32 kHz Clock output for peripherals. At system start-up, the 32 kHz clock is driven to CLK32K (provided as a peripheral clock reference), which is referenced to SPIVCC. The CLK32K is restricted to state machine activation in normal on mode.

CLK32KMCU

32 kHz Clock output for processor. At system start-up, the 32 kHz clock is driven to CLK32KMCU (intended as the CKIL input to the system processor) referenced to VSRTC. The driver is enabled by the start-up sequencer and the CLK32KMCU is programmable for Low Power Off mode control by the state machine.

$\overline{\text{RESETB}}$ AND $\overline{\text{RESETBMCU}}$

Reset output for peripherals and processor respectively. These depend on the Power Control Modes of operation (See Functional Device Operation on page 48). These are meant as reset for the processor, or peripherals in a power up condition, or to keep one in reset while the other is up and running.

WDI

Watchdog input. This pin must be high to stay in the On mode. The WDI IO supply voltage is referenced to SPIVCC (normally connected to SW4=1.8 V). SPIVCC must therefore remain enabled to allow for proper WDI detection. If WDI goes low, the system will transition to the Off state or Cold Start (depending on the configuration).

STANDBY AND STANDBYSEC

Standby input signal from processor and from peripherals respectively.

To ensure that shared resources are properly powered when required, the system will only be allowed into Standby when both the application processor (which typically controls the STANDBY pin) and peripherals (which typically control the STANDBYSEC pin) allow it. This is referred to as a Standby event.

The Standby pins are programmable for Active High or Active Low polarity, and that decoding of a Standby event will take into account the programmed input polarities associated with each pin. Since the Standby pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes.

Table 8. Standby Control Pins

STANDBY (PIN)	STANDBYINV (SPI BIT)	STANDBYSEC (PIN)	STANDBYSECINV (SPI BIT)	STANDBY CONTROL[42]
0	0	x	x	0
x	x	0	0	0
1	1	x	x	0
x	x	1	1	0
0	1	0	1	1
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1

Notes

42. STANDBY = 0: System is not in Standby; STANDBY=1: System is in Standby and Standby programmability is activated.

The state of the Standby pins only have influence in the On mode and are therefore ignored during start up and in the Watchdog phase. This allows the system to power up without concern of the required Standby polarities, since software can make adjustments accordingly, as soon as it is running.

INT

Interrupt to processor. Unmasked interrupt events are signaled to the processor by driving the INT pin high.

PWRON1, 2 AND 3

A turn on event can be accomplished by connecting an open drain NMOS driver to the PWRONx pin of the 13892, so that it is in effect a parallel path for the power key.

PUMS1 AND PUMS2

Power up mode supply setting. Default start-up of the device is selectable by hardwiring the Power Up Mode Select pins. The Power Up Mode Select pins (PUMS1 and PUMS2) are used to configure the start-up characteristics of the regulators. Supply enabling and output level options are selected by hardworking the PUMS pins for the desired configuration.

The following power up defaults table shows the initial setup for the voltage level of the switchers and regulators, and if they get enabled or not, according to the PUMS pins configuration.

Table 9. Power Up Defaults

i.MX	37/51	37/51	37/51	37/51	35	27/31
PUMS1	**GND**	**OPEN**	**VCOREDIG**	**VCORE**	**GND**	**OPEN**
PUMS2	**OPEN**	**OPEN**	**OPEN**	**OPEN**	**GND**	**GND**
SW1[43]	0.775	1.050	1.050	0.775	1.200	1.200
SW2[43]	1.025	1.225	1.225	1.025	1.350	1.450
SW3[43]	1.200	1.200	1.200	1.200	1.800	1.800
SW4[43]	1.800	1.800	1.800	1.800	1.800	1.800
SWBST	Off	Off	Off	Off	5.000	5.000
VUSB	3.300[44]	3.300[44]	3.300[44]	3.300[44]	3.300[46]	3.300[46]
VUSB2	2.600	2.600	2.600	2.600	2.600	2.600
VPLL	1.800	1.800	1.800	1.800	1.500	1.500
VDIG	1.250	1.250	1.250	1.250	1.250	1.250
VIOHI	2.775	2.775	2.775	2.775	2.775	2.775
VGEN2	3.150	Off	3.150	Off	3.150	3.150
VSD	Off	Off	Off	Off	3.15	3.15

Notes

43. The switchers SWx are activated in PWM pulse skipping mode allowed when enabled by the startup sequencer.
44. USB supplies VUSB, is only enabled if 5.0 V is present on UVBUS.
45. The following supplies are not included in the matrix, since they are not intended for activation by the start-up sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO.
46. SWBST = 5.0 V, powers up, as does VUSB, regardless of the 5.0 V present on UVBUS. By default VUSB will be supplied by SWBST.

Table 10. Power Up Sequence

Tap x 2.0 ms	PUMS2 = OPEN (I,MX37,i.MX51)	PUMS2 = GND (i.MX35,i.MX27)
0	SW2	SW2
1	SW4	VGEN2
2	VIOHI	SW4
3	VGEN2	VIOHI, VSD
4	SW1	SWBST, VUSB(50)
5	SW3	SW1
6	VPLL	VPLL
7	VDIG	SW3
8		VDIG
9	VUSB(49), VUSB2	VUSB2

Notes
47. Time slots may be included for blocks which are defined by the PUMS pins as disabled, to allow for potential activation.
48. The following supplies are not included in the matrix, since they are not intended for activation by the start-up sequencer: VCAM, VGEN1, VGEN3, VVIDEO, and VAUDIO. SWBST is not included on the PUMS2 = Open column
49. USB supplies VUSB, is only enabled if 5.0 V is present on UVBUS.
50. SWBST = 5.0 V, powers up, as does VUSB, regardless of the 5.0 V present on UVBUS. By default VUSB will be supplied by SWBST.

MODE

USB LBP mode, normal mode, test mode selection & anti-fuse bias. During evaluation and testing, the IC can be configured for normal operation or test mode via the MODE pin as summarized in the following table.

MODE PIN STATE	MODE
Ground	Normal Operation
VCOREDIG	USB Low Power Boot Allowed
VCORE	Test Mode

GNDCTRL

Ground for control logic.

SPIVCC

Supply for SPI bus and audio bus

CS

CS held low at Cold Start configures the interface for SPI mode. Once activated, CS functions as the SPI Chip Select. CS tied to VCORE at Cold Start configures the interface for I^2C mode; the pin is not used in I^2C mode other than for configuration.

Because the SPI interface pins can be reconfigured for reuse as an I^2C interface, a configuration protocol mandates that the CS pin is held low during a turn on event for the IC (a weak pull-down is integrated on the CS pin).

CLK

Primary SPI clock input. In I^2C mode, this pin is the SCL signal (I^2C bus clock).

MOSI

Primary SPI write input. In I^2C mode, the MOSI pin hard wired to ground or VCORE is used to select between two possible addresses (A0 address selection).

MISO

Primary SPI read output. In I^2C mode, this pin is the SDA signal (bi-directional serial data line).

GNDSPI

Ground for SPI interface.

USB

UID

This pin identifies if a mini-A or mini-B style plug has been connected to the application. The state of the ID detection can be read via the SPI, to poll dedicated sense bits for a floating, grounded, or factory mode condition on the UID pin.

Table 11. UID Pin Levels

UID PIN EXTERNAL CONNECTION	UID PIN VOLTAGE	ACCESSORY
Resistor to Ground	0.18*VCORE<UID<0.77*VCORE	Non-USB accessory is attached
Grounded	0<UID<0.12*VCORE	A type plug (USB Host)
Floating	0.89*VCORE<UID<VCORE	B type plug (USB peripheral, OTG device or no device) is attached
Voltage Applied	3.6 V<UID[51]	Factory mode

Notes
51. UID maximum voltage is 5.25 V

UVBUS

1. USB transceiver cable interface.
2. OTG supply output.

When SWBST is configured to supply the UVBUS pin in OTG mode, the feedback will switch to sense the UVBUS pin instead of the SWBSTFB pin.

VUSB

This is the regulator used to provide a voltage to an external USB transceiver IC.

VINUSB

Input option for VUSB; supplied by SWBST. This pin is internally connected to the UVBUS pin for OTG mode operation (for more details about OTG mode See OTG mode (On the Go) on page 64).

Note: When VUSBIN =1 , UVBUS will be connected via internal switches to VINUSB and incur some current drain on that pin, as much as 270uA maximum, so care must be taken to disable this path and set this SPI bit (VUSBIN) to 0 to minimize current drain, even if SWBST and/or VUSB are disabled.

VBUSEN

External VBUS enable pin for the OTG supply. VBUS is defined as the power rail of the USB cable (+5.0 V).

A TO D CONVERTER

Note: The ADIN5/6/7 inputs must not exceed BP.

ADIN5

ADC generic input channel 5. ADIN5 may be used as a general purpose unscaled input, but in a typical application, ADIN5 is used to read out the battery pack thermistor. The thermistor must be biased with an external pull-up to a voltage rail greater than the ADC input range. In order to save current when the thermistor reading is not required, it can be biased from one of the general purpose IOs such as GPO1. A resistor divider network should assure the resulting voltage falls within the ADC input range, in particular when the thermistor check function is used.

ADIN6

ADC generic input channel 6. ADIN6 may be used as a general purpose unscaled input, but in a typical application, the PA thermistor is connected here.

ADIN7

ADC generic input channel 7, group 1. ADIN7 may be used as a general purpose unscaled input or as a divide by 2 scaled input. In a typical application, an ambient light sensor is connected here.

A second general purpose input ADIN7B is available on channel 7. This input is muxed on the GPO4 pin. In the application, a second ambient light sensor is supposed to be connected here.

TSX1 AND TSX2, TSY1 AND TSY2

Note: The TS[xy] [12] inputs must not exceed BP or VCORE.

Touch Screen Interfaces X1 and X2, Y1 and Y2. The touch screen X plate is connected to TSX1 and TSX2, while the Y plate is connected to Y1 and Y2. In inactive mode, these pins can also be used as general purpose ADC inputs. They are respectively mapped on ADC channels 4, 5, 6, and 7.

In interrupt mode, a voltage is applied to the X-plate (TSX2) via a weak current source to VCORE, while the Y-plate is connected to ground (TSY1).

TSREF

Touch Screen Reference regulator. This regulator is powered from VCORE. In applications not supporting touch screen, the TSREF can be used as a low current general purpose regulator, or it can be kept disabled and the bypass capacitor omitted.

ADTRIG

ADC trigger input. A rising edge on this pin will start an ADC conversion.

GNDADC

Ground for A to D circuitry.

THERMAL GROUNDS

GNDSUB1-9

Non critical signal grounds and thermal heat sinks.

FUNCTIONAL DEVICE OPERATION

PROCESSOR LOGIC INTERFACING

CLOCK GENERATION

A system clock is generated for internal digital circuitry as well as for external applications utilizing the clock output pins. A crystal oscillator is used for the 32.768 kHz time base and generation of related derivative clocks. If the crystal oscillator is not running (for example, if the crystal is not present), an internal 32 kHz oscillator will be used instead.

Support is also provided for an external Secure Real Time Clock (SRTC), which may be integrated on a companion system processor IC. For media protection in compliance with Digital Rights Management (DRM) system requirements, the CLK32KMCU can be provided as a reference to the SRTC module, where tamper protection is implemented.

The internal 32kHz oscillator is an integrated backup for the crystal oscillator and provides a 32.768 kHz nominal frequency at 20% accuracy if running. The internal oscillator only runs if a valid supply is available at BP and would not be used as long as the crystal oscillator is active. In absence of a valid supply at the BP supply node (for instance due to a dead battery), the crystal oscillator continues running supplied from the coin cell battery until the coin cell is depleted. All control functions will run off the crystal derived frequency, occasionally referred to as “32 kHz” for brevity’s sake.

The crystal oscillator has been optimized for use in conjunction with the Micro Crystal CC7V-T1A-

32.768 kHz-9.0 pF-30 ppm or equivalent (such as the Micro Crystal CC5V-T1A or Epson FC135) is capable of handling its parametric variations.

The electrical characteristics of the 32 kHz crystal oscillator are given in Tables 4 and 6, taking into account the crystal characteristics noted previously. The oscillator accuracy depends largely on the temperature characteristics of the used crystal. Application circuits can be optimized for required accuracy by adapting the external crystal oscillator network (via component accuracy and/or tuning).

Additionally, a clock calibration system is provided to adjust the 32,768 cycle counter that generates the 1.0 Hz timer and RTC registers; see the RTC section for more detail.

SRTC SUPPORT AND VSRTC

When configured for DRM mode (SPI bit DRM=1), the CLK32KMCU driver will be kept enabled through all operational states to ensure that the SRTC module always has its reference clock. If DRM=0, the CLK32KMCU driver will not be maintained in the Off state.

It is also necessary to provide a means for the processor to do an RTC initiated wake-up of the system if it has been programmed for such capability. This can be accomplished by connecting an open drain NMOS driver to the PWRON pin of 13892 so that it is in effect a parallel path for the power key. The 13892 will not be able to discern the turn on event from a normal power key initiated turn on, but the processor should have the knowledge since the RTC initiated turn on is generated locally.

The VSRTC regulator provides the CLK32KMCU output level. It is also used to bias the Low Power SRTC domain of the SRTC module integrated on certain FSL processors. The VSRTC regulator is enabled as soon as the RTCPORB is detected. The VSRTC cannot be disabled.

VSRTC

REAL TIME CLOCK

A Real Time Clock (RTC) is provided with time and day counters as well as an alarm function. The RTC utilizes the 32.768 kHz crystal oscillator for the time base, and is powered by the coin cell backup supply when BP has dropped below operational range. In configurations where the SRTC is used, the RTC can be disabled to conserve current drain by setting the RTCDIS bit to a 1 (defaults on at power up).

TIME AND DAY COUNTERS

The 32.768 kHz clock is divided down to a 1.0 Hz time tick which drives a 17 bit Time Of Day (TOD) counter. The TOD counter counts the seconds during a 24 hour period from 0 to 86,399 and will then roll over to 0. When the roll over occurs, it increments the 15 bit DAY counter. The DAY counter can count up to 32767 days. The 1.0 Hz time tick can be used to generate a 1.0 Hz interrupt if unmasked.

TIME OF DAY ALARM

A Time Of Day Alarm (TODA) function can be used to turn on the application and alert the processor. If the application is already on, the processor will be interrupted. The TODA and DAYA registers are used to set the alarm time. When the TOD counter is equal to the value in TODA and the DAY counter is equal to the value in DAYA, the TODAI interrupt will be generated.

TIMER RESET

As long as the supply at BP is valid, the real time clock will be supplied from VCORE. If not, it can be backed up from a coin cell via the LICELL pin. When the backup voltage drops below RTCUVDET, the RTCPORB reset signal is generated and the contents of the RTC will be reset. Additional registers backed up by coin cell will also reset with RTCPORB. To inform the processor that the contents of the RTC are no longer valid due to the reset, a timer reset interrupt function is implemented with the RTCRSTI bit.

COIN CELL BATTERY BACKUP

The LICELL pin provides a connection for a coin cell backup battery or supercap. If the main battery is deeply discharged, removed, or contact-bounced (i.e., during a power cut), the RTC system and coin cell maintained logic will switch over to the LICELL for backup power. A small capacitor should be placed from LICELL to ground under all circumstances.

Coin cells can get damaged and their lifetime reduced when deeply discharged. In order to avoid this, the internal circuitry supplied from LICELL is disconnected for voltages below the coin cell disconnect threshold. This will also cause the ADC reading of the coin cell voltage to yield zero.

The coin cell charger circuit will function as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell voltage is programmable from 2.5 to 3.3 V in 0.1 V steps, excepting 2.6 V. The coin cell charger voltage is programmable in the ON state where the charge current is fixed at ICOINHI. When the device is working in any of the low Power Off modes, the coin cell charger will also go into a low power mode in which the current it supplies to the coin cell will be reduced in order to save power.

Table 12. 13892 Coin Cell Battery Electrical Characteristics

PARAMETER	TYP	UNITS
Voltage Accuracy	100	mV
Coin Cell Charge Current in On and Watchdog modes ICOINHI	60	µA
Coin Cell Charge Current in Off and Low Power Off modes (User Off/Memory Hold) ICOINLO	10	µA
Current Accuracy	30	%
LICELL Bypass Capacitor	100	nF
LICELL Bypass Capacitor as coin cell	4.7	µF

CONTROL INTERFACE SPI/I2C

The IC contains a number of programmable registers for control and communication. The majority of registers are accessed through an SPI interface in a typical application. The same register set may be alternatively accessed with an I^2C interface that is muxed on SPI pins. The following table describes the muxed pin options for the SPI and I^2C interfaces.

Table 13. 13892 Muxed Pin Options for SPI and I^2C Interfaces (SPI Functions)

PIN NAME	SPI MODE FUNCTIONALITY
CS	Configuration (52) Chip Select
CLK	SPI Clock
MISO	Master In, Slave Out (data input)
MOSI	Master Out, Slave In (data input)

Notes

52. CS held low at Cold Start configures the interface for SPI mode; once activated, CS functions as the SPI Chip Select.

SPI INTERFACE

The IC contains a SPI interface port which allows access by a processor to the register set. Via these registers, the resources of the IC can be controlled. The registers also provide status information about how the IC is operating as well as information on external signals.

The SPI port utilizes 32-bit serial data words comprised of 1 write/read_b bit, 6 address bits, 1 null bit, and 24 data bits. The addressable register map spans 64 registers of 24 data bits each.

I2C INTERFACE

When configured for I^2C mode, the interface may be used to access the complete register map. Since SPI configuration is more typical, references within this document will generally refer to the common register set as a “SPI map” and bits as “SPI bits”. However, it should be understood that access reverts to I^2C mode when configured as such.

The SPI pins CLK and MISO are reused for the SCL and SDA lines respectively. Selection of I^2C mode for the interface is configured by hardwiring the CS pin to VCORE on the application board.

Table 14. Muxed Pin Options for SPI and I2C Interfaces (I^2C Functions)

PIN NAME	I^2C Mode Functionality
CS	Configuration(53)
CLK	SCL: I^2C_{BUS} clock
MISO	SDA: Bi-directional serial data line
MOSI	A0 Address Selection(54)

Notes

53. CS tied to VCORE at Cold Start configures interface for I^2C mode; the pin is not used in I^2C mode other than for configuration.
54. In I^2C mode, the MOSI pin hard wired to ground or VCORE is used to select between two possible addresses.

The I2C mode of the interface is implemented generally following the Fast Mode definition, which supports up to 400 kbits/s operation. (exceptions to the standard are noted to be 7-bit only addressing and no support for General Call addressing).

Timing diagrams, electrical specifications, and further details can be found in the I2C specification, which is available for download at:

http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

INTERRUPT CONTROL

The system is informed about important events based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INT pin high; this is true whether the communication interface is configured for SPI or I^2C.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. Each interrupt can be cleared by writing a 1 to the appropriate bit in the Interrupt Status register. This will also cause the interrupt line to go low. If a new interrupt occurs while the processor clears an existing interrupt bit, the interrupt line will remain high.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the interrupt line will not go high. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the interrupt line will go high after unmasking.

Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the INT summary table following later in this chapter. Due to the asynchronous nature of the debounce timer the effective debounce time can vary slightly.

SUPPLIES

A system power scheme for portable devices is provided which includes both switching and linear regulators. Various operational modes are available for the power circuitry, which may be accessible through SPI programming and the state of the STANDBY pins. Programmable Standby mode configuration allows automated system level control to optimize quiescent efficiency without the need for or latency of SPI intervention.

The switch mode supply subsystem include a core block for clock generation, 4 step down (buck) switching regulators and two step up (boost) switching regulators.

Linear regulators are provided for key power domains not supplied directly by switching regulators or the battery. Pass devices are integrated for most regulators for board area and cost advantages. External PNP pass devices are used selectively to help manage internal power dissipation.

A general application of the power tree is illustrated in the Figure 6 diagram. Supply names are suggestive of typical applications, but not restrictive.

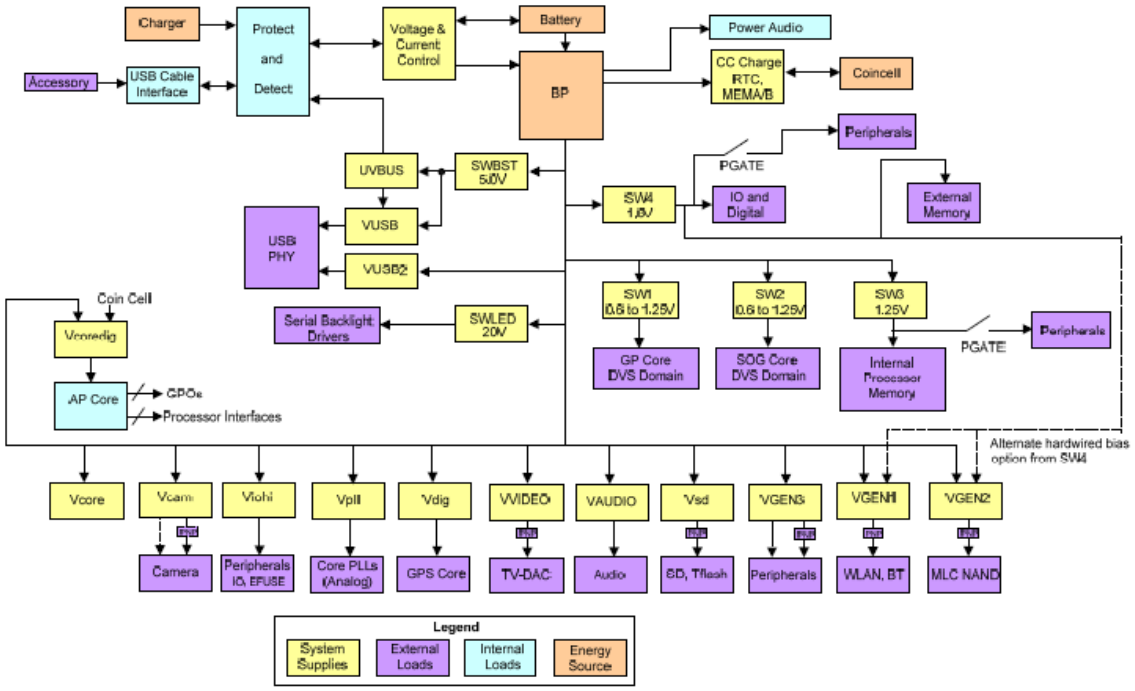


Figure 6. General Application of the Power Tree

The minimum operating voltage for the supply tree while maintaining the performance as specified is 3.0 V. For lower voltages, the performance may be degraded.

BUCK CONVERTERS

Four buck switchers are provided with integrated power switches and synchronous rectification. In a typical application, SW1 and SW2 are used for supplying the Application Processor core power domains. Split power domains allow independent DVS control for processor power optimization, or to support technologies with a mix of device types with different voltage ratings. SW3 is used for powering internal processor memory as well as low voltage peripheral devices and interfaces, which can run at the same voltage level. SW4 is used for powering external memory as well as low voltage peripheral devices and interfaces, which can run at the same voltage level.

An anticipated platform use case applies SW1 and SW2 to processor power domains that require voltage alignment to allow direct interfacing without bandwidth limiting synchronizers.

The buck switchers are supplied from the system supply BP, which is drawn from the main battery or the battery charger (when present). Figure 7 shows a high level block diagram of the buck switchers.

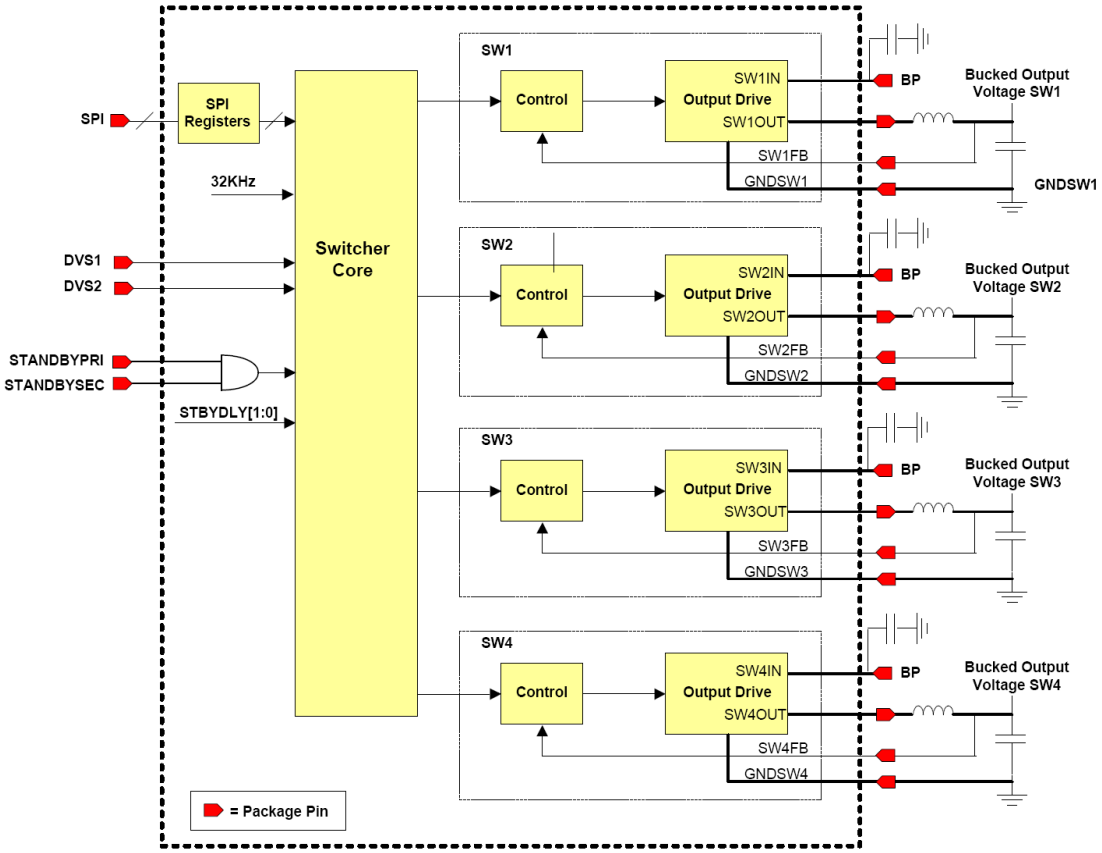


Figure 7. Buck Switch Diagram

The Buck switcher topology includes an integrated synchronous rectifier, meaning that the rectifying diode is implemented on chip as a low ohmic FET. The placement of an external diode is therefore not required, but overall switcher efficiency may benefit from this. The buck converters permit a 100% duty cycle operation.

During normal operation several power modes are possible, depending on the loading. For medium and full loading, synchronous PWM control is the most efficient while maintaining a constant switching frequency.

The output voltages of the buck switchers are SPI configurable and two output ranges are available, individually programmed with SWxHI for SW2, SW3, and SW4 bucks, SW1 is limited to only one output range. Presets are available for both the Normal and Standby operation.

The first voltage range that applies for all the Buck switchers goes from 0.6 to 1.375 V in 25 mV steps. The second one does not apply for SW1 and goes from 1.1 to 1.85 V also in 25 mV steps.

SW1 and SW2 include pin controlled Dynamic Voltage Scaling (DVS) operation. When transitioning from one voltage to another, the output voltage slope is controlled in steps of 25 mV per time step (time step as defined for DVS stepping for SW1 and SW2, fixed at 4.0 µs for SW3, and SW4). This allows for support of dynamic voltage scaling (DVS) by using SPI driven voltage steps, state machine defined modes, and direct DVSx pin control. SW1 and SW2 also include the Switcher Increment/Decrement (SID) feature, with which, an increment command will increase the set point voltage by a single 25 mV step, and a decrement command will decrease it in the same amount of voltage. The transition time for the step will be the same as programmed for the DVS feature. Maximum and minimum voltages are programmable to ensure the switcher voltage does not go out a specific range. Panic mode is also included to quickly return the switcher voltage to its normal programmed set point.

When initially activated, switcher outputs will apply controlled stepping to the programmed value. The soft start feature limits the inrush current at startup.

Point of Load feedback is intended for minimizing errors due to board level IR drops.

MODES OF OPERATION

Two PWM modes are available:

PWM-NPS: sacrifices low load efficiency for a continuous switching operation.

PWM-PS: offers better low load efficiency by allowing the absence of switching cycles at low output loading. This pulse

skipping feature improves efficiency by reducing dynamic switching losses simply by switching less often.

In its lowest power mode, the switcher can regulate using hysteresis control known as a Pulse Frequency Modulation (PFM) control scheme. The frequency spectrum will be a function of input and output voltage, loading, and the external components. Due to its spectral variance and lighter drive capability, PFM mode is generally reserved for non-active radio modes and Deep Sleep operation.

CURRENT LIMITER

A built in current limiter ensures that during normal operation the maximum current through the coil is not exceeded (refer to Electrical Characteristics). This current limiter can be disabled by SPI bits.

SWITCHING FREQUENCY

A PLL generates the switcher system clocking from the 32.768 kHz crystal oscillator reference. To allow for spectral optimization for reduction of spurious influence in a radion environment, the PLL can be programmed via SPI from a multiplication factor of 84 to 105, in steps of 3.

BOOST CONVERTERS

SWBST

SWBST is a boost switching regulator with a fixed 5.0 V output. It runs at 2/3 of the switcher PLL frequency. SWBST supplies the VUSB regulator for the USB system in OTG mode, as well as the VBUS voltage at the UVBUS pin.

When SWBST is configured to supply the UVBUS pin in OTG mode, the feedback will be switched to sense the UVBUS pin instead of the SWBSTFB pin. Therefore, when driving the VBUS for OTG mode, the output of the switcher may rise to 5.75 V to compensate for the voltage drops in the internal switches. Note that the parasitic leakage path for a boost switcher will cause the output voltage SWBSTOUT and SWBSTFB to sit at a Schottky drop below the battery voltage, whenever SWBST is disabled. The switching NMOS transistor is integrated on-chip. An external fly back Schottky diode, inductor, and capacitor are required.

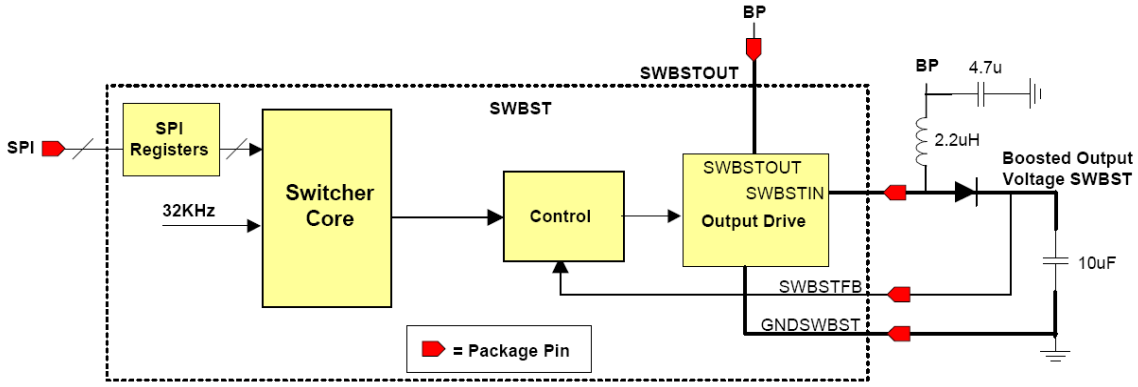


Figure 8. 13892 SWBST Block Diagram.

Main characteristics of SWBST are summarized in Tables 4 and 6.

SWLED

The supply to the serial LEDs is provided by an inductive boost switcher as illustrated in Figure 9. The boost converter is automatically enabled when one or more backlight drivers are enabled.

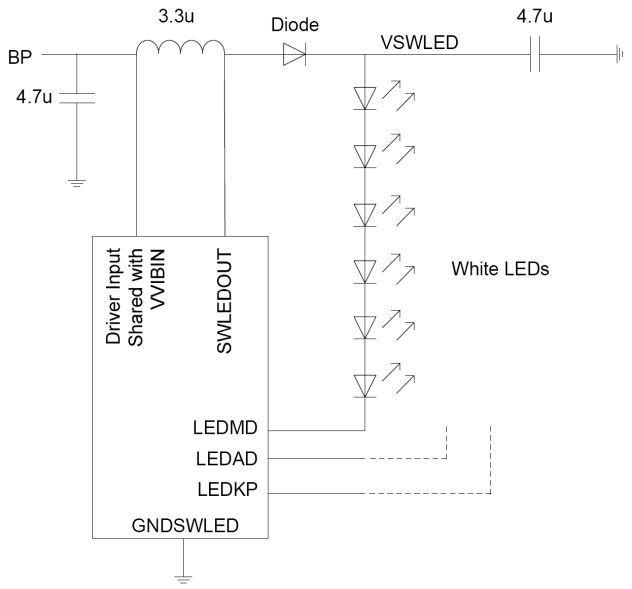


Figure 9.

The boost converter output voltage is adapted automatically to the load such that the headroom on the active LED drivers is maintained at a sufficient level (output voltage range from BP to 25.5 V). This allows for a very efficient backlighting scheme. The control is time continuous. When accounting for the diode drop and the driver headroom, the total available supply for the LEDs will be sufficient for up to 6 white LEDs in series. The boost converter runs at 2/3 of the switcher PLL generated frequency.

PROTECTION FUNCTIONS

Current Limit

SWBST has an over-current limit protection of 1.5 A. A portion of the output current is sensed across an internal sense resistor which creates a drop that is then compared to a fixed voltage. The output of the comparator is the flag of over-current in the output driver of the boost converter. When an over-current is detected, the PWM cycle is stopped by turning off the internal NMOS, which allows the current in the coil to decrease.

Over-voltage Protection

The boost converter contains a two phase over-voltage detection to prevent the SWLEDOUT from rising higher than 28V.

LDOS

The following is a description of the linear regulators. For convenience these regulators are named to indicate their typical or possible applications, but the supplies are not limited to these uses, and may be applied to any loads within the specified regulator capabilities.

A low power standby mode controlled by STANDBY is provided in which the bias current is aggressively reduced. This mode is useful for deep sleep operations, where certain supplies cannot be disabled, but active regulation can be tolerated with lesser parametric requirements. The output drive capability and performance are limited in this mode.

Apart from the integrated linear regulators, there are also GPO output pins provided to enable and disable discrete regulators or functional blocks, or to use as general purpose outputs for any system need. For example, one application may be to enable a battery pack thermistor bias in synchronization with timed ADC conversions.

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at REFCORE. The bandgap and the rest of the core circuitry is supplied from VCORE. The performance of the regulators is directly dependent on the performance of VCOREDIG and the bandgap. No external DC loading is allowed on VCOREDIG or REFCORE. VCOREDIG is kept powered as long as there is a valid supply and/or coin cell. The following table captures the main characteristics of the core circuitry.

Table 15. Core Circuitry Main Characteristics

REFERENCE	PARAMETER	TYPICAL
VCOREDIG (Digital core supply)	Output voltage in ON mode (55), (56)	1.5 V
	Output voltage in OFF mode(56)	1.2 V
	Bypass Capacitor	2.2 µF typ (0.65 µF derated)
VCORE (Analog core supply)	Output voltage in ON mode (55), (56)	2.775 V
	Output voltage in OFF mode(56)	0 V
	Bypass Capacitor	2.2 µF typ (0.65 µF derated)
REFCORE (Bandgap/Regulator Reference)	Output voltage(55)	1.20 V
	Bypass Capacitor	100 nF typ (65 nF derated)

Notes

55. 3.0 V < BP < 4.65 V, no external loading on VCOREDIG, VCORE, or REFCORE. Extended operation down to UVDET with VCORE down to UVDET, but no system malfunction.
56. The core is in On mode when charging, or when the state machine of the IC is not in the Off mode, nor in the power cut mode. Otherwise, the core is in Off mode.

The transient load and line response are specified with the waveforms as depicted in Figure 10. Note that where the transient load response refers to the overshoot only, so excluding the DC shift itself, the transient line response refers to the sum of both overshoot and DC shift. This is also valid for the mode transition response.

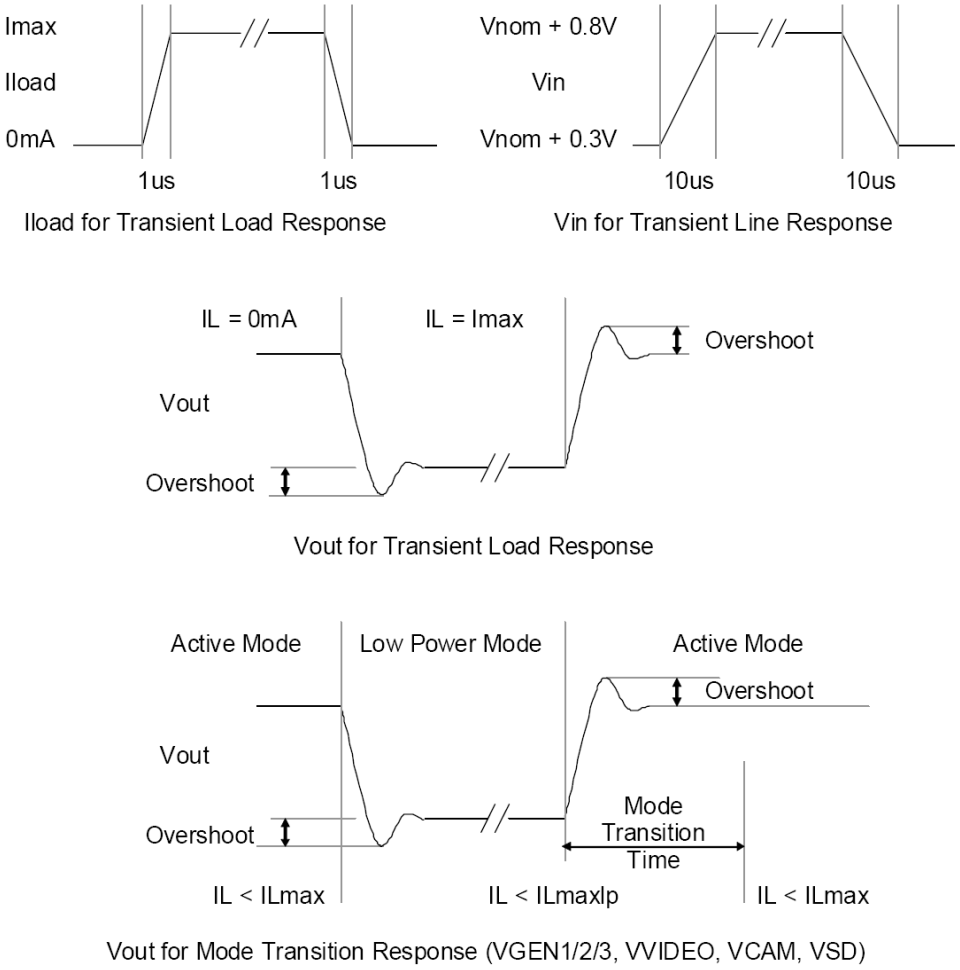


Figure 10. Transient Response Waveforms

VAUDIO AND VVIDEO SUPPLIES

The primary applications of these power supplies are for audio, and TV-DAC. These supplies could also be used for other peripherals if one of these functions is not required. Low Power modes and programmable Standby options can be used to optimize power efficiency during deep sleep modes.

VAUDIO is implemented with an integrated PMOS pass FET and has a dedicated input supply pin VINAUDIO.

The nominal output voltage (V_{NOM} as referred in Table Table 4) of VVIDEO can go from 2.5 to 2.7 V on 0.1 V steps, it also can be programmed to be 2.775 V. Its output current depends on the external pass device.

The nominal output voltage (V_{NOM} as referred in Table Table 4) of VAUDIO can be programmed to be 2.3, 2.5, 2.775 or 3.0 V.

LOW VOLTAGE SUPPLIES

VDIG and VPLL are provided for isolated biasing of the Baseband system PLLs for clock generation in support of protocol and peripheral needs. Depending on the lineup and power requirements, these supplies may be considered for sharing with other loads, but noise injection must be avoided and filtering added if necessary, to ensure suitable PLL performance. The VDIG and VPLL regulators have a dedicated input supply pin: VINDIG for the VDIG regulator and VINPLL for the VPLL regulator. VINDIG and VINPLL can be connected to either BP or a 1.8 V switched mode power supply rail such as from SW4 for the two lower set points of each regulator (1.2 V and 1.25 V output for VPLL and 1.05 and 1.25 V output for VDIG). In addition, when the two upper set points are used (1.50 V and 1.8 V output for VPLL and 1.65 V and 1.8 V for VDIG) can be connected to either BP or a 2.2 V nominal external switched mode power supply rail to improve power dissipation.

The nominal programmable output voltage of VPLL (V_{NOM} as referred in Table 4) could be 1.2, 1.25, 1.50 or 1.8 V, while VDIG can be configured to 1.05, 1.25, 1.65 and 1.8 V.

PERIPHERAL INTERFACING

IC interfaces in the lineups generally fall in two categories: low voltage IO primarily associated with the AP IC and certain peripherals at the SPIVCC level (powered from SW4), and a higher voltage interface level associated with other peripherals not compatible with the 1.8 V SPIVCC. VIOHI is provided at a fixed nominal output voltage 2.775 V level (V_{NOM} as referred in Table 4) for such interfaces, and may also be applied to other system needs within the guidelines of the regulator specifications. The input VINIOHI is not only used by the VIOHI regulator, but also by other blocks. Therefore it should always be connected to BP, even if the VIOHI regulator is not used by the system.

VIOHI has an internal PMOS pass FET which will support loads up to 100 mA.

CAMERA

The camera module is supplied by the regulator VCAM. This allows for powering the entire module independent of the rest of other parts of the system, as well as to select from a number of VCAM output levels for camera vendor flexibility. In applications with a dual camera, it is anticipated that only one of the two cameras is active at a time, allowing the VCAM supply to be shared between them.

VCAM has an internal PMOS pass FET, which will support up to 2Mpixel Camera modules (<65 mA). To support higher resolution cameras, an external PNP is provided. The external PNP configuration is offered to avoid excess on-chip power dissipation at high loads and large differential between BP and output settings. For lower current requirements, an integrated PMOS pass FET is included. The input pin for the integrated PMOS option is shared with the base current drive pin for the PNP option.

The nominal output voltage of this regulator (V_{NOM} as referred in Table 4) is SPI configurable, and can be 2.5, 2.6, 2.75, or 3.0 V. The output current when working with the internal pass FET is 65 mA, and could be up to 250 mA when working with an external PNP.

MULTI-MEDIA CARD SUPPLY

This supply domain is generally intended for user accessible multi-media cards such as Micro-SD (TransFlash), RS-MMC, and the like. An external PNP is utilized for this LDO to avoid excess on-chip power dissipation at high loads and large differential between BP and output settings. The external PNP device is always connected to the BP line in the application. VSD may also be applied to other system needs within the guidelines of the regulator specifications. At the 1.8 V set point, the VSD regulator can be powered from and external buck switcher (2.2 V typ) for an efficiency advantage and reduced power dissipation in the pass devices.

This regulator can be configured for nominal output voltages (V_{NOM} as referred in Table 4) of 1.8, 2.00, 2.60, 2.70, 2.8, 2.9, 3.00, and 3.15 V. All of these configurations can draw a current of 250 mA.

USB SUPPLY

The VUSB regulator is used to supply a nominal output voltage (V_{NOM} as referred in Table 4) of 3.3 V to the external USB PHY. The UVBUS line of the USB interface is supplied by the host, in the case of host mode operation, or by the integrated VBUS generation circuit, in the case of USB OTG mode operation. The VBUS circuit is powered from the SWBST boost supply, to ensure OTG current sourcing compliance through the normal discharge range of the main battery.

The VUSB regulator can be supplied from the VBUS wire of the USB cable (power rail of the USB cable), when supplied by a host, in the case of host mode operation, or by the SWBST voltage for OTG mode operation. The SWBST voltage supplies the VUSB regulator from the VINUSB pin, which is internally connected to SWBST, and also to the UVBUS pin to drive the VBUS on this mode (as long as VBUSEN pin is logic high =1).

When UVBUS/CHARGRAW is detected in host mode, the USB regulators, VUSB and VUSB2 should be automatically enabled. It will be up to the processor to determine what type of device is connected, either a USB host or a wall charger, and take appropriate action.

The VUSB and VUSB2 regulators can be enabled independent of OTG or Host Mode by setting the individual SPI enable bits, VUSBEN and VUSB2EN respectively.

Since UVBUS can be shared with the charger input at the board level, the UVBUS node must be able to withstand the same high voltages as the charger. In over-voltage conditions, the VUSB regulator is disabled. USB supplies characteristics are shown in Tables 4 and 6.

Note: When VUSBIN =1 , UVBUS will be connected via internal switches to VINUSB and incur some current drain on that pin, as much as 270 μA maximum, so care must be taken to disable this path and set this SPI bit (VUSBIN) to 0 to minimize current drain, even if SWBST and/or VUSB are disabled.

VUSB REGULATOR

VUSB2 is implemented with an integrated PMOS pass FET and has a dedicated supply pin VINUSB2. The pin VINUSB2 should always be connected to BP, even in case the regulators are not used by the application.

The nominal output voltage of this regulator (V_{NOM} as referred in Table 4) can be programmed to be 2.400, 2.600, 2.700, and 2.775 V with a load capability of 50 mA.

GEN1, GEN2 AND GEN3 REGULATORS

General purpose LDOs VGEN1, VGEN2, and VGEN3 are provided for expansion of the power tree, to support peripheral devices which could include WLAN, BT, GPS, or other functional modules. All the regulators include programmable set points for system flexibility. At the 1.2 V and 1.5 V set points, both VGEN1 and VGEN2 can be powered from an external buck switcher (2.2 V typ), for an

efficiency advantage and reduced power dissipation in the pass devices.

VGEN1 nominal output voltage (V_{NOM} as referred in Table 4) can be 1.20, 1.50, 2.7775, or 3.15 V, and has a capability of 200 mA. VGEN2 is configurable for 1.20, 1.50, 1.60, 1.80, 2.70, 2.80, 3.00, and 3.15 V, and can supply up to 350 mA.

VGEN3 has an internal PMOS pass FET, which will support loads up to 50 mA. For higher current capability, drive for an external PNP is provided. The external PNP configuration is offered to avoid excess on-chip power dissipation at high loads and large differential between BP and output settings. The input pin for the integrated PMOS option is shared with the base current drive pin for the PNP option.

This regulator is configurable for nominal output voltages (V_{NOM} as referred in Table 4) of 1.80 and 2.90 V with a capability of 200 mA when working with an external PNP.

GENERAL PURPOSE OUTPUTS

The GPO drivers included can provide useful system level signaling with SPI enabling and programmable Standby control. Key use cases for GPO outputs include battery pack thermistor biasing and enabling of peripheral devices, such as light sensor(s), camera flash, or even supplemental regulators.

SPI enabling can be used for coordinating GPOs with ADC conversions for consumption efficiency and desired settling characteristics.

The GPO1 output is intended to be used for battery thermistor biasing. For accurate thermistor reading by the ADC, the output resistance of the GPO1 driver is of importance.

Finally, a muxing option is included to allow GPO4 to be configured for a muxed connection into Channel 7 of the GP ADC. As an example for a dual light sensor application, Channel 7 can be toggled between the ADIN7 (ADINSEL7=00) and GPO4 (ADINSEL7=11), for convenient connectivity and monitoring of two sensors. The GPO4 pin is configured for ADC input mode by default (GPO4ADIN=1), so that the GPO driver stage is at high impedance at power up. The GPO4 pin can be configured by software for GPO operation with GPO4ADIN=0.

Table 16. 13892 General Purpose Outputs Electrical Characteristics

PIN NAME	PARAMETER	LOAD CONDITION	MIN	MAX	UNIT
GPO1	Output Low	-400 µA	0	0.2	V
	Output High	400 µA	VCORE-0.2	VCORE	V
GPO2, GPO3, GPO4	Output Low	-100 µA	0	0.2	V
	Output High	100 µA	VIOHI-0.2	VIOHI	V

PROTECTION FUNCTIONS

SHORT-CIRCUIT PROTECTION

The higher current LDOs, and those most accessible in product applications, include short-circuit detection and protection (VVIDEO, VAUDIO, VCAM, VSD, VGEN1, VGEN2, and VGEN3). The short-circuit protection (SCP) system includes debounced fault condition detection, regulator shutdown, and processor interrupt generation to contain failures and minimize chance of product damage. If a short-circuit condition is detected, the LDO will be disabled by resetting its VxEN bit while at the same time an interrupt SCPI will be generated to flag the fault to the system processor.

BATTERY MANAGEMENT

The 13892 supports single path and serial path charging. In single path charging, the device is always supplied from the battery and therefore always has to be present and valid. In a serial path charging scheme, the device may operate directly from the charger while the battery is removed or deeply discharged. The charger supports charging from a USB host or a wall charger.

The charger interface provides linear operation via an integrated DAC at programmable current levels. It incorporates a standalone trickle charge mode, in case of a dead battery with dual LED indicator driver. Over-voltage, short-circuit, and under-voltage detectors are included as well as charger detection and removal. The charger includes the necessary circuitry to allow for USB charging and for reverse supply to an external accessory. The battery management system also provides a battery presence detector, and an A to D converter that serves for measuring the charge current, battery and other supply voltages, as well as for measuring the battery thermistor and die temperature. Finally, a system is included for monitoring the current drawn from, or charged into the main battery for support of a Coulomb Counter function.

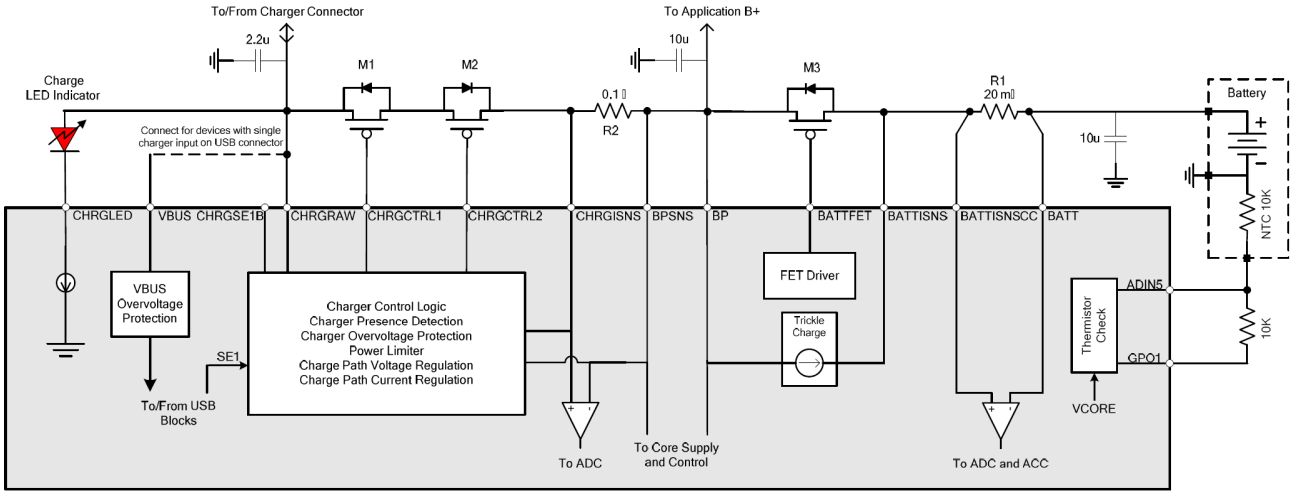


Figure 11. 13892 Charge Path

Transistors M1 and M2 control the charge current and provide voltage regulation. The latter is used as the top off change voltage, and as the regulated supply voltage to the application, in case of dead battery operation. In order to support dead battery operation, a so called “serial path” charging configuration including M3 needs to be used. Then in case of a dead battery, the transistor M3 is made non-conducting and the internal trickle charge current charges the battery. If the battery is sufficiently charged, the transistor M3 is made conducting which connects the battery to the application, just like during normal operation without a charger. In so called single path charging, M3 is replaced by a short and the pin BATTFET must be floating. Dead battery operation is not supported in that case. Transistors M1 and M2 become non-conducting if the charger voltage is too high. The UVBUS pin must be shorted to CHRGRAW in cases where the charger is being supplied from the USB cable. A current can be supplied from the battery to an accessory with all transistors M1, M2, and M3 conducting by enabling the reverse supply mode. An unregulated wall charger configuration can be built, in which case CHRGSE1B must be pulled low. The battery current monitoring resistor R1 and the charge LED indicator are optional.

CHARGE PATH REGULATOR

M1 and M2 are permanently used as a combined pass device for a super regulator, with a programmable output voltage and programmable current limit.

The voltage loop consists of M1, M2, and an amplifier with voltage feedback taken from the BPSNS pin. The value of the sense resistor is of no influence on the output voltage. The output voltage is programmable by SPI from 3.8 to 4.45 V.

The current loop is composed of the M1 and M2 as control elements, the external sense resistor, a programmable current limit, and an amplifier. The control loop will regulate the voltage drop over the external resistor. The charge current is programmable by SPI from 0 to 1600 mA.

INTERNAL TRICKLE CHARGE CURRENT SOURCE

An internal current source between BP and BATTISNS provides small currents to the battery, in case of trickle charging a dead battery.

COMPARATORS

The charger detection is based on three comparators. The “charger valid”, which monitors CHRGRAW, the “charger presence”, which monitors the voltage drop between CHRGRAW and BPSNS, and the “CHGCURR” comparator, which monitors the current through the sense resistor connected between CHRGISNS and BPSNS. A charger insertion is detected, based on the charger presence comparator and the “charger valid” comparator both going high. For all but the lowest current setting, a charger removal is detected, based on both the “charger presence” comparator going low and the charger current falling below CHGCURR. In addition, for the lowest current settings, or if not charging, the “charger valid” comparator going low is an additional cause for charger removal detection.

In addition to the aforementioned comparators, three more comparators play a role in battery charging. These comparators are “BATTMIN”, which monitors BATT for the safe charging battery voltage, “BATTON”, which monitors BATT for the safe operating battery voltage, and “BATTCYCL”, which monitors BPSNS for the constant current to constant voltage transition. The BATTMIN and BATTON comparators have a normal and a long (slow) debounced output. The slow output is used in some places in the charger flow to provide enough time to the battery protection circuit to reconnect the battery cell.

BATTERY THERMISTOR CHECK CIRCUITRY

A battery pack may be equipped with a thermistor, which value decreases over temperature.

By default, the battery thermistor value is taken into account for charging the battery

CHARGE LED INDICATOR

Since normal LED control via the SPI bus is not always possible in the standalone operation, a current sink is provided at the CHRGLED pin. The driver at CHRGLED serves as the trickle (sign of life) LED and will be activated when standalone charging is started, and will remain on also when the device is powered on, until the charger is programmed by SPI.

MODES OF OPERATION

REVERSE SUPPLY MODE

The battery voltage can be applied to an external accessory via the charge path. The path is only established if the normal charge path is disabled. The turn on of M1 and M2 is intentionally slow. The current through the accessory supply path is monitored via the charge path sense resistor R2. It can be read out via the ADC. The accessory supply path is disabled and an interrupt CHGSHORTI is generated when the slow threshold or the fast threshold is crossed. The reverse path is disabled when a current reversal occurs, and an interrupt CHREVI is generated. This function operates up to 40°C.

STANDALONE CHARGING

A standalone charge mode of operation is provided to minimize software interaction. It also allows that a completely discharged battery can be revived without processor control. This is especially important when charging from a USB host or when the optional transistor M3 is not placed.

SOFTWARE CONTROLLED CHARGING

The charger can also be operated under software control. In this mode, full control of the charger settings is assumed by software; the state machine will no longer determine the mode of charging.

FACTORY MODE

In factory mode, power is provided to the application with no battery present. It is not a situation which should occur in the field. The factory mode is differentiated from a USB Host by, in addition to a valid VBUS, a UID being pulled high to VBUS level during the attach, See Connectivity (USB Interface) on page 63.

USB LOW POWER BOOT

USB low power boot allows the application to boot with a dead battery within the 100 mA USB budget, until the processor has negotiated for the full current capability. This mode expedites the charging of the dead battery and allows the software to bring up the LCD display screen with the message “Charging battery”.

PROTECTION FUNCTIONS

OVER-VOLTAGE PROTECTION

In order to protect the application, the voltage at the CHRGRAW pin is monitored. When crossing the threshold (16 V high to low and low to high), the charge path regulator will be turned off by opening the mosfets connected to pins CHRGCTRL1 and CHRGCTRL2. An interrupt CHGFAULTI is generated with the associated CHGFAULTM mask bit. In order to ensure immediate protection, the control of M1, M2, and M3 occurs in real time.

The UVBUS pin is also protected against over-voltages. This will occur at much lower levels then for CHRGRAW. When a VBUS over-voltage is detected the internal circuitry of the USB block is disconnected. An USBOVI is generated in this case.

When the maximum voltage of the IC is exceeded, damage will occur to the IC, and the state of the mosfets connected to pins CHRGCTRL1 and CHRGCTRL2 cannot be guaranteed. If one wants to protect against these failure conditions, additional protection will be required. The same is valid for charger polarity inversion protection.

OVER-POWER DISSIPATION PROTECTION

Since the charge path operates in a linear fashion, the dissipation can be significant and care must be taken to ensure that the external pass FETs M1 and M2 are not over dissipating when charging. By default, the charge system will protect against this by a built in power limitation circuit.This circuit will monitor the voltage drop between CHRGRAW and CHRGISNS, and the current through the external sense resistor connected between CHRGISNS and BPSNS. When required, a duty cycle is applied to the FETs connected on CHRGCTRL1 and CHRGCTRL2, and thus the charge current, in order to stay within the power budget. At the same time the FET connected to BATTFET pin is forced to conduct to keep the application powered. In case of excessive supply conditions, the power limiter minimum duty cycle may not be sufficiently small to maintain the actual power dissipation within budget. In that case, the charge path will be disabled and the CHGFAULTI interrupt generated.

The power budget can be programmed by the SPI through the PLIM[1:0] bits, which establishes a power limit from 600 to 1200 mW in 200 mV steps. The power dissipation limiter can be disabled by setting the PLIMDIS bit. In this case, it is advised to use close software control to estimate the dissipated power in the external pass FETs. The power limiter is automatically disabled in serial path factory mode and in reverse mode.

Since a charger attachment can be a Turn On event when a product is initially in the Off state, any nondefault settings that are intended for PLIM[1:0] and PLIMDIS should be programmed early in the configuration sequence to ensure proper supply conditions adapted to the application. To avoid any false detection during power up, the power limiter output is blanked at the start of the charge cycle. As a safety

precaution, the power dissipation is monitored and the desired duty cycle is estimated. When this estimated duty cycle falls below the power limiter minimum duty cycle, the charger circuit will be disabled.

ADC SUBSYSTEM

The ADC core is a 10 bit converter. The ADC core and logic run on 2/3 of the switcher PLL generated frequency, so approximately 2.0 MHz. If an ADC conversion is requested while the PLL is not active, it will be automatically enabled by the ADC. A 32.768 kHz equivalent time base is derived from the 2.0 MHz clock to time ADC events. The ADC is supplied from VCORE. The ADC core has an integrated auto calibration circuit which reduces the offset and gain errors.

The switcher PLL is programmable, so when the switcher frequency is changed, the frequency applied to the ADC converter will change accordingly. Although the conversion time is inversely proportional to the PLLX[2:0] setting, this will not influence the ADC performance. The locally derived 32.768 kHz will remain constant in order to not influence the different timings depending on this time base.

The ADC Subsystem has 8 channels:

Channel 0 Battery Voltage:

The battery voltage is read at the BATT pin at channel 0.

Channel 1 Battery Current:

The current flowing out of and into the battery can be read via the ADC by monitoring the voltage drop over the sense resistor between BATT and BATTISNSCC.

Channel 2 Application Supply:

The application supply voltage is read at the BP pin at channel 2.

Channel 3 Charger Voltage:

The charger voltage is measured at the CHRGRAW pin at channel 3.

Channel 4 Charger Current:

The charge current is read by monitoring the voltage drop over the charge current sense resistor. This resistor is connected between CHRGISNS and BPSNS.

Channel 5 ADIN5, Battery Thermistor and Battery Detect:

On channel 5, ADIN5 may be used as a general purpose input, but in a typical application, ADIN5 is used to read out the battery pack thermistor. The thermistor will have to be biased with an external pull-up to a voltage rail greater than the ADC input range. In order to save current when the thermistor reading is not required, it can be biased from one of the general purpose IOs such as GPO1. A resistor divider network should assure the resulting voltage falls within the ADC input range, especially when the thermistor check function is used.

When the application is on and supplied by the charger, a battery removal can be detected by a battery thermistor presence check. When the thermistor terminal becomes high-impedance, the battery is considered being removed. This detection function is available at the ADIN5 input.

Channel 6 ADIN6 and Coin Cell Voltage:

On channel 6, ADIN6 may be used as a general purpose unscaled input but in a typical application, the PA thermistor is connected here. In addition, on channel 6, the voltage of the coin cell connected to the LICELL pin can be read.

Channel 7 ADIN7 and ADIN7B, UID and Die Temperature:

On channel 7, ADIN7 may be used as a general purpose input. In a typical application, an ambient light sensor is connected here. A second general purpose input ADIN7B is available. In the application, a second ambient light sensor is supposed to be connected here.

In addition, on channel 7, the voltage of the USB ID line connected to the UID pin and the die temperature can be read.

COULOMB COUNTER

As discussed previously, the current into and from the battery can be read out through the general purpose ADC as a voltage drop over the R1 sense resistor. Together with the battery voltage reading the battery capacity can be estimated. A more accurate battery capacity estimation can be obtained by using the integrated Coulomb Counter.

The Coulomb Counter (or CC) monitors the current flowing in/out of the battery by integrating the voltage drop across the battery current sense resistor R1, followed by an A to D conversion. The result of the A to D conversion is used to increase/decrease the contents of a counter that can be read out by software.

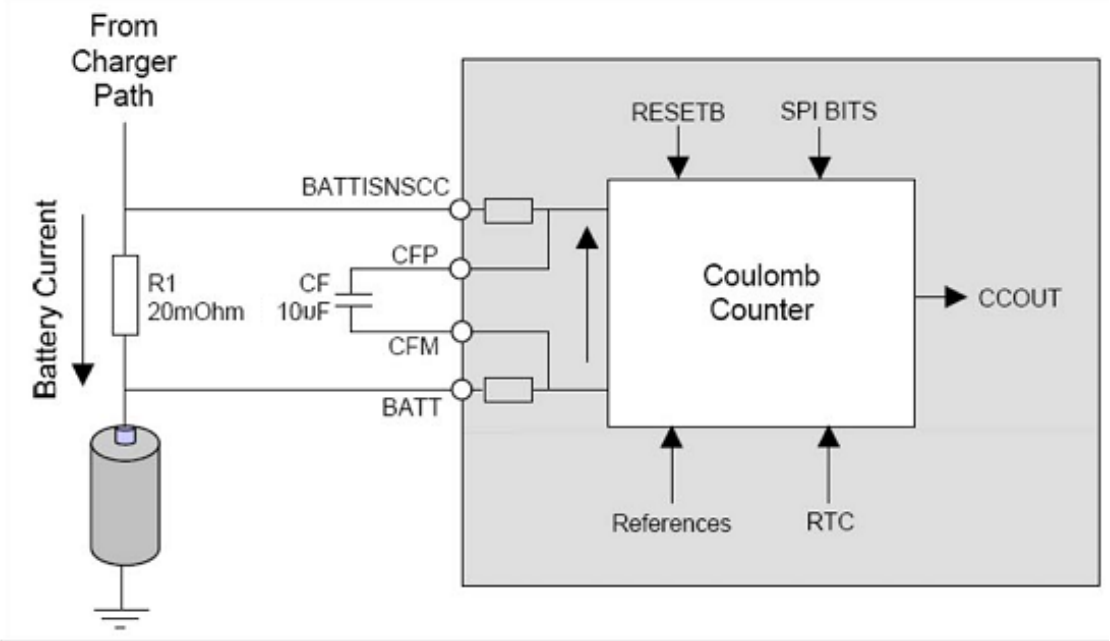


Figure 12. 13892 Coulomb Counter Block Diagram.

PROTECTIONS AGAINST FAULT CONDITIONS

Counter roll over: CCOUT[15:0]=8000HEX

This occurs when the contents of CCOUT[15:0] go from a negative to a positive value or vice versa. Software may interpret incorrectly the battery charge by this change in polarity. When CCOUT[15:0] becomes equal to 8000HEX the CCFAULT is set. The counter stays counting so its contents can still be exploited.

Battery removal: 'BP<UVDET'

When removing and replacing the battery, the contents of the counter are no longer valid. A battery removal is characterized by the input supply to the IC dropping below the under-voltage detect threshold, so BP<UVDET. To avoid false detection due to short power cuts, the CCFAULT is set only after a long debounce of 1.0 second.

Battery removal when charging: BATTDETBS=1

The battery removal detection as described previously is not applicable when charging, since in this case, the charger will continue to supply the application and the BP will not drop below UVDET. To still detect a battery removal, one can use the battery detect function, as described in ADC Subsystem on page 61. When the sense bit BATTDETBS becomes a 1, the CCFAULT is set only after a long debounce of 1.0 second.

Touch Screen Interface

The touch screen interface provides all circuitry required for the readout of a 4-wire resistive touch screen. The touch screen X plate is connected to TSX1 and TSX2, while the Y plate is connected to TSY1 and TSY2. A local supply TSREF will serve as a reference. Several readout possibilities are offered.

To perform touch screen readings, the processor will have to select the touch screen mode, program the delay between the conversions via the ATO and ATOX settings, trigger the ADC via one of the trigger sources, wait for an interrupt indicating the conversion is done, and then read out the data. In order to reduce the interrupt rate and to allow for easier noise rejection, the touch screen readings are repeated in the readout sequence. The reference for the touch screen is TSREF and is powered from VCORE. In touch screen operation, TSREF is a dedicated regulator that is to say, no other loads than the touch screen should be connected here.

Table 17. 13892 Touch Screen ADC Readings

ADC CONVERSION	SIGNALS SAMPLED
0	X position
1	X position
2	Dummy
3	Y position
4	Y position
5	Dummy
6	Contact resistance
7	Contact resistance

The dummy conversion inserted between the different readings is to allow the references in the system to be pre-biased for the change in touch screen plate polarity and will read out as ‘0’.

MODES OF OPERATION

In inactive mode, the inputs TSX1, TSX2, TSY1, and TSY2 can be used as general purpose inputs. They are respectively mapped on ADC channels 4, 5, 6, and 7.

In interrupt mode, a voltage is applied to the X-plate (TSX2) via a weak current source to VCORE, while the Y-plate is connected to ground (TSY1). When the two plates make contact both will be at a low potential. This will generate a pen interrupt TSI to the processor. This detection does not make use of the ADC core or the TSREF regulator, so both can remain disabled.

In touch screen mode, the XY coordinate pairs and the contact resistance are read. The X-coordinate is determined by applying TSREF over the TSX1 and TSX2 pins while performing a high-impedance reading on the Y-plate through TSY1. The Y-coordinate is determined by applying TSREF between TSY1 and TSY2 while reading the TSX1 pin. The contact resistance is measured by applying a known current into the TSY1 terminal of the touch screen and through the terminal TSX2, which is grounded. The voltage difference between the two remaining terminals TSY2 and TSX1 is measured by the ADC, and equals the voltage across the contact resistance. Measuring the contact resistance helps in determining if the touch screen is touched with a finger or stylus.

LED DRIVERS FOR LIGHTING SYSTEM

BACKLIGHT LED DRIVERS

The lighting system includes backlight drivers for main display, auxiliary display, and keypad. The backlight LEDs are configured in series and supplied from an inductive boost supply See Boost Converters on page 53. Three additional drivers are provided for RGB or general purpose signaling.

Ramp up and ramp down patterns are implemented in hardware to reduce the burden of real time software control via the SPI, to orchestrate dimming and soft start lighting effects. These patterns are guaranteed by design.

The current level is programmable in a low range mode and in a high range mode from 0 to 21 mA and from 0 to 42 mA respectively. This facilitates the current setting, in case two or more serial LED strings are connected in parallel to the same driver, or when using super bright LEDs.

The boost switcher SWLED supplying the backlight LEDs is shared between all three backlight drivers. However, a maximum of only two backlight drivers can be activated at the same time, for instance the main display plus keypad. If all three backlight drivers are enabled meaning none of the duty cycles equals 0/32, then none of the drivers will be activated.

SIGNALING LED DRIVERS

The signaling LED drivers LEDR, LEDG, and LEDB are independent current sink channels. Each driver channel features programmable current levels from 0 to 21 mA as well as programmable PWM duty cycle settings. By a combination of level and PWM settings, each channel provides flexible LED intensity control. By driving LEDs of different colors, color mixing can be achieved.

Blue LEDs or bright green LEDs require more headroom than red and normal green signal LEDs. In the application, a 5.0 V or equivalent supply rail is therefore required. This is provided by the integrated boost converter SWBST. As with the backlight driver channels, the signaling LED drivers include ramp up and ramp down patterns are implemented in hardware.

In addition, programmable blink rates are provided. Blinking is obtained by lowering the PWM repetition rate of each of the drivers, while the on period is determined by the duty cycle setting. To avoid high frequency spur coupling in the application, the switching edges of the output drivers are softened."

CONNECTIVITY (USB INTERFACE)

The 13892 contains the regulators required to supply the PHY contained in the i.MX51, i.MX37, i.MX35, and i.MX27 processors. The regulators used to power the external PHY in the i.MX51 and i.MX37 are VUSB, VUSB2, and VUSB for the i.MX35 and i.MX27 processors. The IC also provides the 5.0 V supply for USB OTG operation. The USB interface may be used for portable product battery charging. Finally included are comparators/detectors for VBUS and ID detection. VBUS is the power rail of the USB cable that must be connected to the UVBUS pin.

The USB interface is illustrated in Figure 13.

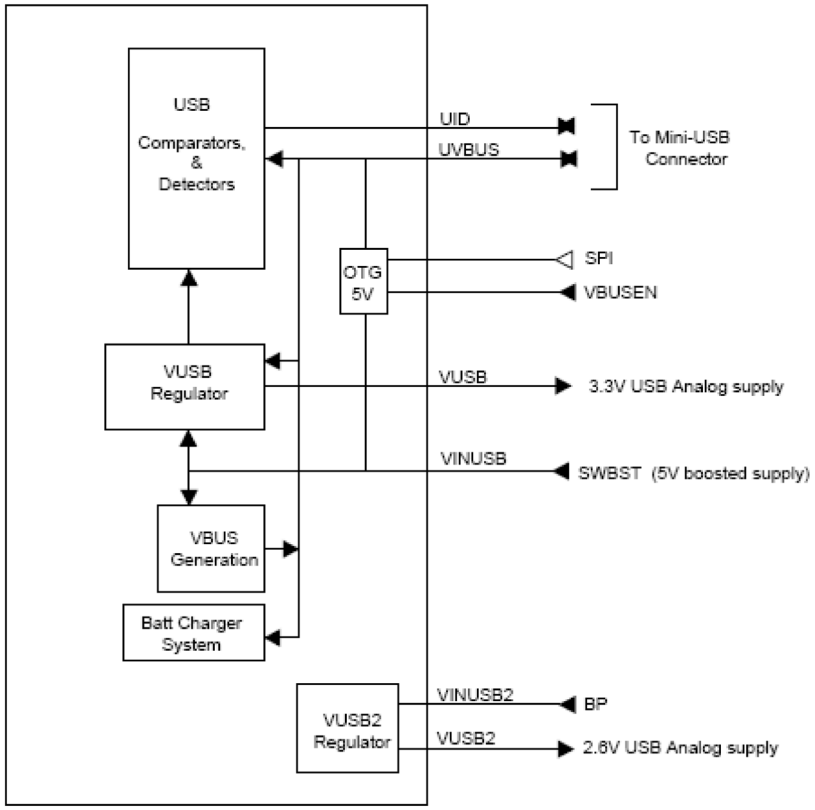


Figure 13. 13892 USB Interface Block Diagram

OTG MODE (ON THE GO)

The ID detector is primarily used to determine if a mini-A or mini-B style plug has been inserted into a mini-AB style receptacle on the application. However, it also supports two additional modes which are outside of the USB standards: a factory mode, and a non-USB accessory mode. The state of the ID detection can be read via the SPI to poll dedicated sense bits for a floating, grounded, or factory mode condition on the UID pin. There are also dedicated maskable interrupts for each UID condition as well.

Since portable applications have limited capabilities, this supplement to the USB2.0 specification was developed in order to allow a portable device to take the role of a USB host. In this mode of operation, SWBST is internally switched to supply the VUSB regulator, and SWBST will drive VBUS from the VUSBIN pin as long as VBUSEN pin is a logic high = 1.

According to the USB2.0 specification, the USB host is the device where the USB Host Controller is installed, through which it interacts with the USB devices. The USB host is responsible for:

- Detecting the attachment and removal of USB devices.
- Managing control flow between the host and USB devices.
- Managing data flow between the host and USB devices.
- Collecting status and activity statistics.
- Providing power to attached USB devices.

When working in host mode, VUSB is supplied from the VBUS wire of the USB cable (VBUS).

Parameter	Condition	Min	Typ	Max	Units
VBUS input impedance	As A_device	40		100	KΩ
UID 220K Pull-up[57]	IDPUCNTRL=0, Resistor to VCORE	132	220	308	KΩ
UID Pull-up[57]	IDPUCNTRL=1, Current source from VCORE	4.75	5	5.25	uA
UID Parallel Pull-up[57]	ID100KPU=1, Resistor to VCORE	60	100	140	KΩ

Notes

57. Note that the UID Pull-ups are not mutually exclusive of each other, they are independently controlled by their enable bits and thus multiple pull-ups can be engaged simultaneously.

POWER CONTROL LOGIC (STATE MACHINE)

The power control system interfaces with the processor via different IO signals and the SPI bus. It also uses on chip signals and detector outputs.

Figure 14 shows the flow of the power control state machine. This diagram serves as the basis for the description of Operational Modes.

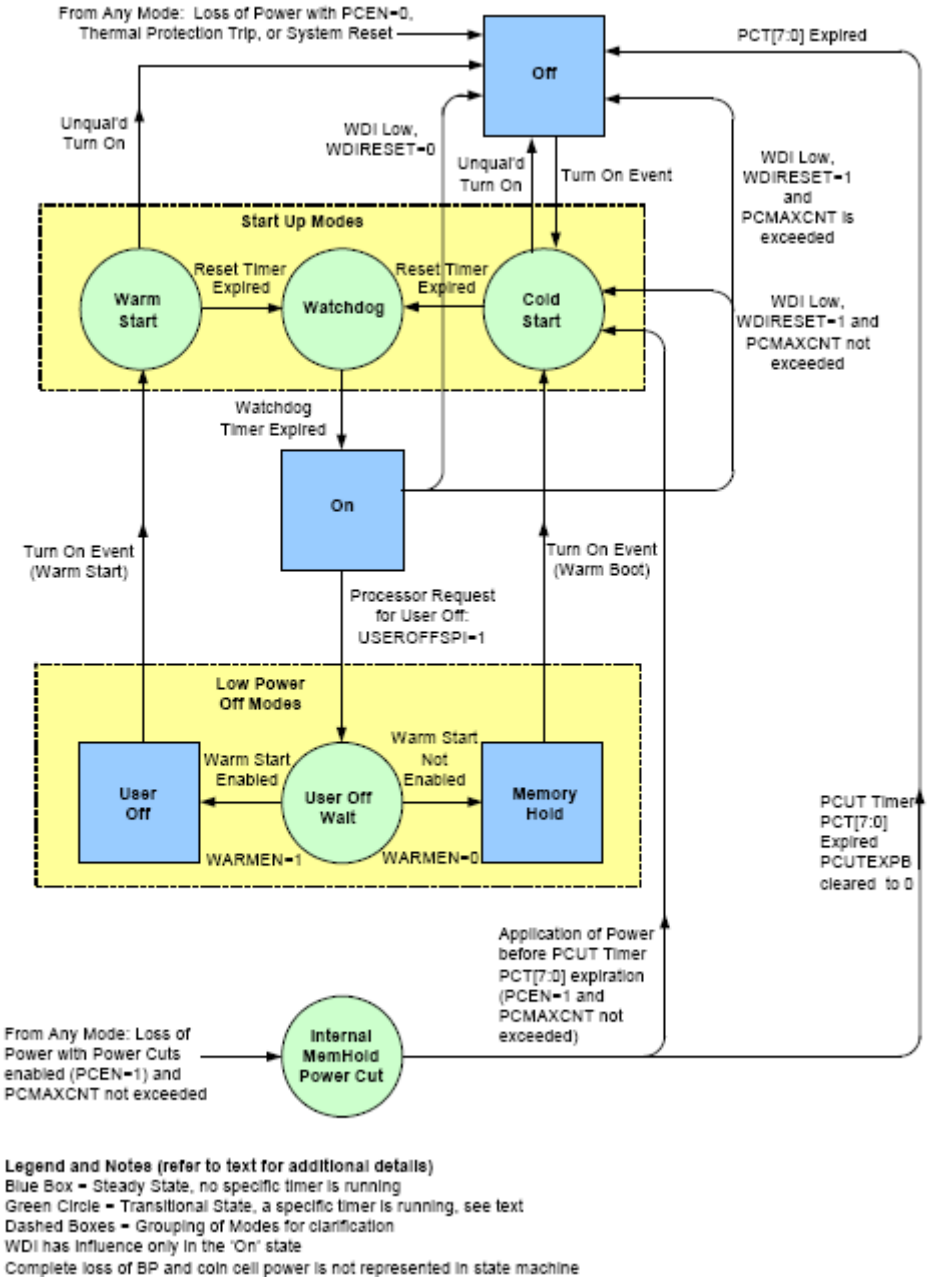


Figure 14. Power Control Logic (State Machine)

OPERATIONAL MODES

The following are text descriptions of the power states of the system with additional details of the state machine to complement Figure 14. Note that SPI control is only possible in the Watchdog, On, and User Off Wait states, and that the interrupt line INT is kept low in all states except for Watchdog and On.

OFF

If the supply at BP is above the UVDET threshold, only the IC core circuitry at VCOREDIG and the RTC module are powered. All other supplies are inactive. To exit the Off mode, a valid turn on event is required. No specific timer is running in this mode.

If the supply at BP is below the UVDET threshold, no turn on events are accepted. If a valid coincell is present, the core gets its power from LICELL. The only active circuitry is the RTC module, and the BP greater than UVDET detection.

COLD START

This is entered upon a Turn On event from Off, Warm Boot, successful PCUT, or Silent System Restart. The first 8.0 ms are used for initialization which includes bias generation, PUMS / configuration latching, and qualification of the input supply level BP. The switchers and regulators are then powered up sequentially to limit the inrush current. The reset signals RESETB and RESETBMCU are kept low. The Reset timer starts running when entering Cold Start. The input control pins WDI and STANDBYx are ignored.

WATCHDOG

The system is fully powered and under SPI control. RESETB and RESETBMCU are high. The Watchdog timer starts running when entering the Watchdog state. When expired, the system transitions to the On state, where WDI will be checked and monitored. The input control pins WDI and STANDBYx are ignored while in the Watchdog state.

ON

The system is fully powered and under SPI control. RESETB and RESETBMCU are high. The WDI pin must be high to stay in this mode.

USER OFF WAIT

The system is fully powered and under SPI control. The WDI pin no longer has control over the part. The Wait mode is entered by a processor request for User Off. The Wait timer starts running when entering User Off Wait mode. This leaves the processor time to suspend or terminate its tasks.

MEMORY HOLD AND USER OFF (LOW POWER OFF STATES)

As noted in the User Off Wait description, the system is directed into low power Off states, based on a SPI command in response to an intentional Turn Off by the end user. The only exit then will be a Turn On event.

To an end user, the Memory Hold and User Off states look like the product has been shut down completely. However, a faster startup is facilitated by maintaining external memory in self-refresh mode (Memory Hold and User Off mode), as well as powering portions of the processor core for state retention (User Off only).

MEMORY HOLD

RESETB and RESETBMCU are low, and both CLK32K and CLK32KMCU are disabled (CLK32KMCU active if DRM is set).

Upon a Turn On event, the Cold Start state is entered, the default power up values are loaded, and the MEMHLDI interrupt bit is set. A Cold Start out of the Memory Hold state will result in shorter boot times compared to starting out of the Off state, since software does not have to be loaded and expanded from flash. The startup out of Memory Hold is also referred to as Warm Boot. No specific timer is running in this mode.

USER OFF

RESETB is low and RESETBMCU is kept high. The 32 kHz peripheral clock driver CLK32K is disabled; CLK32KMCU (connected to the processor's CKIL input) is maintained in this mode, if the CLK32KMCUEN and USEROFFCLK bits are both set, or if DRM is set.

Any peripheral loading on SW1 and/or SW2 should be isolated from the output node(s) by the PWGT1 switch, which opens in both low power Off modes, due to the RESETB transition. In this way, leakage is minimized from the power domain, maintaining the processor core.

Since power is maintained for the core (which is put into its lowest power state), and since MCU RESETBMCU does not trip, the processor's state may be quickly recovered when exiting USEROFF upon a Turn On event. The CLK32KMCU clock can be used for very low frequency / low power idling of the core(s), minimizing battery drain while allowing a rapid recovery from where the system left off before the USEROFF command.

Upon a Turn On event, Warm Start state is entered, and the default power up values are loaded. A Warm Start out of User Off will result in an almost instantaneous startup of the system, since the internal states of the processor were preserved along with external memory. No specific timer is running in this mode.

WARM START

Entered with a Turn On event from User Off. The first 8.0 ms is used for initialization which includes bias generation, PUMS latching, and qualification of the input

supply level BP. The switches and regulators are then powered up sequentially to limit the inrush current.

$\overline{\text{RESETB}}$ is kept low and $\overline{\text{RESETBMCU}}$ is kept high. CLK32KMCU is kept active if CLK32KMCU was set. The reset timer starts running when entering Warm Start. When expired, the Warm Start state is exited for the Watchdog state, a WARMI interrupt is generated, and $\overline{\text{RESETB}}$ will go high.

INTERNAL MEMHOLD POWER CUT

Power Cut description: When the supply at BP drops below the UVDET threshold due to battery bounce or battery removal, the Internal MemHold Power Cut mode is entered and a Power Cut (PCUT) timer starts running. The backup coin cell will now supply the RTC as well as the on chip memory registers and some other power control related bits. All other supplies will be disabled.

Internal MemHold Power Cut: As previously described, a momentary power interruption will put the system into the Internal MemHold Power Cut state if PCUTs are enabled. The backup coin cell will now supply 13892's core along with the 32 k crystal oscillator, the RTC system and coin cell backed up registers. All regulators and switchers will be shut down to preserve the coin cell and RTC as long as possible.

Both $\overline{\text{RESETB}}$ and $\overline{\text{RESETBMCU}}$ are tripped, bringing the entire system down along with the supplies and external clock drivers, so the only recovery out of a Power Cut state is to reestablish power and initiate a Cold Start.

POWER SAVING

SYSTEM STANDBY

A product may be designed to go into DSM after periods of inactivity, such as if a music player completes a play list and no further activity is detected, or if a gaming interface sits idle for an extended period. Two Standby pins are provided for board level control of timing in and out of such deep sleep modes.

When a product is in DSM it may be able to reduce the overall platform current by lowering the switcher output voltage, disabling some regulators, or forcing GPOx low. This can be obtained by SPI configuration of the Standby response of the circuits along with control of the Standby pins.

To ensure that shared resources are properly powered when required, the system will only be allowed into Standby when both the application processor (which typically controls the STANDBY pin) and peripherals (which typically control the STANDBYSEC pin) allow it—this is referred to as a Standby event.

REGULATOR MODE CONTROL

The regulators with embedded pass devices (VDIG, VPLL, VIOHI, VUSB, VUSB2, and VAUDIO) operate in two modes: a normal mode, and a low power mode. The transition between both modes occurs automatically, based on the load current. Therefore, no specific control is required to put these regulators in a low power mode (i.e., "On" implies an adaptive mode control" based on load current). Bits are reserved in case the automatic scheme shows to be insufficient.

The regulators with external pass devices (VSD, VVIDEO, VGEN1, and VGEN2) can also operate in a normal and low power mode. However, since a load current detection cannot be performed for these regulators, the transition between both modes is not automatic, and is controlled by setting the corresponding mode bits for the operational behavior desired.

The regulators VGEN3, and VCAM can be configured for using the internal pass device or external pass device as explained in LDOs on page 54. Therefore, depending on the configuration selected, the automatic low power mode is or is not available.

BUCK SWITCHERS

Operational modes of the Buck switchers can be controlled by direct SPI programming, altered by the state of the STANDBY pins, by direct state machine influence (i.e., entering Off or low power Off states, for example), or by load current magnitude when so configured. Available modes include PWM with No Pulse Skipping (PWM), PWM with Pulse Skipping (PWMPS), Pulse Frequency Mode (PFM), and Off. The transition between the two modes PWMPS and PFM can occur automatically based on the load current (auto). Therefore, no specific control is required to put the switchers in a low power mode. When the buck switchers are not configured in the auto mode, power savings may be achieved by disabling the switchers when not needed, or running them in PFM mode, if loading conditions are light enough.

SW1, SW2, SW3, and SW4 can be configured for mode switching with STANDBY or autonomously, based on load current with adaptive mode control (Auto). Additionally, provisions are made for maintaining PFM operation in USEROFF and MEMHOLD modes, to support state retention for faster startup from the low power Off modes, for Warm Start or Warm Boot.

POWER GATING SYSTEM

The low power Off states are provided to allow faster system booting from two pseudo Off conditions: Memory Hold, which keeps external memory powered for self refresh, and User Off, which keeps the processor powered up for state retention. For reduced current drain in low power Off states, parts of the system can benefit from power gating, to isolate the minimum essentials for such operational modes. It is also necessary to ensure that the power budget on backed up domains is within the capabilities of switchers in PFM mode. An additional benefit of power gating peripheral loads during system startup is to enable the processor core to complete booting and begin running software before additional supplies or peripheral devices are powered. This allows system software to bring up the additional supplies and close power gating switches in the most optimum order

to avoid problems with supply sequencing or transient current surges. The power gating switch drivers and integrated control are included for optimizing the system power tree.

The power gate drivers could be used for other general power gating as well. The text herein assumes the standard application of PWGT1 for core supply power gating and PWGT2 for Memory Hold power gating.

USER OFF POWER GATING

User Off configuration maintains PFM mode switchers on both the processor and external memory power domains. PWGTDRV1 is provided for power gating peripheral loads sharing the processor core supply domain(s) SW1, and/or SW2, and/or SW3. In addition, PWGTDRV2 provides support to power gate peripheral loads on the SW4 supply domain.

In a typical application, SW1, SW2, and SW3 will be kept active for the processor modules in state retention, and SW4 will be retained for the external memory in self refresh mode. SW1, SW2, and SW3 power gating FETs drive would typically be connected to PWGTDRV1 (for parallel NMOS switches). The SW4 power gating FET drive would typically be connected to PWGTDRV2. When low power Off mode is activated, the power gate drive circuitry will be disabled, turning off the NMOS power gate switches, to isolate the maintained supply domains from any peripheral loading.

MEMORY HOLD POWER GATING

As with the User Off power gating strategy described previously, Memory Hold power gating is intended to allow isolation of the SW4 power domain to selected circuitry in low power modes, while cutting off the switcher domain from other peripheral loads. The only difference is that processor supplies SW1, and/or SW2, and/or SW3 are shut down in Memory Hold, so just the external memory is maintained in self-refresh mode.

An external NMOS is to be placed between the direct-connected memory supply and any peripheral loading. The PWGTDRV2 pin controls the gate of the external NMOS, and is normally pulled up to a charge pumped voltage (~5.0 V). During Memory Hold or User Off, PWGTDRV2 will go low to turn off the NMOS switch and isolate memory on the SW4 power domain.

POWER DISSIPATION

During operation, the temperature of the die should not exceed the maximum junction temperature. Depending on the operating ambient temperature and the total internal dissipation, this limit can be exceeded. To optimize the thermal management scheme and avoid overheating, the 13892 provides a thermal management system. The thermal protection is based on a circuit with a voltage output that is proportional to the absolute temperature. This voltage can be read out via the ADC for precise temperature readouts (See Functional Device Operation).

THERMAL PROTECTION

Thermal protection is integrated to power off the 13892 and disable the charger circuitry in case of over dissipation. This thermal protection will act above the maximum junction temperature to avoid any unwanted power downs. The protection is debounced by one period of the 32kHz clock in order to suppress any (thermal) noise. This protection should be considered as a fail-safe mechanism and therefore the application design should be dimensioned such that this protection is not tripped under normal conditions. The temperature thresholds are listed in the last section of Table 4.

TYPICAL APPLICATIONS

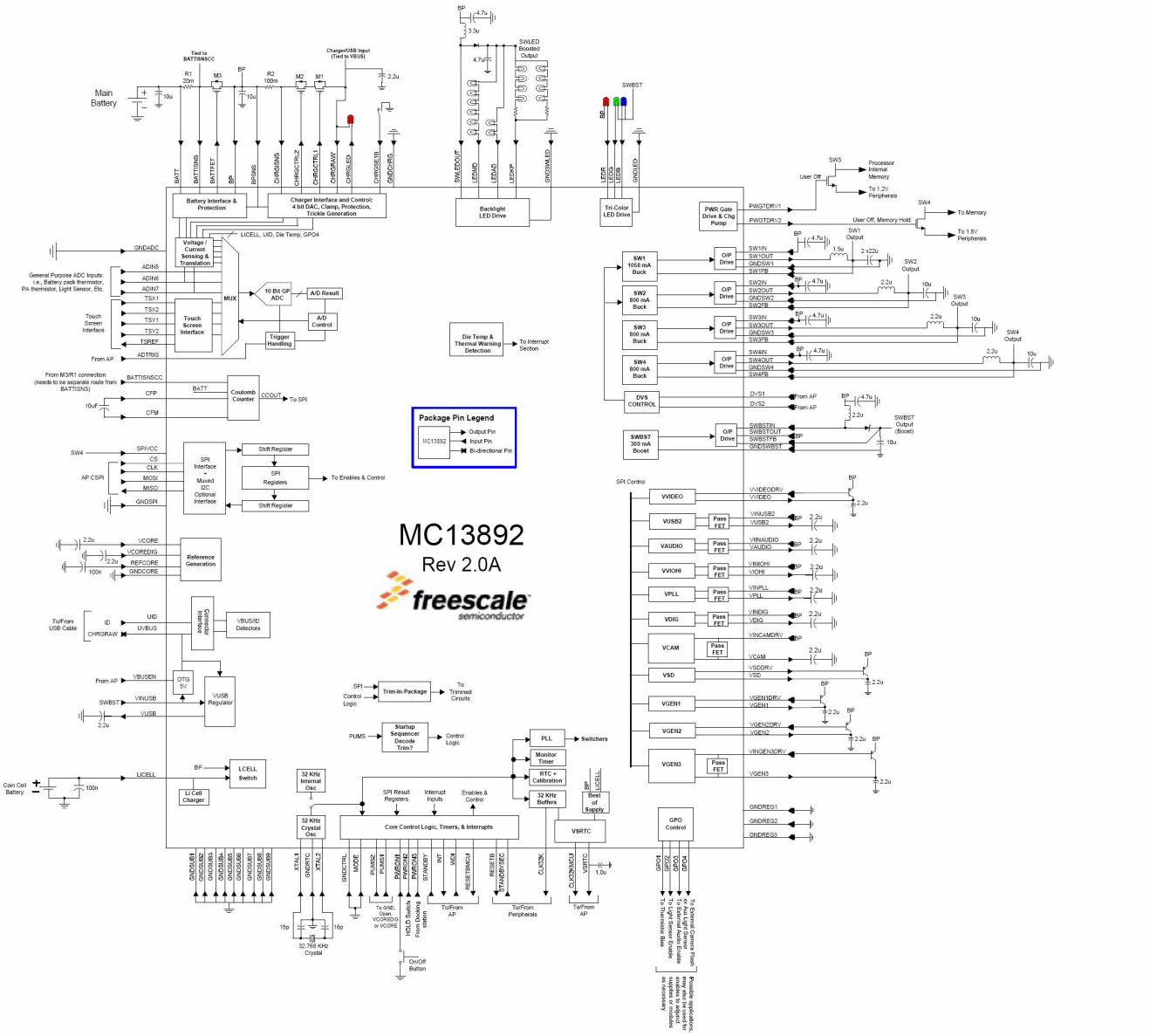
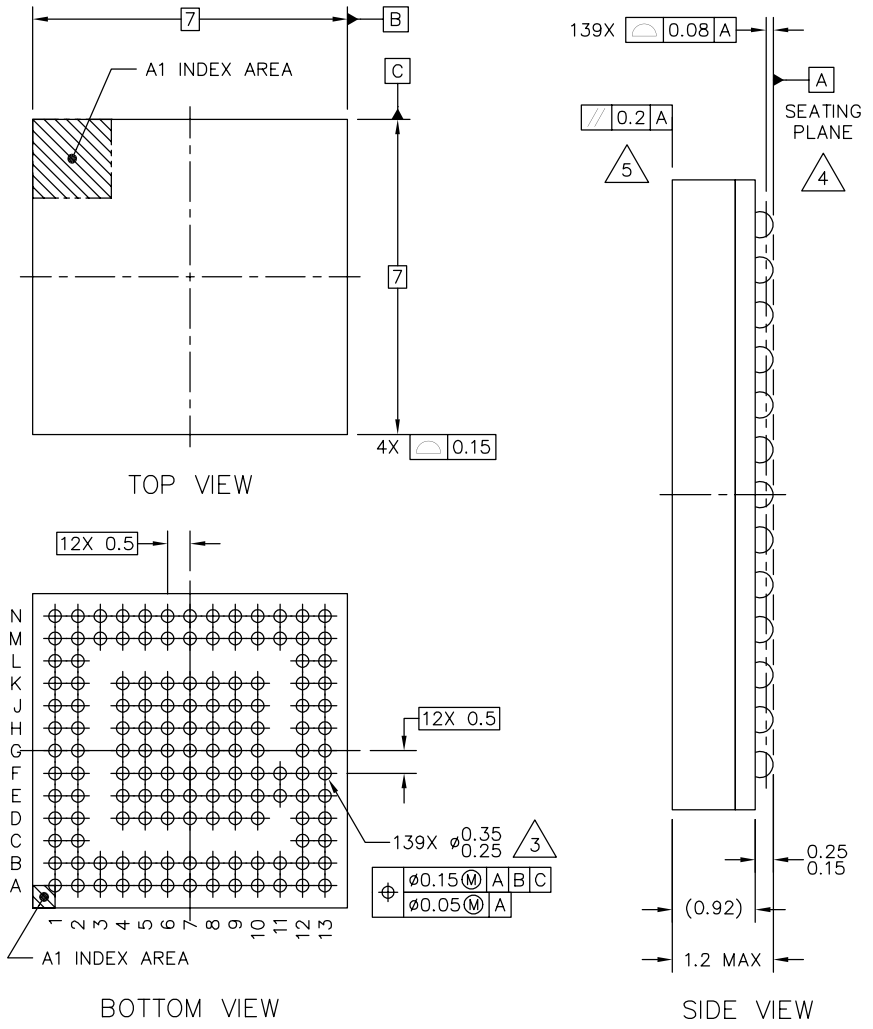


Figure 15. 13892 Typical Application

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the "98A" listed below.



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	STANDARD: MO–195–AD	

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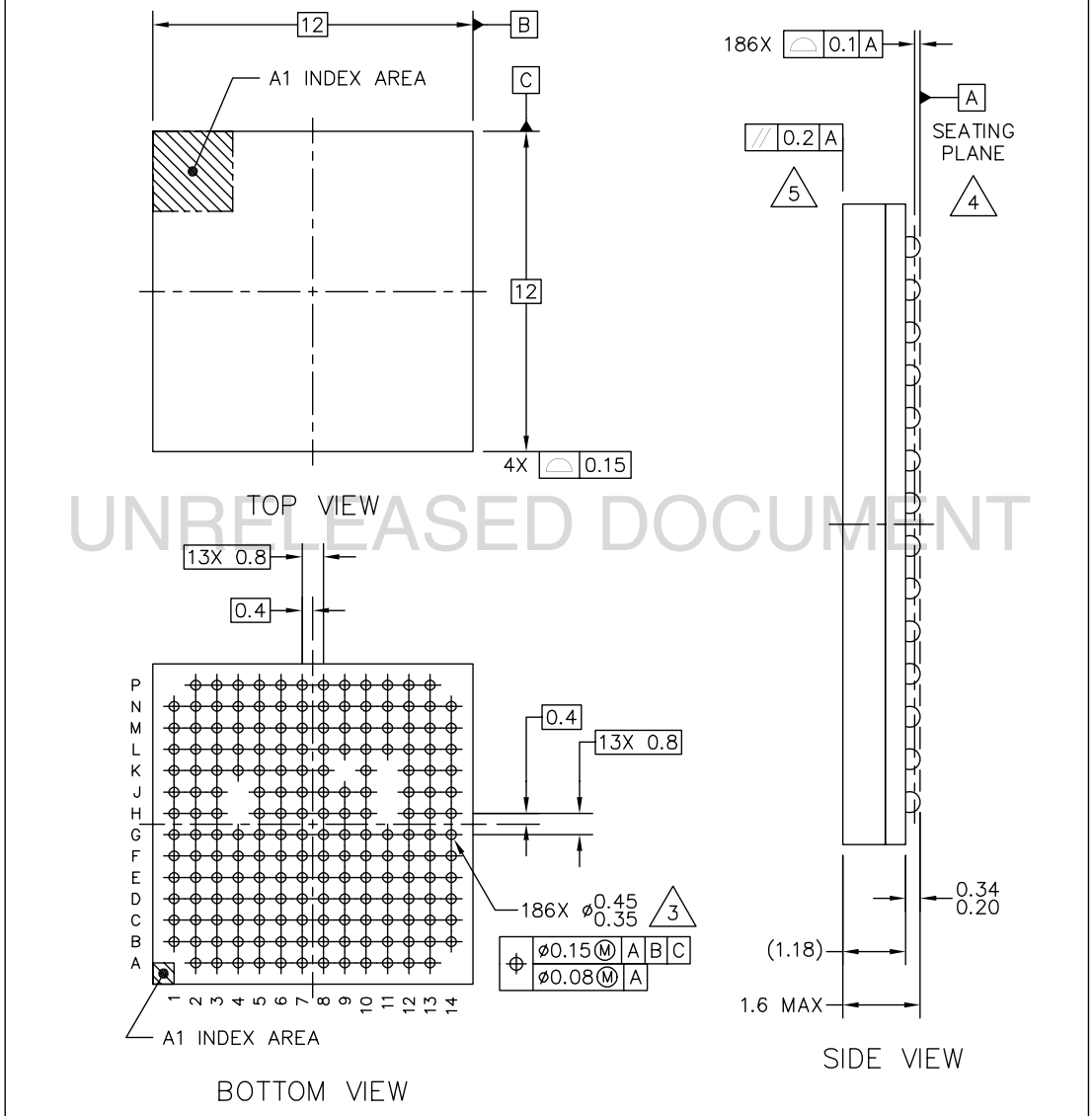

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	10/2009	• Initial release
2.0	10/2009	• Updated Status to Advance Information.

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MC13892VK and MC13892VL in 139, 186 MAPBGA packages.

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