迪一電子®

# 15N10

## 100V N-Channel Power MOSFET

### Features

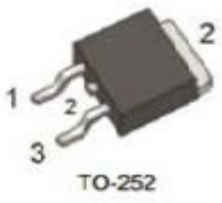
- $R_{DS(ON)}$<110mΩ @ $V_{GS}$=10V
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Lead free in compliance with EU RoHS directive.
- Green molding compound

### PRODUCT SUMMARY

| $V_{DS}$ (V) | $R_{DS(on)}$(mΩ) | $I_D$ (A) |
|---|---|---|
| 100 | 110@ $V_{GS}$ =10V | 15 |

### Mechanical Data

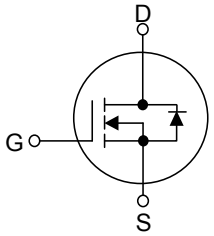
- Case: TO-252




Pin Definition:

1. Gate
2. Drain
3. Source

**Block Diagram**




## Ordering Information

| Part No. | Package | Packing |
|---|---|---|
| DMD15N10-TR | TO-252 | 2.5Kpcs / 13" Reel |
| DMD15N10-TU | TO-252 | 75pcs / Tube |

### ABSOLUTE MAXIMUM RATINGS ($T_C$=25°C, unless otherwise specified)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Continuous Drain Current[1] | $I_D$ @Tc=25℃ | 15.0 | A |
| Continuous Drain Current[1] | $I_D$ @Tc=70℃ | 13.8 | A |
| Pulsed Drain Current[2] | $I_{DM}$ | 24 | A |
| Total Power Dissipation[4] | $P_D$ @Tc=25℃ | 34.7 | W |
| Total Power Dissipation | $P_D$ @TA=25℃ | 2 | W |
| Single Pulse Avalanche Energy[3] | EAS | 8 | mJ |
| Avalanche Current | $I_{AS}$ | 11 | A |
| Operating Junction and Storage Temperature Range | Tj, Tstg | -55 ~ +150 | ℃ |

### THERMAL DATA

| Parameter | Symbol | Max. Value | Unit |
|---|---|---|---|
| Thermal Resistance Junction-ambient[1] | $R_{\theta JA}$ | 62.5 | ℃/W |
| Thermal Resistance Junction-case[1] | $R_{\theta JC}$ | 3.6 | ℃/W |

**ELECTRICAL CHARACTERISTICS** (Tj = 25℃ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 100 | - | - | V | $V_{GS}$=0, $I_D$=250uA |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1.0 | - | 2.5 | V | $V_{DS}$= $V_{GS}$ , $I_D$=250uA |
| Gate-Source Leakage Current | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$= ±20V |
| Drain-Source Leakage Current | $I_{DSS}$ | - | - | 1.0 | uA | $V_{DS}$=80V, $V_{GS}$=0 |
| Static Drain-Source On-Resistance[2] | $R_{DS(ON)}$ | - | - | 110 | mΩ | $V_{GS}$=10V, $I_D$=8A |
| | | - | - | 120 | | $V_{GS}$=4.5V, $I_D$=8A |
| Total Gate Charge[2] | $Q_g$ | | 26.2 | | nC | $I_D$=10A<br>$V_{DS}$=80V<br>$V_{GS}$=10V |
| Gate-Source Charge | $Q_{gs}$ | | 4.6 | | | |
| Gate-Drain (“Miller”) Change | $Q_{gd}$ | | 5.1 | | | |
| Turn-on Delay Time[2] | $T_{d(on)}$ | - | 4.2 | - | ns | $V_{DS}$=50V<br>$I_D$=10A<br>$V_{GS}$=10V<br>$R_G$=3.3Ω |
| Rise Time | $T_r$ | - | 8.2 | - | | |
| Turn-off Delay Time | $T_{d(off)}$ | - | 35.6 | - | | |
| Fall Time | $T_f$ | - | 9.6 | - | | |
| Input Capacitance | $C_{iss}$ | - | 1535 | - | pF | $V_{GS}$=0V<br>$V_{DS}$=15V<br>f=1.0MHz |
| Output Capacitance | $C_{oss}$ | - | 60 | - | | |
| Reverse Transfer Capacitance | $C_{rss}$ | - | 37 | - | | |
| Gate Resistance | $R_g$ | - | 2 | - | Ω | f=1.0MHz |

## Guaranteed Avalanche Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Single Pulse Avalanche Energy[5] | EAS | 1.25 | - | - | mJ | $V_{DD}$=25V, L=0.1mH, $I_{AS}$=5A |

## Source-Drain Diode

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Continuous Source Current[1,6] | $I_S$ | - | - | 15 | A | $V_G$=$V_D$=0V, Force Current |
| Pulsed Source Current[2,6] | $I_{SM}$ | - | - | 24 | A | |
| Forward On Voltage[2] | $V_{SD}$ | - | - | 1.2 | V | $V_{GS}$=0V, $I_S$=8A , $T_J$=25℃ |
| Reverse Recovery Time | $t_{rr}$ | - | 37 | - | ns | $I_F$=10A, dI/dt=100A/μs,<br>$T_J$=25℃ |
| Reverse Recovery Charge | $Q_{rr}$ | - | 27.3 | - | nC | |

Notes: **1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, ≦10sec, 125℃/W at steady state.**

**2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.**

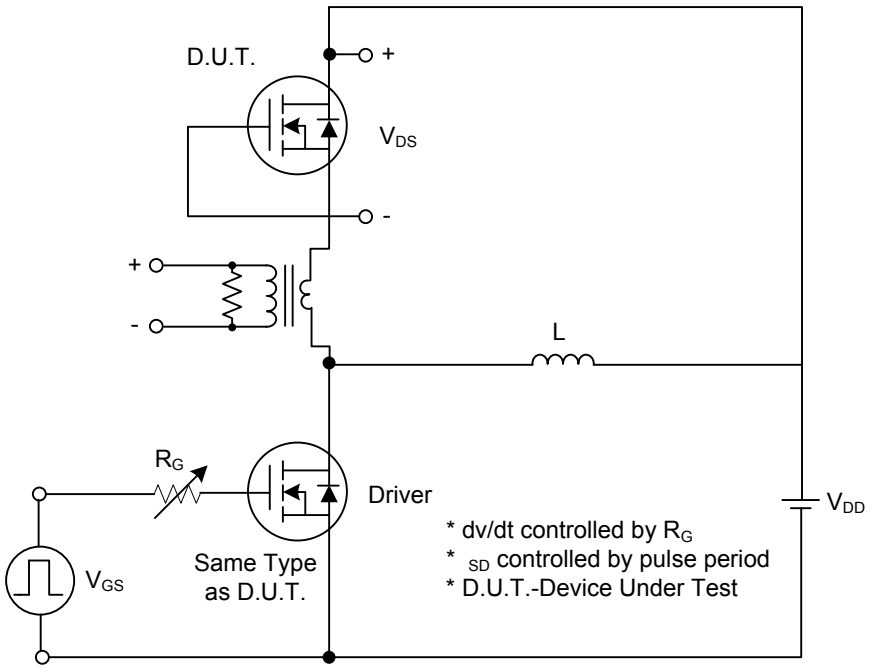
**3. The EAS data shows Max. rating. The test condition is VDD=25V, VGS=10V, L=0.1mH, IAS=11A.**

**4. The power dissipation is limited by 150℃ junction temperature.**

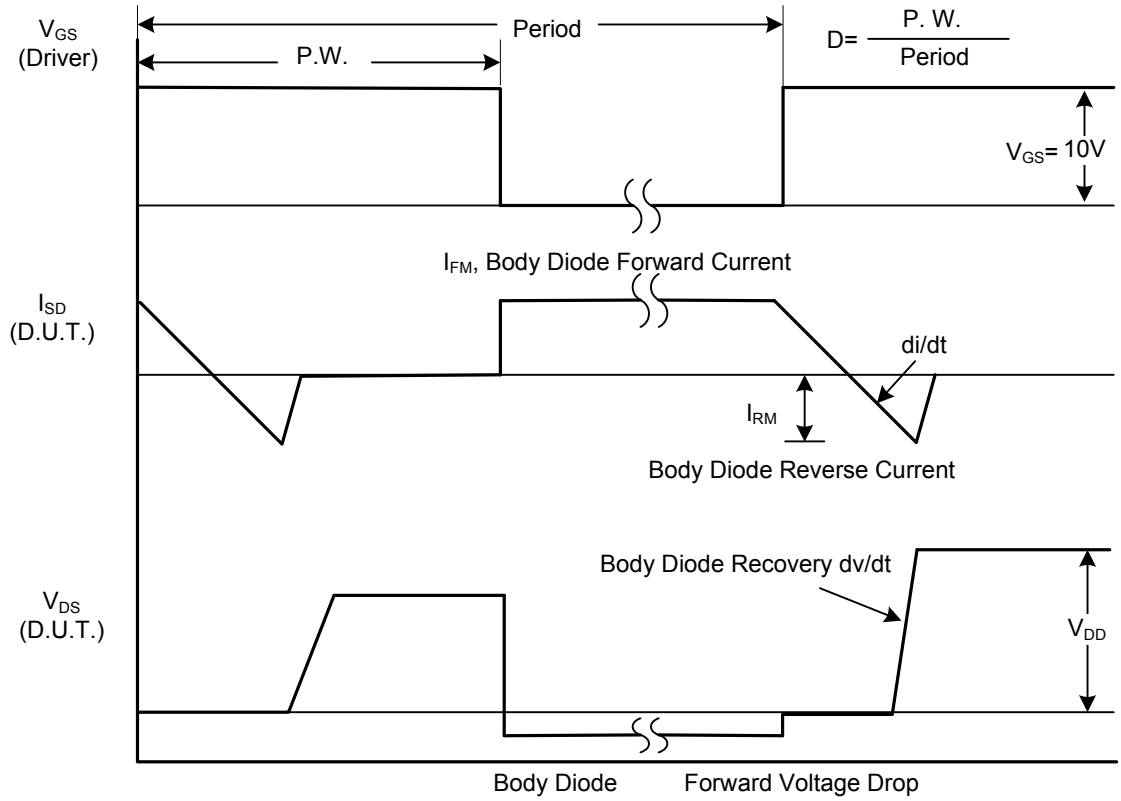
**5. The Min. value is 100% EAS tested guarantee.**

**6. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.**

## TEST CIRCUITS AND WAVEFORMS

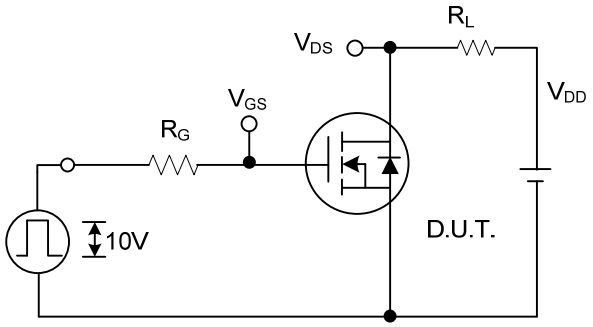



**Peak Diode Recovery dv/dt Test Circuit**

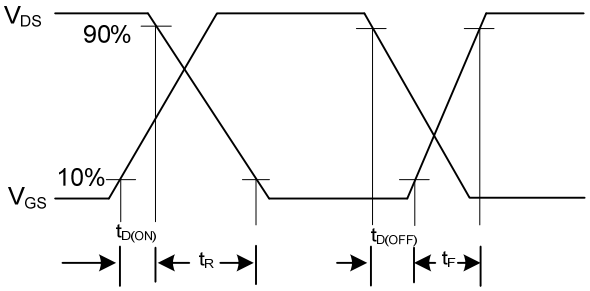



**Peak Diode Recovery dv/dt Waveforms**

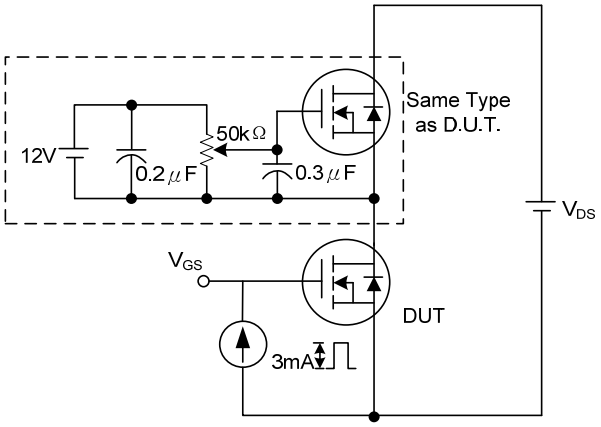
## TEST CIRCUITS AND WAVEFORMS(Cont.)



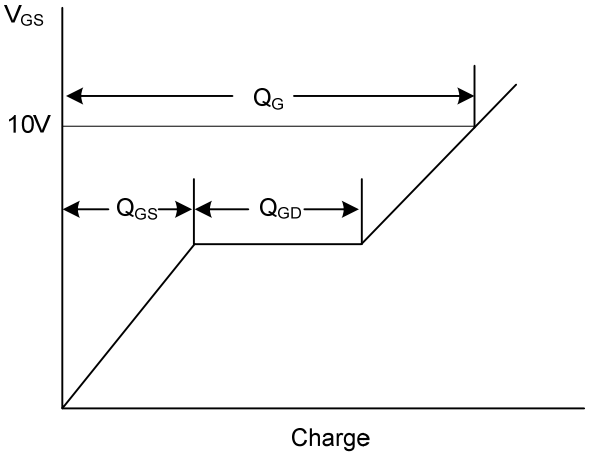

**Switching Test Circuit**



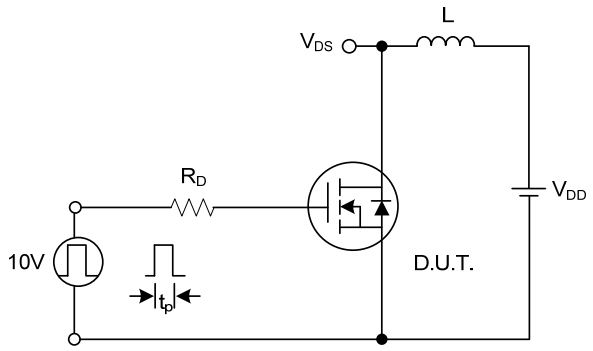

**Switching Waveforms**



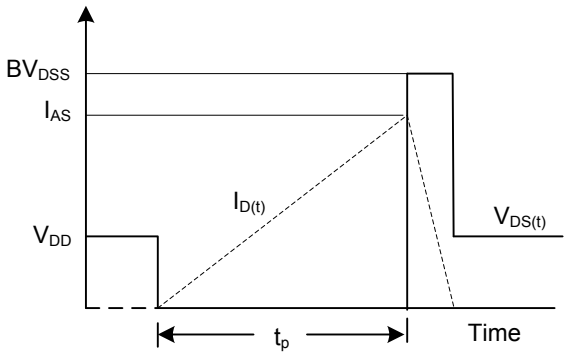

**Gate Charge Test Circuit**




**Gate Charge Waveform**




**Unclamped Inductive Switching Test Circuit**




**Unclamped Inductive Switching Waveforms**

## TYPICAL CHARACTERISTICS

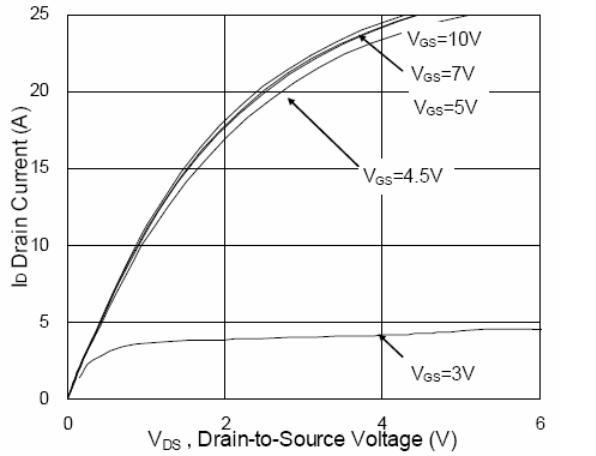



**Fig.1 Typical Output Characteristics**

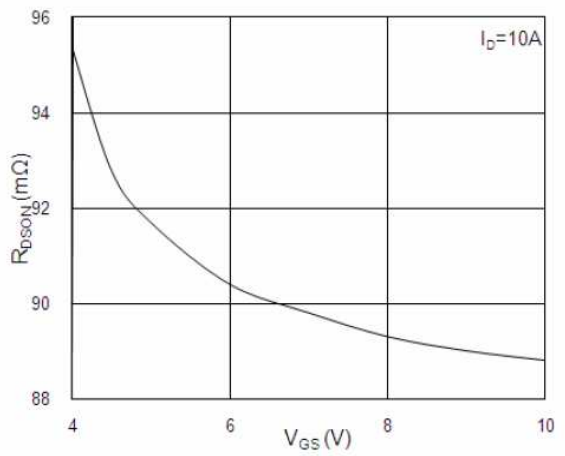



**Fig.2 On-Resistance vs. G-S Voltage**

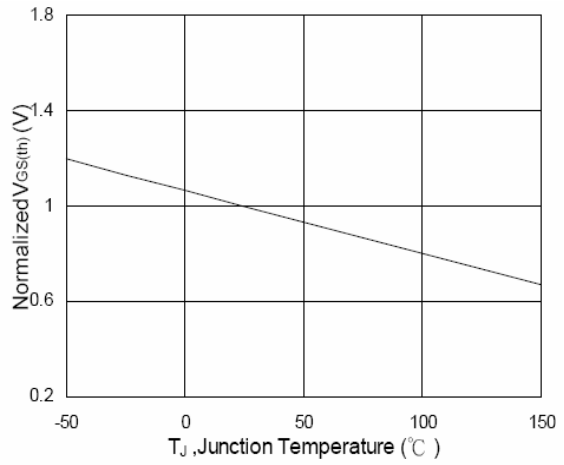



**Fig.3 Normalized $V_{GS(th)}$ vs. $T_J$**

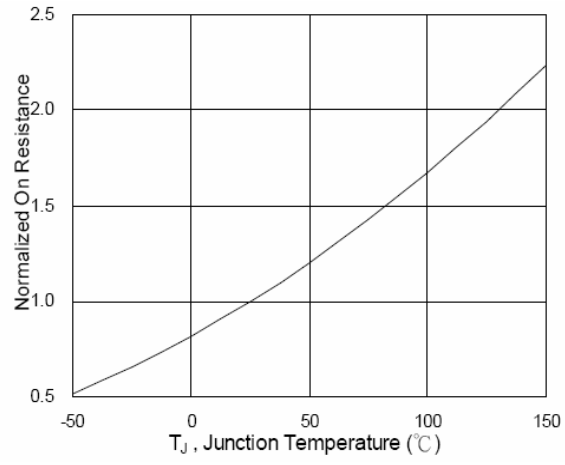



**Fig.4 Normalized $R_{DSON}$ vs. $T_J$**

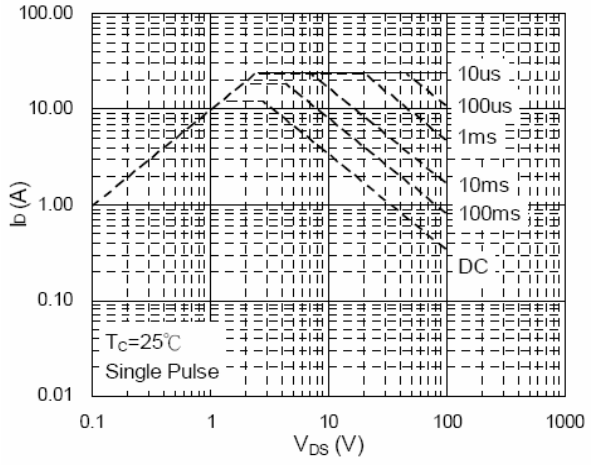



**Fig.5 Safe Operating Area**

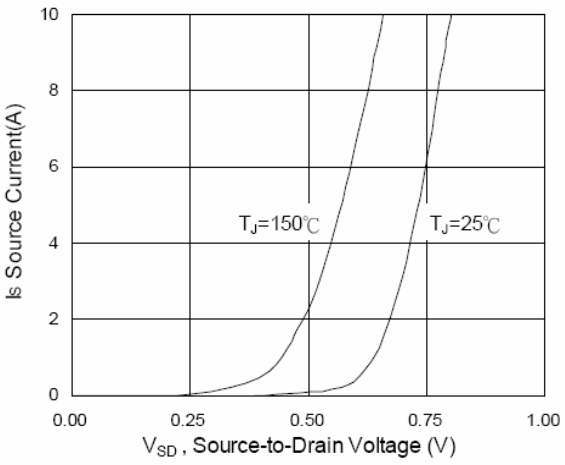



**Fig.6 Forward Characteristics of Reverse**

## TYPICAL CHARACTERISTICS(Cont.)

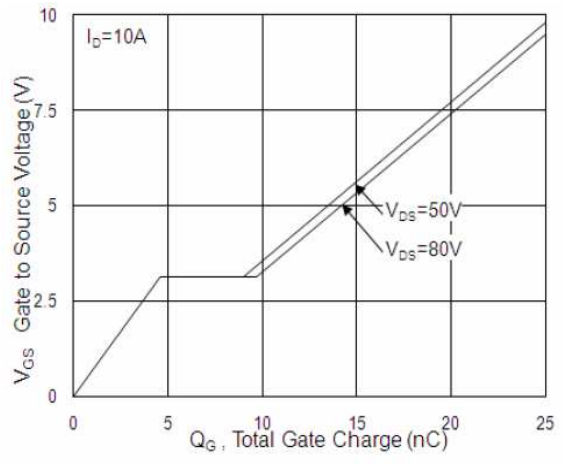



Fig.7 Gate Charge Characteristics

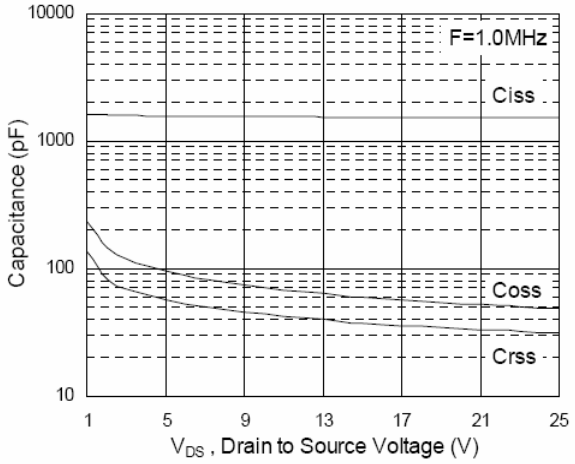



Fig.8 Capacitance Characteristic

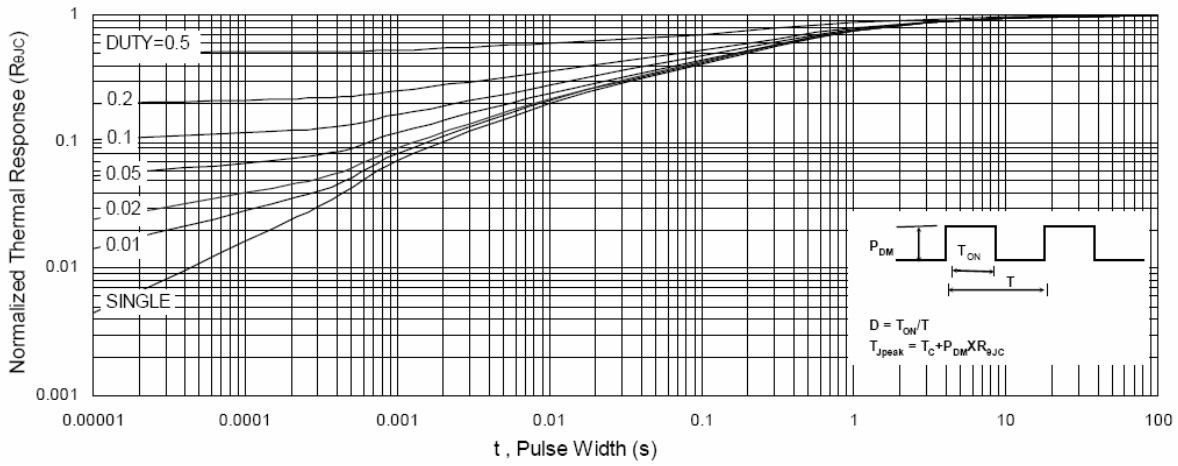



Fig.9 Normalized Maximum Transient Thermal Impedance

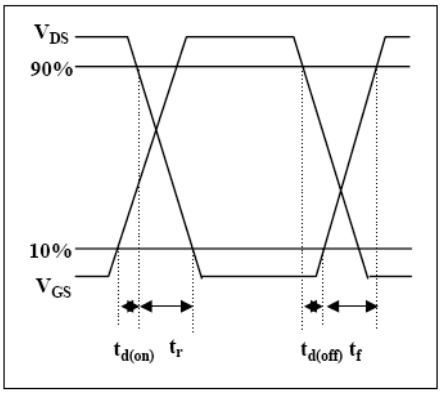



Fig.10 Switching Time Waveform

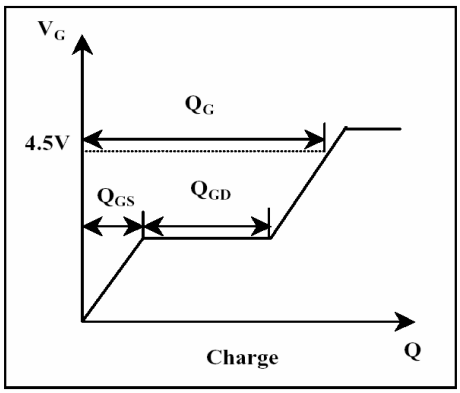
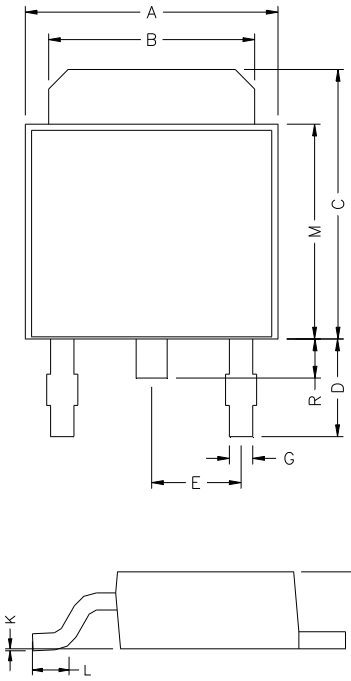



Fig.11 Gate Charge Waveform

# TO-252 Mechanical Drawing







| REF. | Millimeter | |
|---|---|---|
| | Min. | Max. |
| A | 6.40 | 6.80 |
| B | 5.13 | 5.53 |
| C | 6.80 | 7.25 |
| D | 2.90 | 3.30 |
| E | 2.19 | 2.39 |
| G | 0.45 | 0.85 |
| H | 2.20 | 2.40 |
| J | 0.41 | 0.61 |
| K | 0 | 0.15 |
| L | 1.40 | 1.85 |
| M | 5.90 | 6.30 |
| R | 0.60 | 1.20 |

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