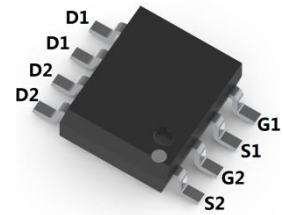


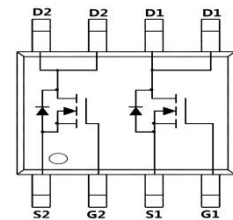
## Dual N-Channel Enhancement Mode Field Effect Transistor

## FEATURES

- Low on-resistance:  $V_{DS}=30V, I_D=6.9A, R_{DS(ON)} \leq 28m\Omega @ V_{GS}=10V$
- Low gate charge
- For synchronous rectifier applications
- Surface Mount device



SOP-8



## MECHANICAL DATA

- Case: SOP-8
- Case Material: Molded Plastic. UL flammability
- Classification Rating: 94V-0
- Weight: 0.3 grams (approximate)

MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-source voltage	$V_{DS}$	30	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current	$I_D$	$T_A = 25^\circ\text{C}$	6.9
		$T_A = 70^\circ\text{C}$	5.8
Pulsed drain current	$I_{DM}$	30	A
Power dissipation	$P_D$	$T_A = 25^\circ\text{C}$	2
		$T_A = 70^\circ\text{C}$	1.44
Thermal resistance from Junction to ambient	$R_{\theta JA}$	110	$^\circ\text{C/W}$
Thermal resistance from Junction to Lead	$R_{\theta JL}$	40	$^\circ\text{C/W}$
Junction temperature	$T_J$	150	$^\circ\text{C}$
Storage temperature	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain-Source breakdown voltage	$V_{(BR)DSS}^*$	30			V	$V_{GS}=0V, I_D=250\mu A$
Zero gate voltage drain current	$I_{DSS}^*$			1	$\mu A$	$V_{DS}=24V, V_{GS}=0V$
Gate-body leakage current	$I_{GSS}^*$			$\pm 100$	nA	$V_{DS}=0V, V_{GS}=\pm 20V$
Gate-threshold voltage	$V_{GS(th)}^*$	1	1.9	3	V	$V_{DS}=V_{GS}, I_D=250\mu A$
On-State Drain Current	$I_{D(ON)}^*$	20			A	$V_{DS}=5V, V_{GS}=4.5V$
Drain-source on-resistance	$R_{DS(ON)}^*$		22.5	28	m $\Omega$	$V_{GS}=10V, I_D=6.9A,$
			31.3	38	m $\Omega$	$V_{GS}=10V, I_D=6.9A, T_J=125^\circ\text{C}$
			34.5	42	m $\Omega$	$V_{GS}=4.5V, I_D=5A$
Forward transconductance	$g_{FS}$	10	15.4		S	$V_{DS}=5V, I_D=5A$
Diode forward voltage	$V_{SD}$		0.76	1	V	$I_S=1A, V_{GS}=0V$
Diode forward current	$I_S$			3	A	
Input capacitance	$C_{iss}$		680	820	pF	
Output capacitance	$C_{oss}$		102		pF	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$
Reverse transfer capacitance	$C_{rss}$		77		pF	
Gate resistance	$R_g$		3	3.6	$\Omega$	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$
Total gate charge	$Q_g$		6.74	8.1	nC	$V_{GS}=4.5V, V_{DS}=15V, I_D=6.9A$
			13.84	17	nC	
Gate-source charge	$Q_{gs}$		1.82		nC	$V_{GS}=10V, V_{DS}=15V, I_D=6.9A$
Gate-drain charge	$Q_{gd}$		3.2		nC	
Turn-on delay time	$t_{d(on)}$		4.6	7	nS	
Turn-on rise time	$t_r$		4.1	6.2	nS	$V_{GS}=10V, V_{DS}=15V,$
Turn-off delay time	$t_{d(off)}$		20.6	30	nS	$R_{GEN}=3\Omega, R_L=2.2\Omega$
Turn-off fall time	$t_f$		5.2	7.5	nS	
Body Diode Reverse Recovery Time	$t_{rr}$		16.5	20	nS	$I_F=6.9A, di/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	$Q_{rr}$		7.8	10	nC	$I_F=6.9A, di/dt=100A/\mu s$

\*Pulse test ; Pulse width =80 $\mu s$ , Duty cycle  $\leq 0.5\%$  .

Dual N-Channel Enhancement Mode Field Effect Transistor

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

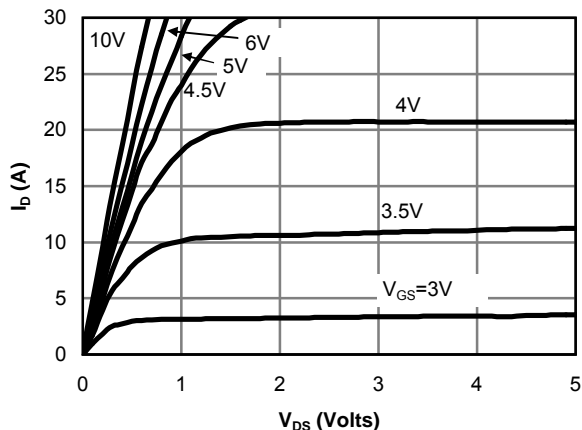


Fig 1: On-Region Characteristics

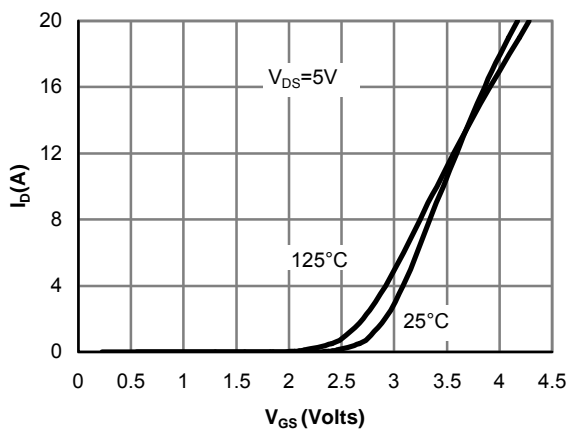


Figure 2: Transfer Characteristics

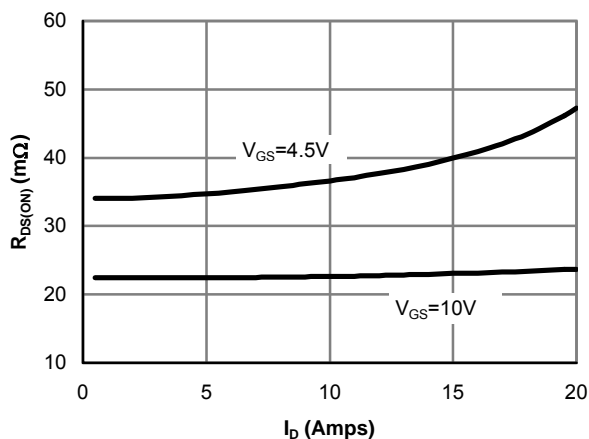


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

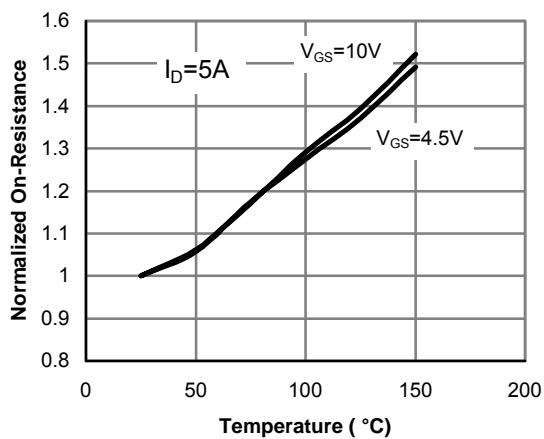


Figure 4: On-Resistance vs. Junction Temperature

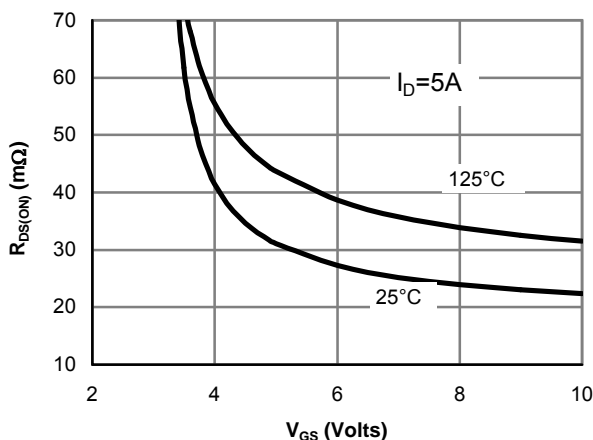


Figure 5: On-Resistance vs. Gate-Source Voltage

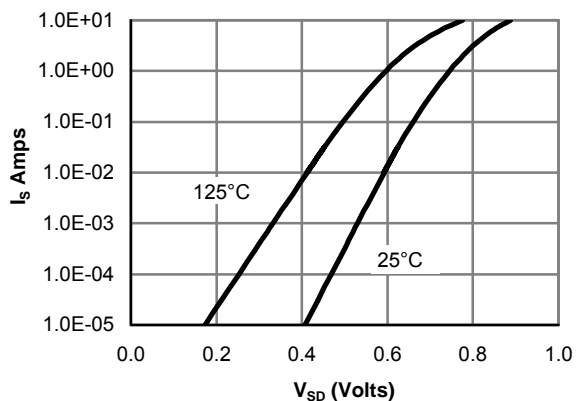


Figure 6: Body diode characteristics

Dual N-Channel Enhancement Mode Field Effect Transistor

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

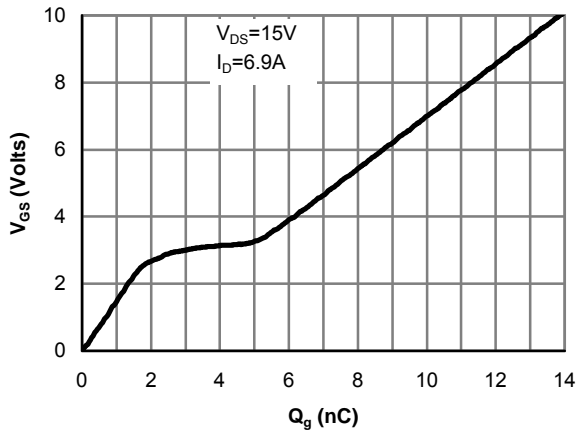


Figure 7: Gate-Charge characteristics

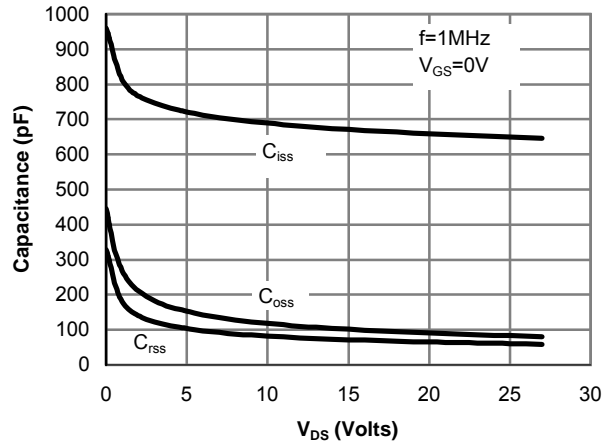


Figure 8: Capacitance Characteristics

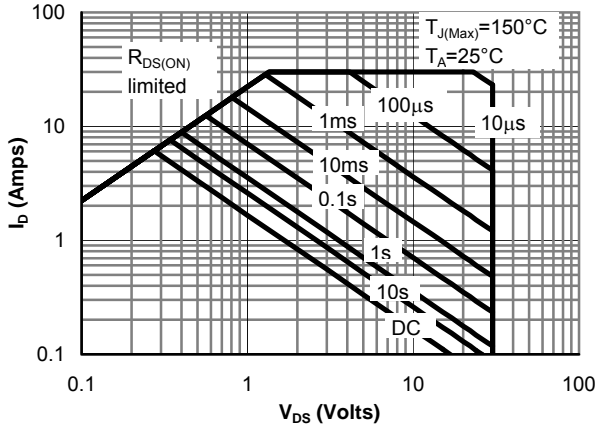


Figure 9: Maximum Forward Biased Safe Operating Area

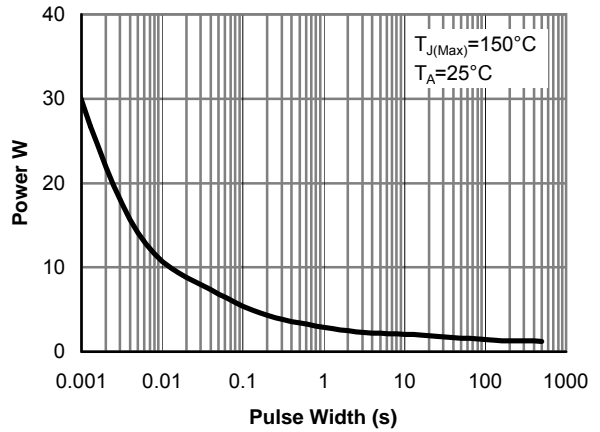


Figure 10: Single Pulse Power Rating Junction-to-Ambient

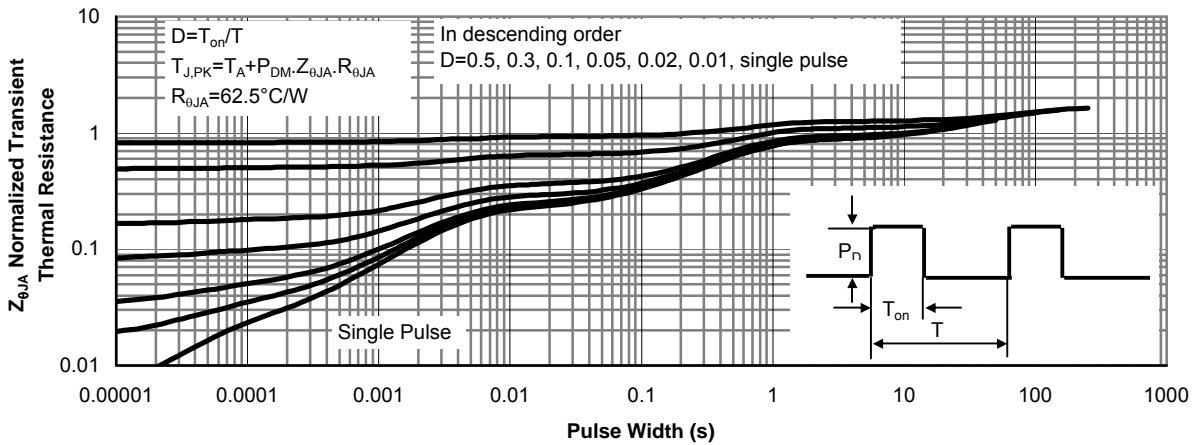
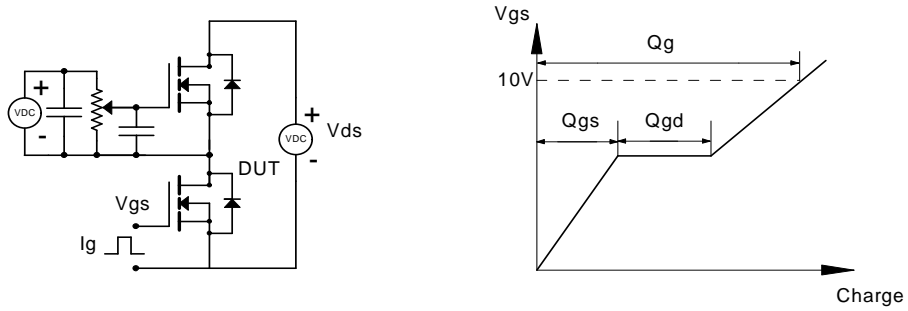


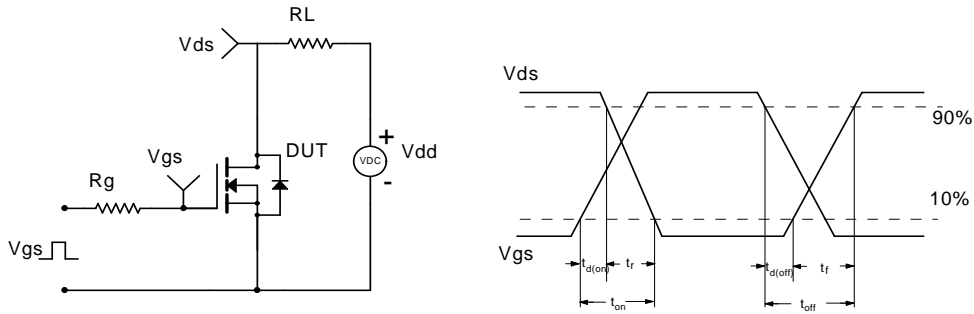
Figure 11: Normalized Maximum Transient Thermal Impedance

Dual N-Channel Enhancement Mode Field Effect Transistor

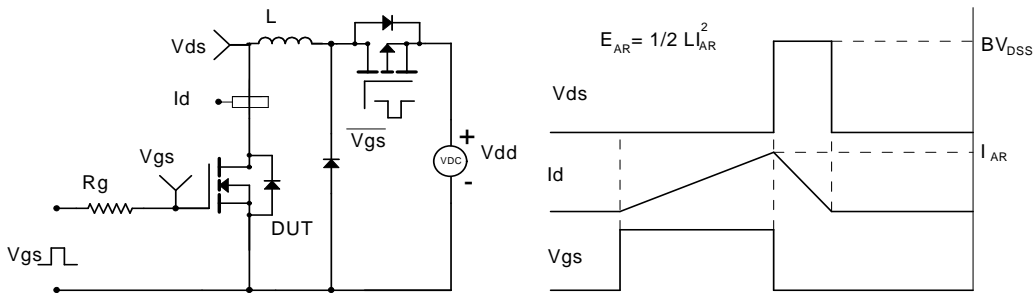
Gate Charge Test Circuit & Waveform



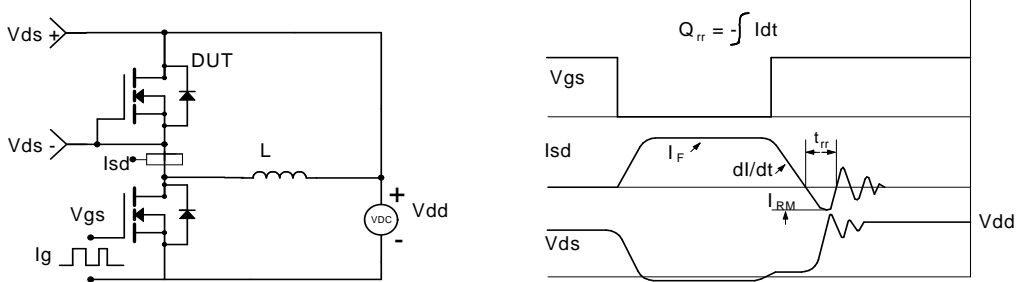
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

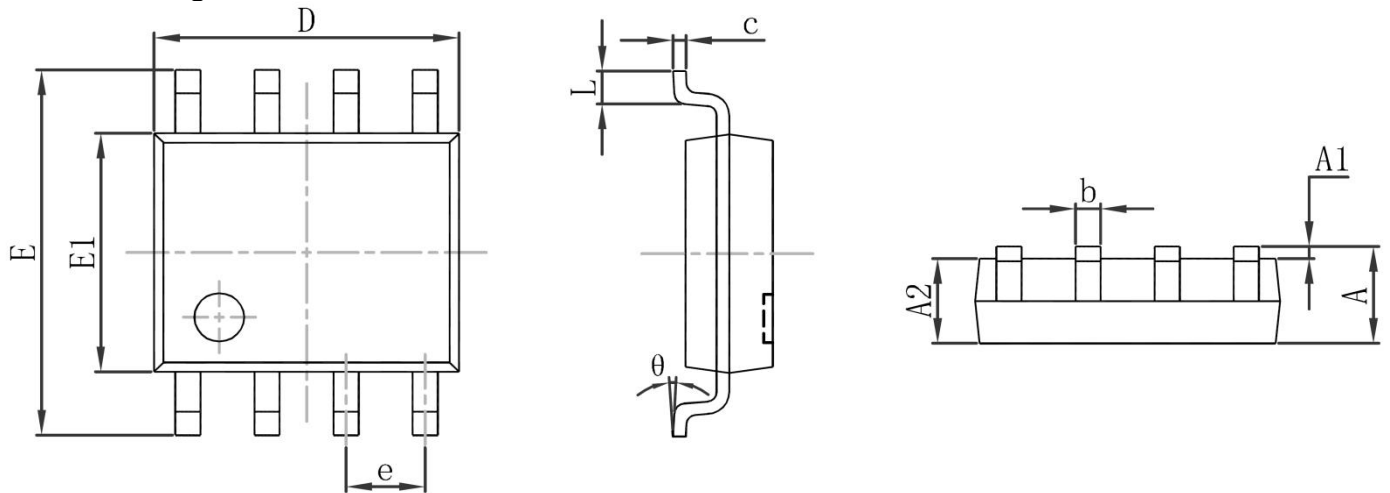


Diode Recovery Test Circuit & Waveforms



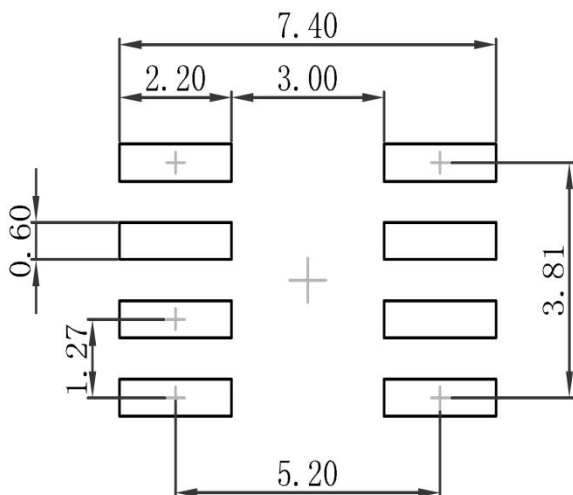
Dual N-Channel Enhancement Mode Field Effect Transistor

SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP-8 Suggested Pad Layout



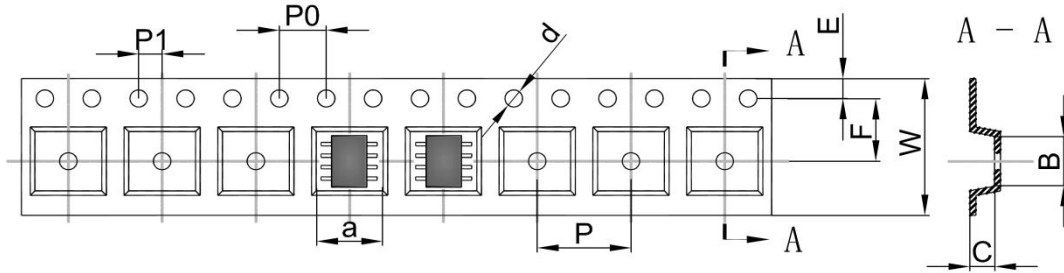
Note:

1. Controlling dimension: in millimeters
2. General tolerance: ±0.05mm
3. The pad layout is for reference purposes only

Dual N-Channel Enhancement Mode Field Effect Transistor

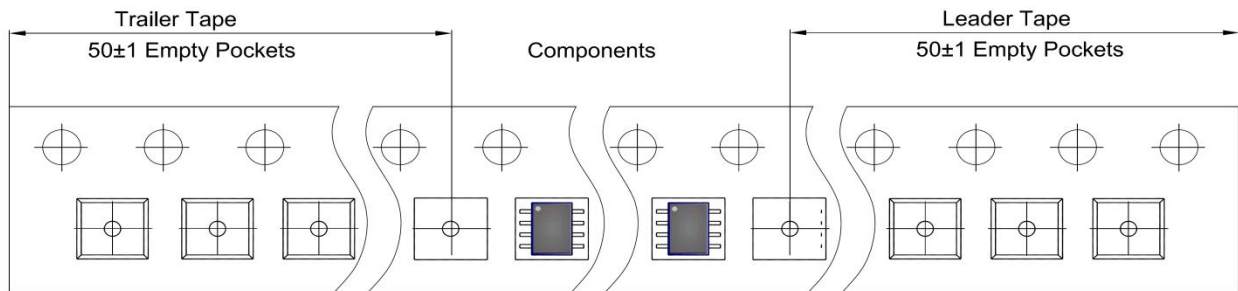
SOP-8 Tape and Reel

SOP-8 Embossed Carrier Tape

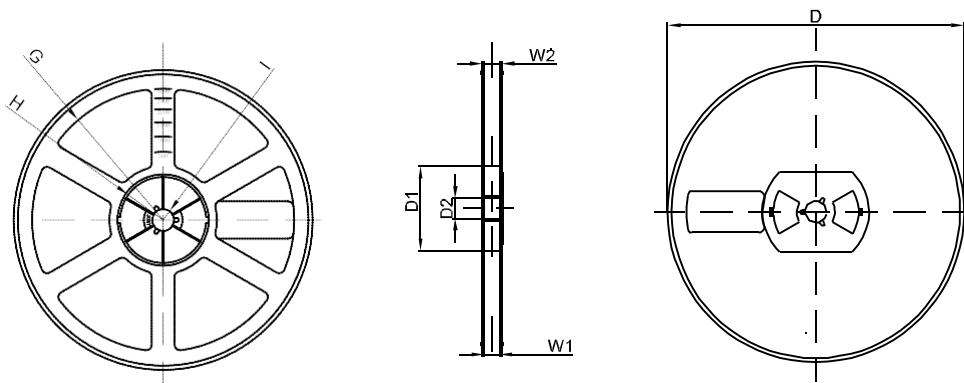


DIMENSIONS ARE IN MILLIMETER										
TYPE	A	B	C	d	E	F	P0	P	P1	W
SOP-8	6.40	5.40	2.10	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00
TOLERANCE	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1	±0.1

SOP-8 Tape Leader and Trailer



SOP-8 Reel



DIMENSIONS ARE IN MILLIMETER								
REEL OPTION	D	D1	D2	G	H	I	W1	W2
13" DIA	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60
TOLERANCE	±2	±1	±1	±1	±1	±1	±1	±1