

## NCE N-Channel Enhancement Mode Power MOSFET

### Description

The NCE4080K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

- $V_{DS} = 40V, I_D = 80A$   
 $R_{DS(ON)} < 7m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 15m\Omega @ V_{GS} = 4.5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

### Application

- PWM
- Load Switching

**100% UIS TESTED!**

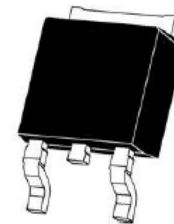
**100%  $\Delta V_{ds}$  TESTED!**



Schematic diagram



Marking and pin assignment



TO-252-2L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE4080K	NCE4080K	TO-252-2L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	80	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	56	A
Pulsed Drain Current	$I_{DM}$	350	A
Maximum Power Dissipation	$P_D$	80	W
Derating factor		0.53	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	750	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1.88	$^{\circ}\text{C/W}$
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**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

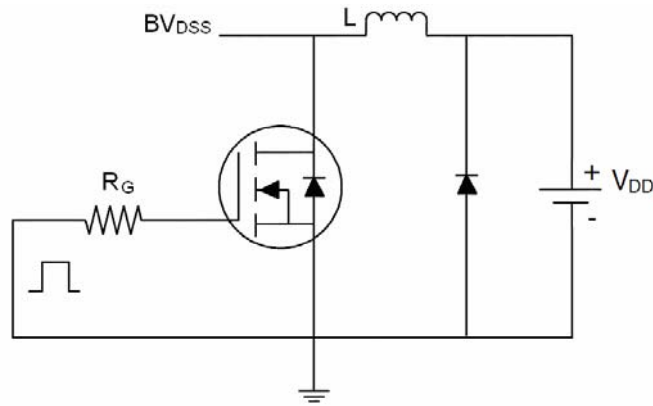
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40	45	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	5.2	7	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	10	15	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=20A$	15	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	2662	3200	PF
Output Capacitance	$C_{oss}$		-	322	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	246	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, R_L=1\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	12	-	nS
Turn-on Rise Time	$t_r$		-	11	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	39	-	nS
Turn-Off Fall Time	$t_f$		-	12	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=20V, I_D=20A,$ $V_{GS}=10V$	-	54.3	-	nC
Gate-Source Charge	$Q_{gs}$		-	6.9	-	nC
Gate-Drain Charge	$Q_{gd}$		-	14.5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	80	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = 20A$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-	-	45	nS
Reverse Recovery Charge	$Q_{rr}$		-	-	50	nC

**Notes:**

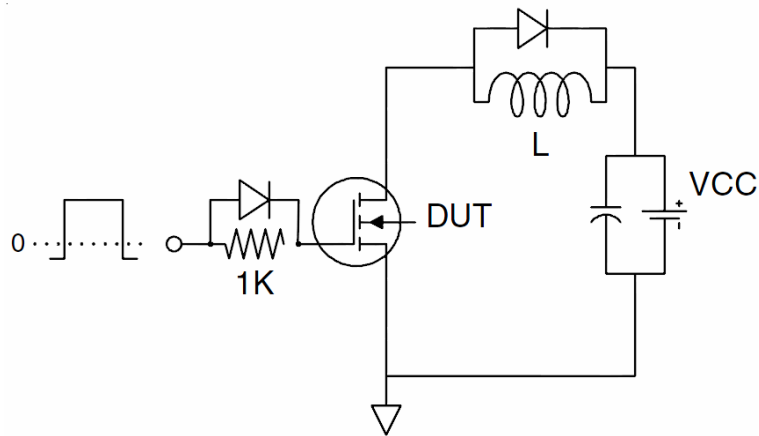
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition :  $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=1\text{mH}, R_g=25\Omega, I_{AS}=42A$

Test circuit

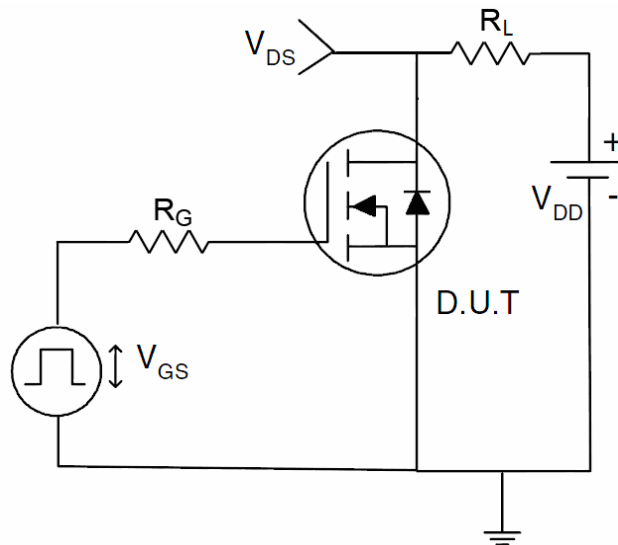
1)  $E_{AS}$  Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

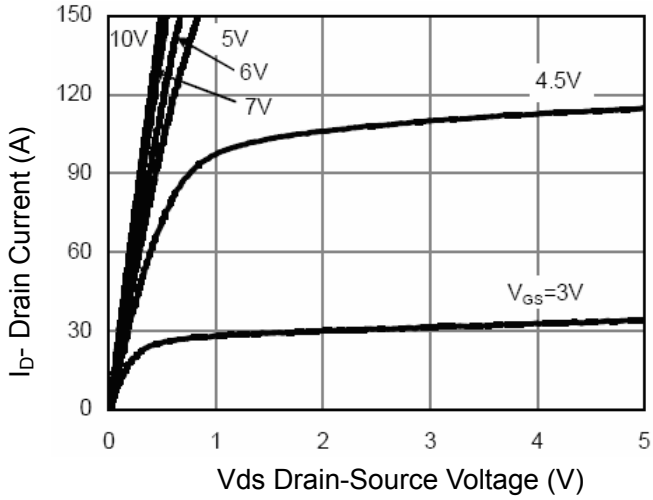


Figure 1 Output Characteristics

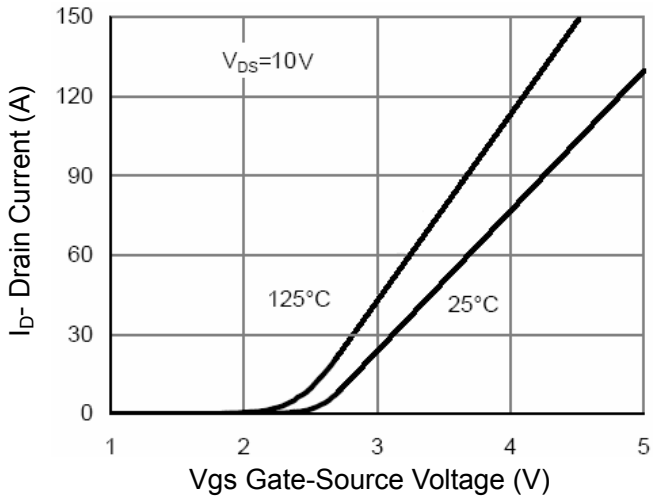


Figure 2 Transfer Characteristics

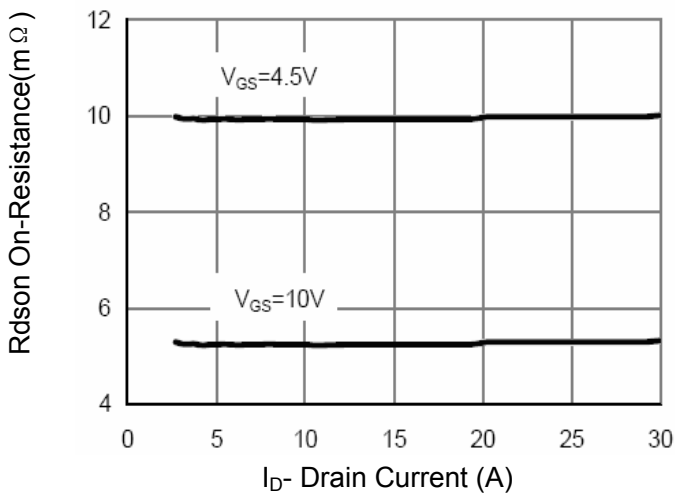


Figure 3 Rdson- Drain Current

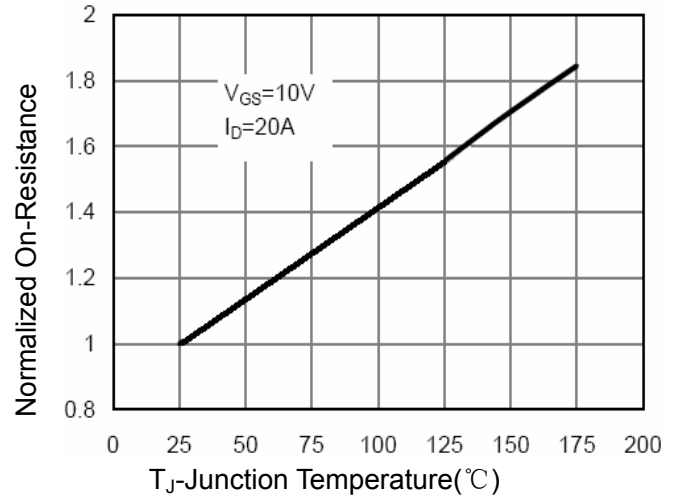


Figure 4 Rdson-Junction Temperature

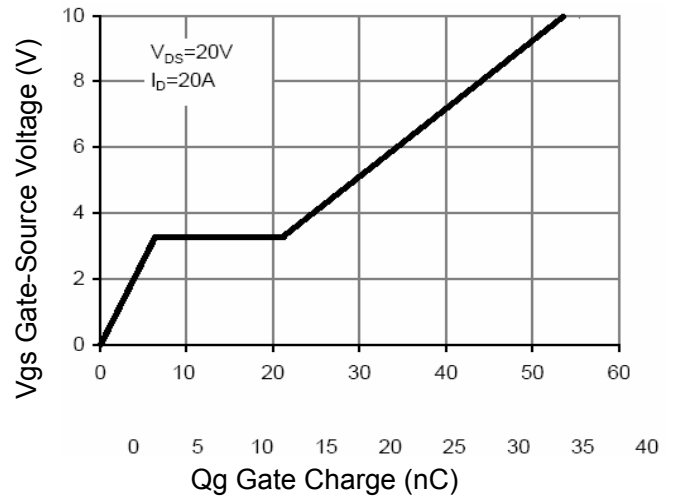


Figure 5 Gate Charge

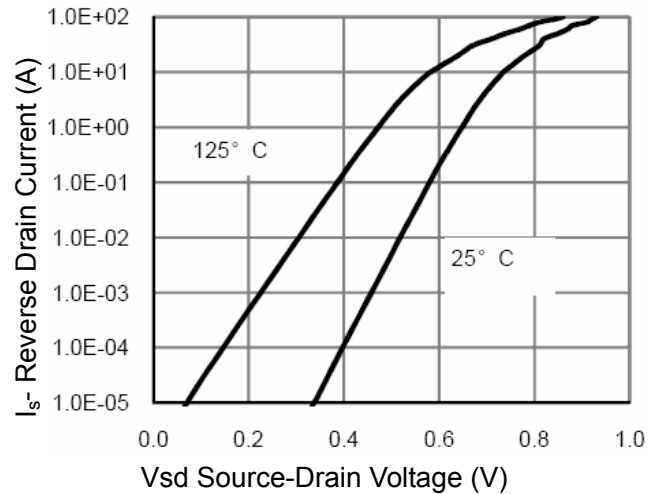


Figure 6 Source- Drain Diode Forward

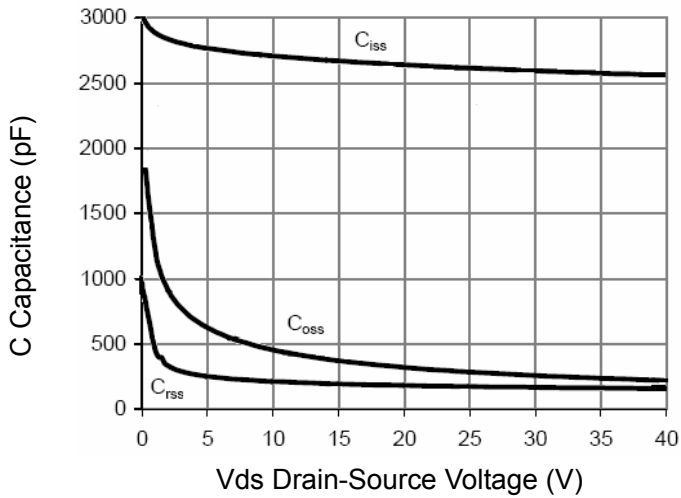


Figure 7 Capacitance vs Vds

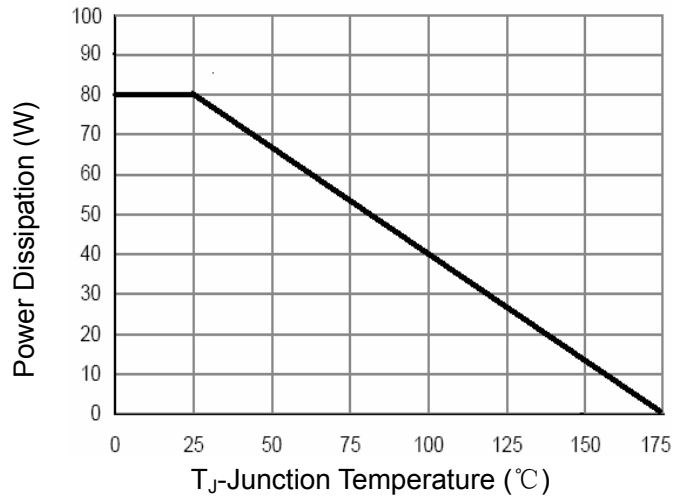


Figure 9 Power De-rating

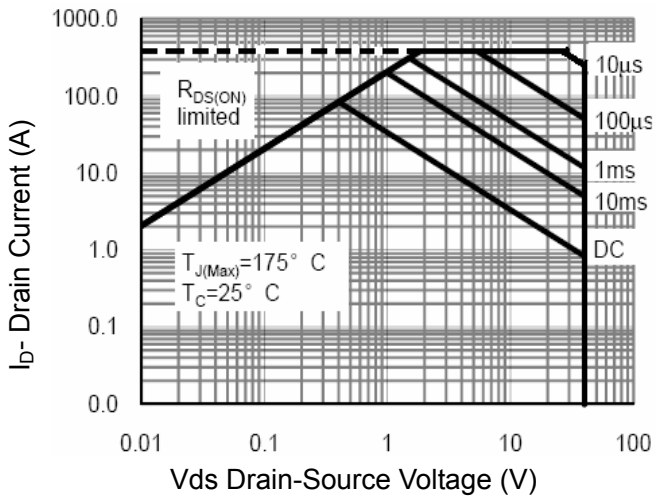


Figure 8 Safe Operation Area

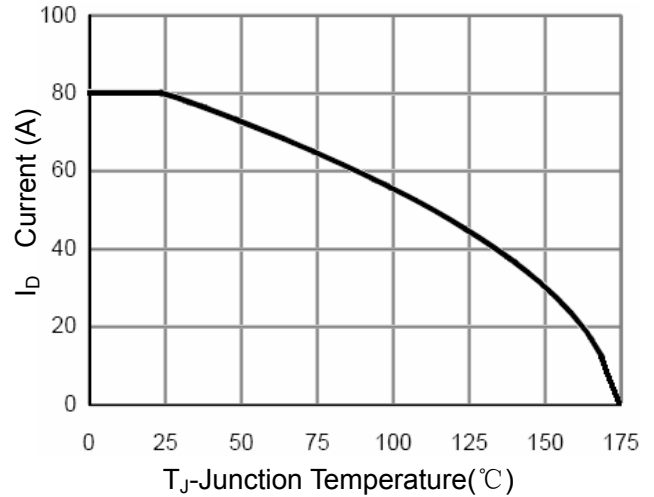


Figure 10 ID Current- Junction Temperature

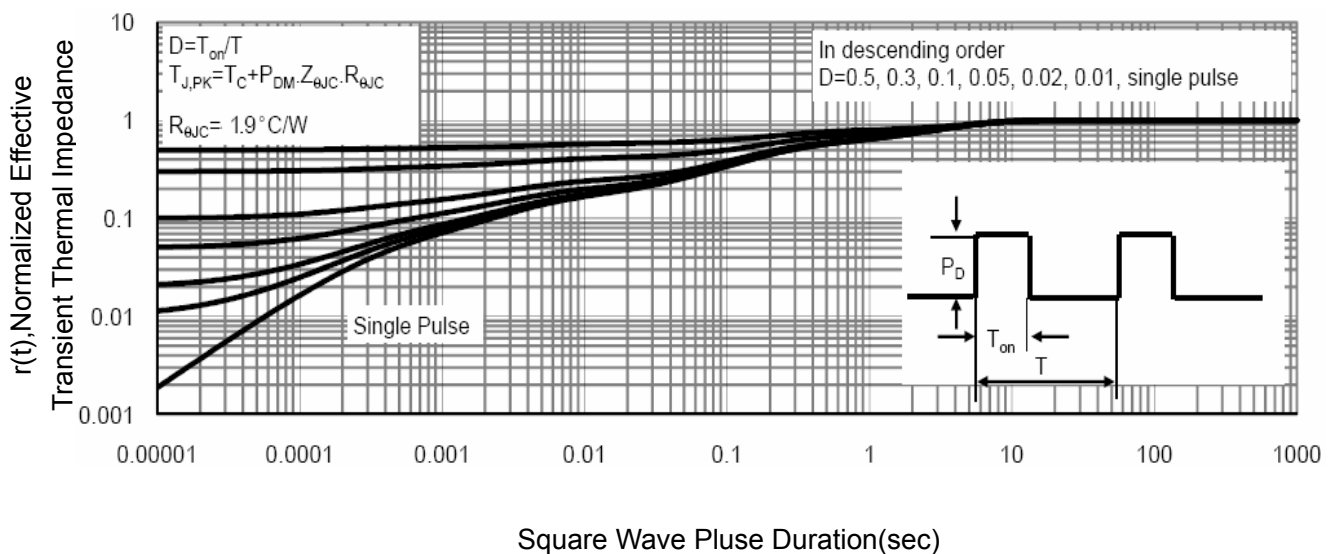
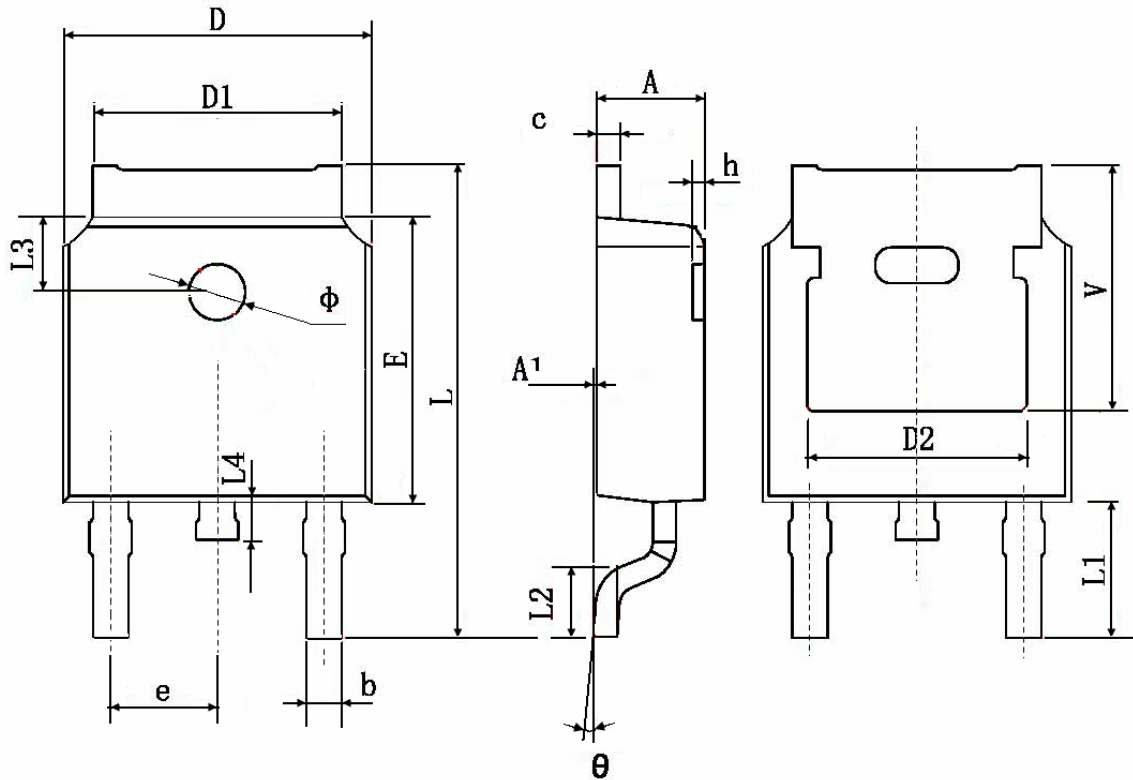


Figure 11 Normalized Maximum Transient Thermal Impedance

**TO-252 Package Information**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

**Remark:** 由于有多家封装合格供应商，在封装外形有略微差异，脚间距符合JEDEC标准。

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