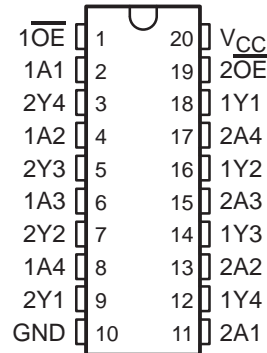


# SN54HCT240, SN74HCT240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS174E – MARCH 1984 – REVISED AUGUST 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current Outputs Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

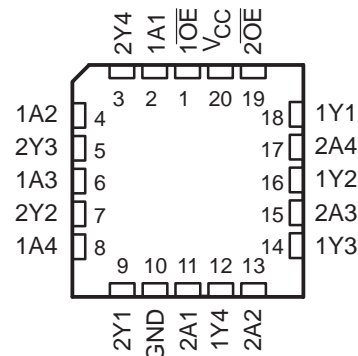
SN54HCT240 . . . J OR W PACKAGE  
SN74HCT240 . . . DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



## description/ordering information

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The 'HCT240 devices are organized as two 4-bit buffers/drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes inverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

SN54HCT240 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 20	SN74HCT240N	SN74HCT240N
	SOIC – DW	Tube of 25	SN74HCT240DW	HCT240
		Reel of 2000	SN74HCT240DWR	
	SOP – NS	Reel of 2000	SN74HCT240NSR	HCT240
	TSSOP – PW	Tube of 70	SN74HCT240PW	HT240
		Reel of 2000	SN74HCT240PWR	
Reel of 250		SN74HCT240PWT		
-55°C to 125°C	CDIP – J	Tube of 20	SNJ54HCT240J	SNJ54HCT240J
	CFP – W	Tube of 85	SNJ54HCT240W	SNJ54HCT240W
	LCCC – FK	Tube of 55	SNJ54HCT240FK	SNJ54HCT240FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

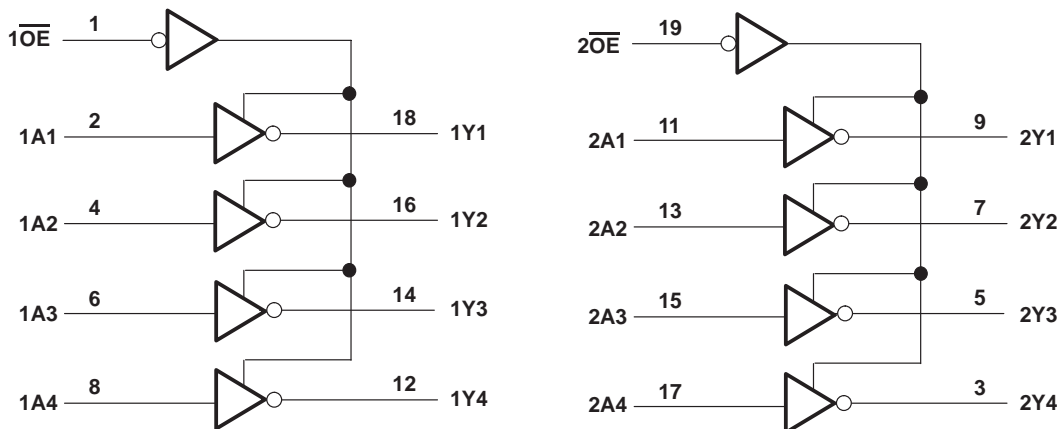
# SN54HCT240, SN74HCT240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS174E – MARCH 1984 – REVISED AUGUST 2003

FUNCTION TABLE  
(each buffer/driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND	$\pm 70$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54HCT240, SN74HCT240 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

		SN54HCT240			SN74HCT240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			2			V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			0.8			V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
Δt/Δv	Input transition rise/fall time	500			500			ns
T <sub>A</sub>	Operating free-air temperature	-55	125		-40	85		°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT240		SN74HCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4	V	
		I <sub>OH</sub> = -6 mA		3.98	4.3		3.7		3.84		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.5 V		0.001	0.1		0.1	0.1	V	
		I <sub>OL</sub> = 6 mA			0.17	0.26		0.4	0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		5.5 V	±0.1	±100		±1000	±1000	nA		
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		5.5 V	±0.01	±0.5		±10		±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		5.5 V			8	160		80	μA	
ΔI <sub>CC</sub> †	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>		5.5 V		1.4	2.4	3		2.9	mA	
C <sub>i</sub>			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT240		SN74HCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	4.5 V		13	25		37		32	ns
			5.5 V		12	23		33		29	
t <sub>en</sub>	$\overline{\text{OE}}$	Y	4.5 V		21	35		53		44	ns
			5.5 V		19	32		48		40	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	4.5 V		19	35		53		44	ns
			5.5 V		18	32		48		40	
t <sub>t</sub>		Y	4.5 V		8	12		18		15	ns
			5.5 V		7	11		16		14	



**SN54HCT240, SN74HCT240**  
**OCTAL BUFFERS AND LINE DRIVERS**  
**WITH 3-STATE OUTPUTS**

SCLS174E – MARCH 1984 – REVISED AUGUST 2003

switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$   
(unless otherwise noted) (see Figure 1)

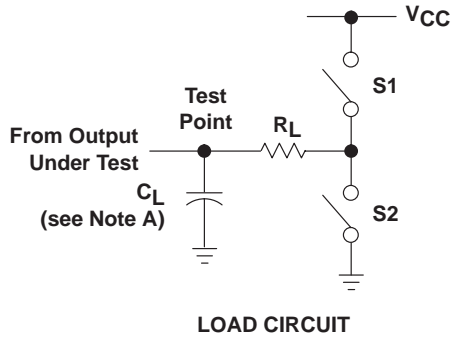
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT240		SN74HCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	4.5 V	20	42	63	53	ns			
			5.5 V	19	38	56	48				
$t_{en}$	$\overline{OE}$	Y	4.5 V	25	52	79	65	ns			
			5.5 V	22	47	71	59				
$t_t$		Y	4.5 V	17	42	63	53	ns			
			5.5 V	14	38	57	48				

operating characteristics,  $T_A = 25^\circ\text{C}$

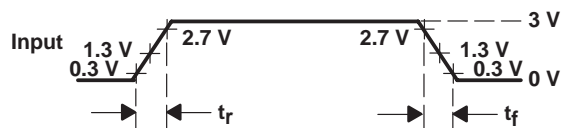
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	40	pF



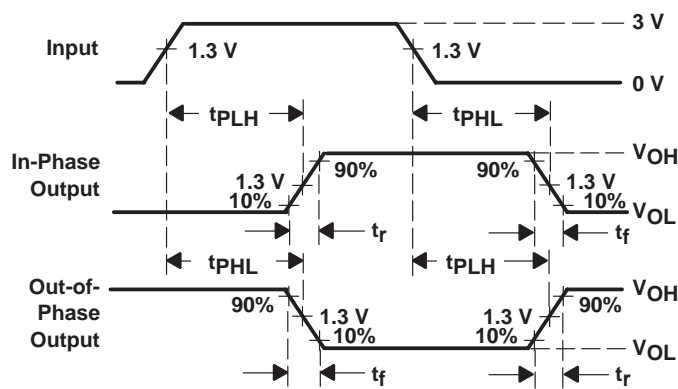
PARAMETER MEASUREMENT INFORMATION



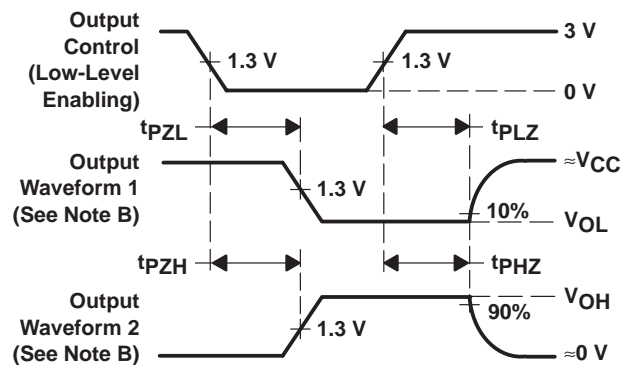
PARAMETER		$R_L$	$C_L$	S1	S2
$t_{en}$	$t_{PZH}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
	$t_{PZL}$			Closed	Open
$t_{dis}$	$t_{PHZ}$	1 k $\Omega$	50 pF	Open	Closed
	$t_{PLZ}$			Closed	Open
$t_{pd}$ or $t_t$		--	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORM  
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
85505012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	POST-PLATE	N / A for Pkg Type	-55 to 125	85505012A SNJ54HCT 240FK	<a href="#">Samples</a>
8550501RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	8550501RA SNJ54HCT240J	<a href="#">Samples</a>
JM38510/65753BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65753BRA	<a href="#">Samples</a>
M38510/65753BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65753BRA	<a href="#">Samples</a>
SN54HCT240J	ACTIVE	CDIP	J	20	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HCT240J	<a href="#">Samples</a>
SN74HCT240DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT240	<a href="#">Samples</a>
SN74HCT240DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT240	<a href="#">Samples</a>
SN74HCT240DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT240	<a href="#">Samples</a>
SN74HCT240DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT240	<a href="#">Samples</a>
SN74HCT240N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT240N	<a href="#">Samples</a>
SN74HCT240NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT240	<a href="#">Samples</a>
SN74HCT240PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT240	<a href="#">Samples</a>
SN74HCT240PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT240	<a href="#">Samples</a>
SN74HCT240PWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT240	<a href="#">Samples</a>
SNJ54HCT240FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Non-Green	POST-PLATE	N / A for Pkg Type	-55 to 125	85505012A SNJ54HCT 240FK	<a href="#">Samples</a>
SNJ54HCT240J	ACTIVE	CDIP	J	20	1	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	8550501RA SNJ54HCT240J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HCT240, SN74HCT240 :**

● Catalog: [SN74HCT240](#)

● Military: [SN54HCT240](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74HCT240NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HCT240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HCT240PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HCT240NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HCT240PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74HCT240PWT	TSSOP	PW	20	250	367.0	367.0	38.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002



# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.