TPS2595xx 2.7V 至 18V、4A、34mΩ 电子保险丝，具有快速过压保护

1 特性

- 宽输入电压范围：2.7V 至 18V
  - 绝对最大值为 20V
  - TPS2595x5 版本：3V 至 18V
- 低导通电阻：R_{ON} = 34mΩ（典型值）
- 快速过压保护钳位（3.8V、5.7V 和 13.7V），响应时间 5µs（典型值）
- TPS2595x0、TPS2595x1、TPS2595x5：带有可调节欠压锁定 (UVLO) 的高电平有效使能输入
- TPS2595x3：带有可调节过压锁定 (OVLO) 的低电平有效使能输入
- 配备负载电流监控器输出 (ILM) 的可调节电流限制
  - 电流范围：0.5A 至 4A
  - 电流限制准确度：±7.5%
- 可调节的输出转换率控制 (dVdt)
- 过热保护 (OTP)
- 故障指示引脚 ($\overline{FLT}$)
- UL 2367 认证 – 文件号E169910
  - R_{ILM} >= 487Ω（最大电流 4.42A）
- IEC 62368-1 认证
- 单点故障测试期间安全 (IEC 62368-1)
  - ILM 引脚断开/短路检测

2 应用

- 热插拔
- 适配器供电型系统
- 多功能打印机
- 固态硬盘 (SSD) 和硬盘 (HDD)
- 工业系统
- 白色家电
- 机顶盒
- 数字电视

3 说明

TPS2595xx 系列电子保险丝（集成式 FET 热插拔设备）是小型封装内高度集成电路的保护和电源管理解决方案。这些设备只需很少的外部组件即可提供多种保护模式，能够非常有效地抵御过载、短路、电压浪涌和过多浪涌电流。

输出电流限制级别可通过单个外部电阻设定。还可能通过测量整个电流限制电阻的压降实现对输出负载电流的准确感应。对 浪涌电流有特别要求的应用可以通过单个外部电容器设定输出转换率。过压事件由内部钳位电路快速限制在一个安全的固定最大值，而无需外部组件。TPS259573 型号提供可以设置用户定义过压截止阈值的选项。

在 TPS2595x5 型号中，可通过将 OUT 引脚连接到 QOD 引脚实施快速输出放电功能。

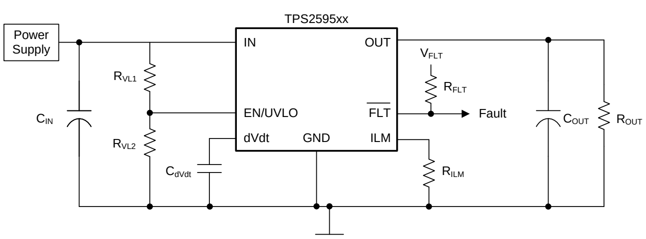
这些器件的独特运行温度范围为 –40°C 至 +125°C。

器件信息[1]

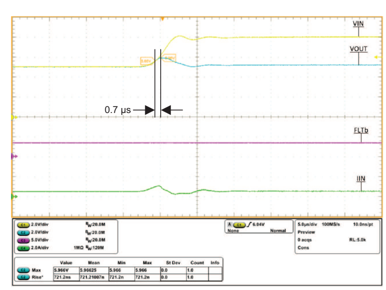
器件型号	封装	封装尺寸（标称值）
TPS2595xxDSG	WSON (8)	2.00mm x 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



TPS25953x 过压钳位响应时间



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4 修订历史记录

Changes from Revision B (March 2018) to Revision C	Page
• 已添加 将 (IEC 62368-1) 添加到*特性* 部分中的单点故障测试期间安全	1
• Changed UL 60950 to IEC 62368-1 in the Specifications *Electrical Characteristics* table	5

Changes from Revision A (December 2017) to Revision B	Page
• 已更改 multiplication symbol to an equal symbol before 229.2 mW in 公式 15	29

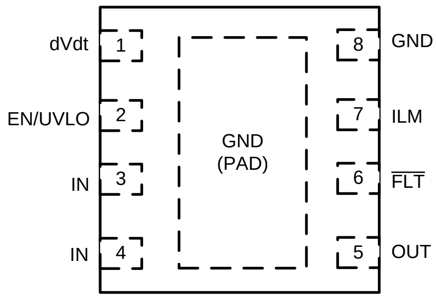
Changes from Original (June 2017) to Revision A	Page
• 将状态从预告信息更改成了生产数据	1

5 Device Comparison Table

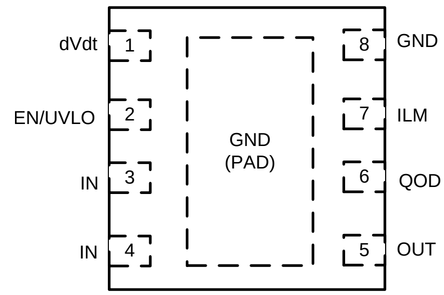
DEVICE NUMBER	OUTPUT VOLTAGE CLAMP	RESPONSE TO THERMAL SHUTDOWN (TSD)	ENABLE	QUICK OUTPUT DISCHARGE
TPS259520DSG	3.8 V (typ)	Latch-off	Active high	No
TPS259521DSG	3.8 V (typ)	Auto-retry	Active high	No
TPS259530DSG	5.7 V (typ)	Latch-off	Active high	No
TPS259531DSG	5.7 V (typ)	Auto-retry	Active high	No
TPS259533DSG	5.7 V (typ)	Auto-retry	***Active low***	No
TPS259540DSG	13.7 V (typ)	Latch-off	Active high	No
TPS259541DSG	13.7 V (typ)	Auto-retry	Active high	No
TPS259570DSG	No OV clamp	Latch-off	Active high	No
TPS259571DSG	No OV clamp	Auto-retry	Active high	No
TPS259573DSG	Programmable Overvoltage Lockout	Auto-retry	***Active low***	No
TPS259525DSG	3.8 V (typ)	Auto-retry	Active high	***Yes***
TPS259535DSG	5.7 V (typ)	Auto-retry	Active high	***Yes***

6 Pin Configuration and Functions

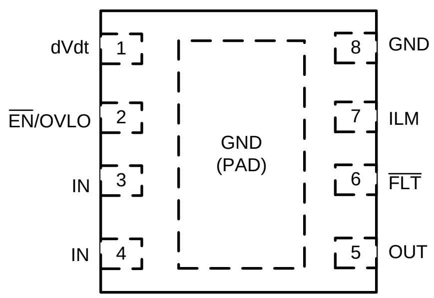
TPS2595x0/1 DSG Package
8-Pin WSON
Top View



TPS2595x5 DSG Package
8-Pin WSON
Top View



TPS2595x3 DSG Package
8-Pin WSON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	dVdt	Analog I/O	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. (See *Switching Characteristics*).
2	EN/UVLO	Analog input	Active high enable for the **TPS2595x0, TPS2595x1, TPS2595x5** variants. A resistor divider can be used to adjust the undervoltage lockout threshold. Do not leave floating.
	$\overline{\text{EN}}$/OVLO		Active low enable for the **TPS2595x3** variants. A resistor divider can be used to adjust the overvoltage lockout threshold. Do not leave floating.
3,4	IN	Power	Power input
5	OUT	Power	Power output
6	$\overline{\text{FLT}}$	Digital output	**TPS2595x0, TPS2595x1, TPS2595x3**: Fault event indicator which is pulled low when a fault is detected. It is an open drain output that requires an external pull up resistance.
	QOD		**TPS2595x5**: Quick Output Discharge Pin, when tied to OUT directly or through external resistor.
7	ILM	Analog I/O	This is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit. The pin voltage can also be used to monitor the output load current. Do not leave floating.
8	GND	Ground	Ground
PAD	GND	Thermal/Ground	The exposed pad is used primarily for heat dissipation and must be connected to GND.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{IN}	Maximum input voltage	IN	–0.3	20	V
V_{OUT}	Maximum output voltage	OUT	–0.3	V_{IN} + 0.3	V
$V_{OUT,PLS}$	Minimum output voltage pulse (< 1 µs)	OUT	–1.2		V
V_{EN}	Maximum enable pin voltage	EN/UVLO or $\overline{EN}$/OVLO	–0.3	7	V
V_{FLTB}	Maximum fault pin voltage (TPS2595x0/1/3)	$\overline{FLT}$	–0.3	7	V
V_{QOD}	Maximum QOD pin voltage (TPS2595x5)	QOD	–0.3	7	V
V_{dVdt}	Maximum dVdt pin voltage	dVdt		2.5	V
I_{FLTB}	Maximum fault pin sink current	$\overline{FLT}$		10	mA
I_{MAX}	Maximum continuous switch current	IN to OUT	Internally limited		
$T_{J,MAX}$	Maximum junction temperature		Internally limited		
T_{LEAD}	Maximum lead temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range (TPS2595x0/1/3)	IN	2.7	18 (1)	V
V_{IN}	Input voltage range (TPS2595x5)	IN	3.0	18(1)	V
V_{OUT}	Output voltage	OUT	0	V_{IN} + 0.3	V
V_{EN}	Enable pin voltage	EN/UVLO or $\overline{EN}$/OVLO	0	6(2)	V
V_{FLTB}	Fault pin voltage (TPS2595x0/1/3)	$\overline{FLT}$	0	6	V
V_{QOD}	Fault pin voltage (TPS2595x5)	QOD	0	6	V
I_{MAX}	Continuous output current (T_J = –40 to 125°C)	IN to OUT		4	A
	Continuous output current (T_J = –40 to 105°C)	IN to OUT		5(3)	A
R_{ILM}	ILM pin resistance (Active Current Limiting Operation)	ILM	487	5000	Ω
C_{dVdt}	dVdt capacitor value	dVdt	3300		pF
V_{dVdt}	dVdt pin capacitor voltage rating	dVdt	4		V
T_J	Operating junction temperature		–40	125	°C

(1) The nominal input voltage should be limited to the output clamp voltage for the selected device option as listed in the Electrical Characteristics section
(2) For supply voltages below 6V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 6V, it is recommended to use an appropriate resistor divider between IN, EN and GND to ensure the voltage at the EN pin is within the specified limits.
(3) Guaranteed by design. Not tested at production.

7.4 Thermal Information

THERMAL METRIC (1)		TPS2595x DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V for TPS25954x/7x, V_{IN} = 5 V for TPS25953x, V_{IN} = 3.3 V for TPS25952x, V_{EN} = 5 V (= 0 V for TPS2595x3 only) , R_{ILM} = 487 Ω , C_{dVdT} = Open, OUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT SUPPLY (IN)								
I_Q	IN quiescent current	TPS2595x0/1/5	V_{EN} ≥ V_{UVLO}			175	250	µA
		TPS2595x3	V_{EN} ≤ V_{OVLO}					
I_{SD}	IN shutdown current	TPS2595x0/1/5	V_{EN} < 0.5V	V_{IN} ≤ 5 V		0.04		µA
				5 V < VIN ≤ 18 V		0.45	2	µA
		TPS2595x3	V_{EN} > 2 V			45	65	µA
V_{UVP}	IN Undervoltage Protection Threshold	TPS2595x5	V_{IN} Rising		2.7	2.8	2.9	V
		TPS2595x5	V_{IN} Falling		2.58	2.68	2.78	V
		TPS2595x0/1/3	V_{IN} Rising		2.44	2.54	2.64	V
		TPS2595x0/1/3	V_{IN} Falling		2.33	2.43	2.53	V
OUTPUT VOLTAGE CLAMP (OUT)								
V_{OVC}	Overvoltage clamp threshold(1)	TPS25952x	V_{IN} Rising, R_{OUT} = 10 kΩ		3.65	3.87	4.1	V
		TPS25953x			5.5	5.7	5.9	V
		TPS25954x			13.3	13.7	14.3	V
V_{CLAMP}	Output voltage while clamping(1)	TPS25952x	V_{IN} ≥ V_{OVC}, I_{OUT} = 10 mA		3.4	3.6	3.8	V
		TPS25953x			5.2	5.45	5.7	V
		TPS25954x			13	13.55	14.1	V
t_{OVC}	Output clamp response time(1)	TPS25952x/3x/4x	I_{OUT} = 4 A			5		µs
			I_{OUT} = 100 mA			10		µs
OUTPUT CURRENT LIMIT AND MONITOR (ILM)								
G_{IMON}	Current monitor gain as measured on ILM pin (I_{ILM} / I_{OUT})	I_{OUT} = 4 A			254	276	299	µA/A
		I_{OUT} = 1 A			249	276	304	µA/A
I_{LIMIT}	I_{OUT} Current limit(2)	R_{ILM} = 487 Ω			3.87	4.17	4.42	A
		R_{ILM} = 1780 Ω			1.09	1.17	1.24	A
		R_{ILM} = 4420 Ω(3)			0.46	0.49	0.52	A
		R_{ILM} = Open (Single Point Failure Test IEC 62368-1)				0		A
I_{CB}	I_{OUT} Circuit Breaker Threshold during R_{ILM} Short condition	R_{ILM} = Short to GND (Single Point Failure Test IEC 62368-1)				3		A
t_{LIM}	Current limit response time(2)	I_{OUT} > I_{LIMIT} + 20% to I_{OUT} ≤ I_{LIMIT}				250		µs
t_{SC}	Short circuit response time(4)	I_{OUT} > I_{SC} to I_{OUT} ≤ I_{LIMIT}				5		µs
ON-RESISTANCE (IN - OUT)								
R_{ON}	ON state resistance	V_{IN} = 4 V to 18 V	T_J = 25°C			34	37	mΩ
			T_J = –40°C to 85°C				47	mΩ
			T_J = –40°C to 125°C				53	mΩ
		V_{IN} = 2.7 V to 4 V	T_J = 25°C			36	40	mΩ
			T_J = –40°C to 85°C				51	mΩ
			T_J = –40°C to 125°C				58	mΩ

(1) Refer to Fig 49
(2) Refer to Fig 50
(3) Guaranteed by design and characterization. Not tested at production.
(4) Refer to Fig 52

Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V for TPS25954x/7x, V_{IN} = 5 V for TPS25953x, V_{IN} = 3.3 V for TPS25952x, V_{EN} = 5 V (= 0 V for TPS2595x3 only) , R_{ILM} = 487 Ω , C_{dVdT} = Open, OUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO) - TPS2595x0/1/5						
I_{EN}	EN/UVLO pin leakage current		–0.1		0.1	µA
$V_{UVLO(R)}$	Undervoltage lockout threshold	V_{EN} rising	1.13	1.2	1.27	V
$V_{UVLO(F)}$		V_{EN} falling	1.03	1.1	1.17	V
$\overline{EN}$ / OVERVOLTAGE LOCKOUT ($\overline{EN}$/OVLO) - TPS2595x3						
I_{EN}	$\overline{EN}$/OVLO pin leakage current		–0.1		0.1	µA
$V_{OVLO(R)}$	Overvoltage lockout threshold	V_{EN} rising	1.13	1.2	1.27	V
$V_{OVLO(F)}$		V_{EN} falling	1.03	1.1	1.17	V
t_{OVLO}	Overvoltage lockout response time	V_{EN} > V_{OVLO} to $\overline{FLT}$ ↓		3		µs
FAULT INDICATION ($\overline{FLT}$) - TPS2595x0/1/3						
R_{FLTB}	$\overline{FLT}$ pin resistance	$\overline{FLT}$ ↓		12		Ω
I_{FLTB}	$\overline{FLT}$ pin leakage current	V_{EN} = 2 V, V_{FLTB} = 0 V to 6 V	–0.1		0.1	µA
QUICK OUTPUT DISCHARGE (QOD) - TPS2595x5						
R_{QOD}	QOD effective resistance	IN connected to EN, OUT connected to QOD, EN↓ to 1V		19		Ω
OVERTEMPERATURE PROTECTION (TSD)						
TSD	Thermal shutdown	T_J Rising		157		°C
TSD_{HYS}	Thermal shutdown hysteresis	T_J Falling		5		°C
$t_{TSD,RST}$	Thermal Shutdown Auto-Retry Interval	TPS2595x1/3/5 — Device Enabled and T_J < TSD - TSD_{HYS}		93		ms

7.6 Switching Characteristics

Typical Values are taken at T_J = 25°C unless specifically noted otherwise. R_{OUT} = 100 Ω, C_{OUT} = 1 µF

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 3300pF	UNIT
SR_{ON}	Output Rising slew rate	3.3 V	16.3	10.0	V/ms
		5 V	21.9	11.6	
		12 V	38.2	12.4	
$t_{D,ON}$	Turn on delay	3.3 V	147	254	µs
		5 V	149	289	
		12 V	153	335	
t_R	Rise time	3.3 V	157	259	µs
		5 V	179	349	
		12 V	248	763	
$t_{D,OFF}$	Turn off delay	3.3 V	11.6	11.6	µs
		5 V	11.3	11.5	
		12 V	11.0	11.4	

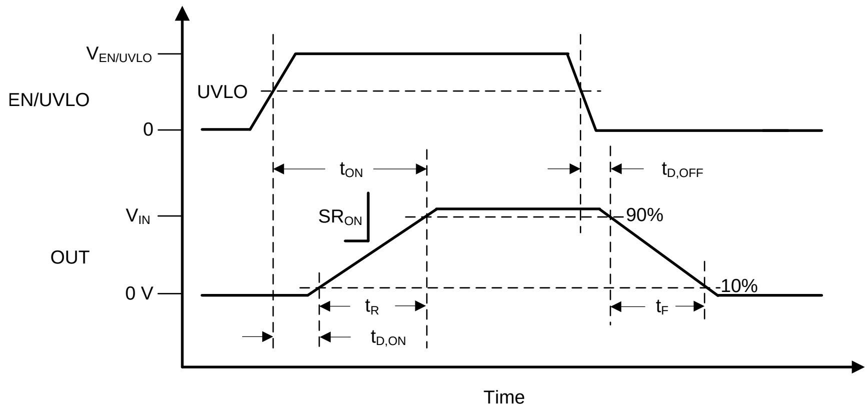


图 1. TPS2595x0, TPS2595x1, TPS2595x5 Switching Times

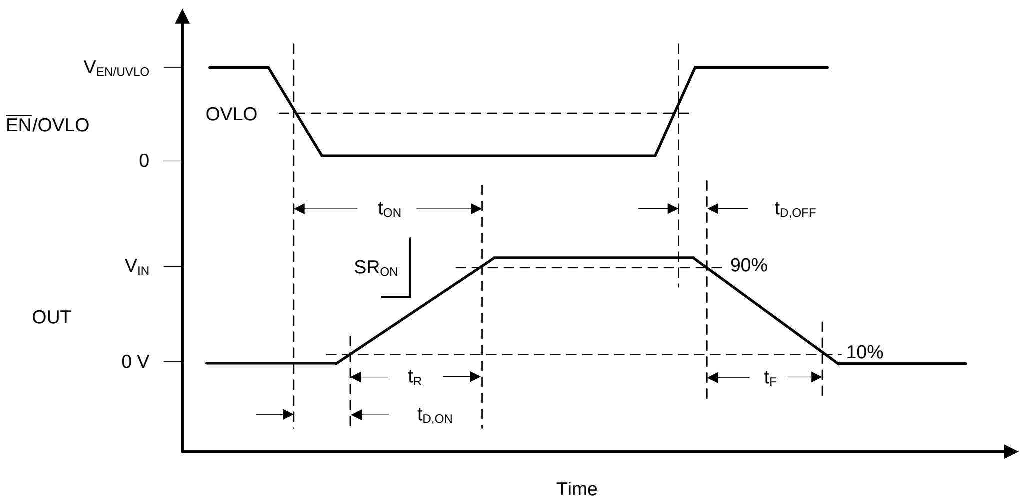
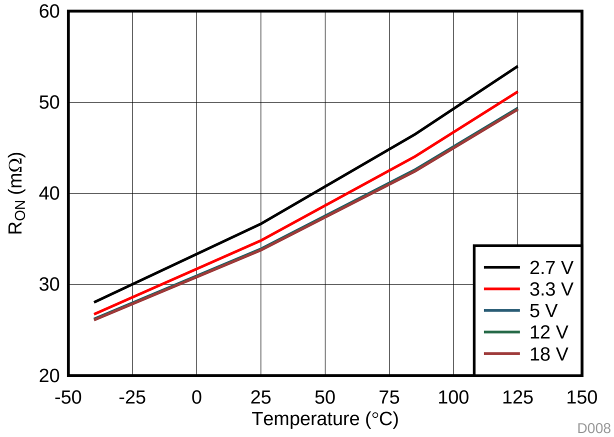


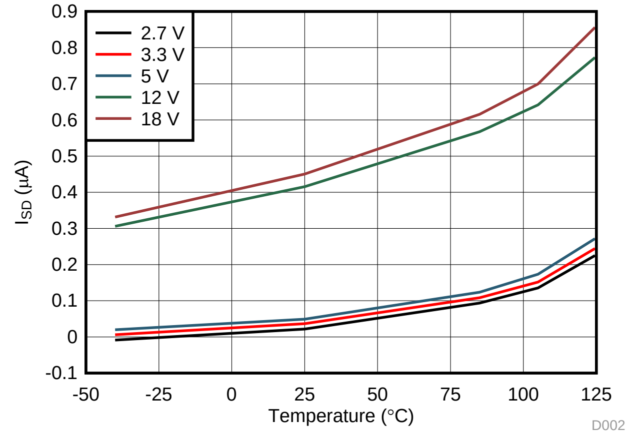
图 2. TPS2595x3 Switching Times

7.7 Typical Characteristics



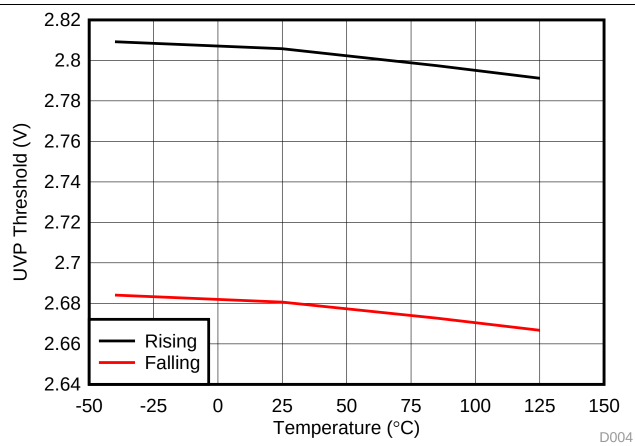
I_{OUT} = 0.5A , Different Input Voltages

图 3. On-resistance vs Temperature



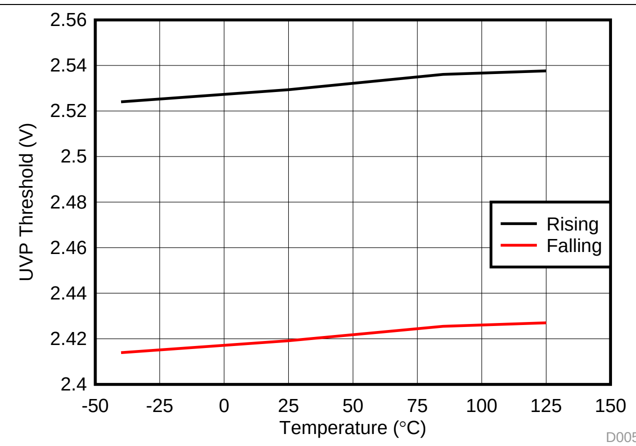
TPS2595x0/1/5, EN=GND, OUT=Open, Different Input Voltages

图 4. Shutdown Current vs Temperature



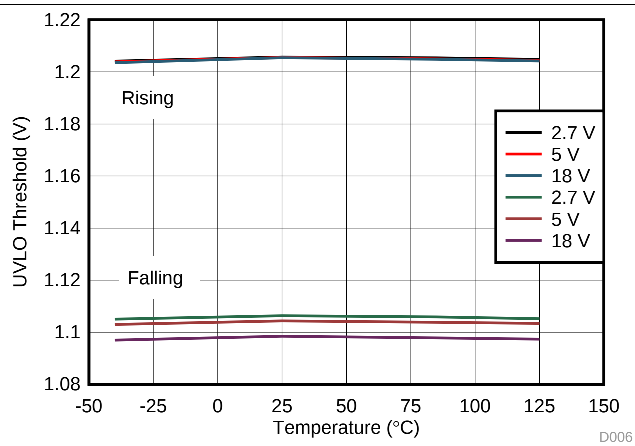
TPS2595x5

图 5. UVP Threshold vs Temperature



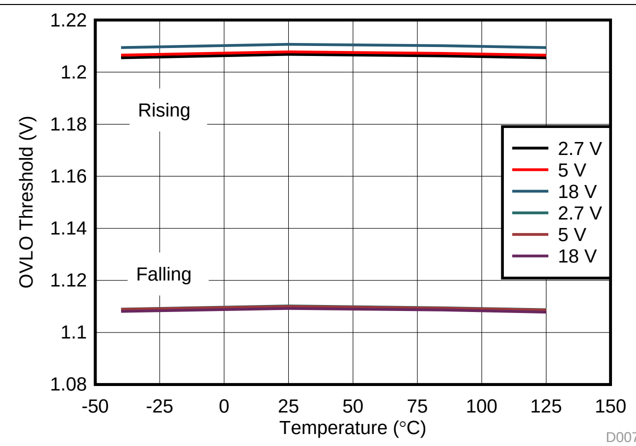
TPS2595x0/1/3

图 6. UVP Threshold vs Temperature



TPS2595x0/1/5, Different Input Voltages

图 7. UVLO Threshold vs Temperature



TPS259573, Different Input Voltages

图 8. OVLO Threshold vs Temperature

Typical Characteristics (接下页)

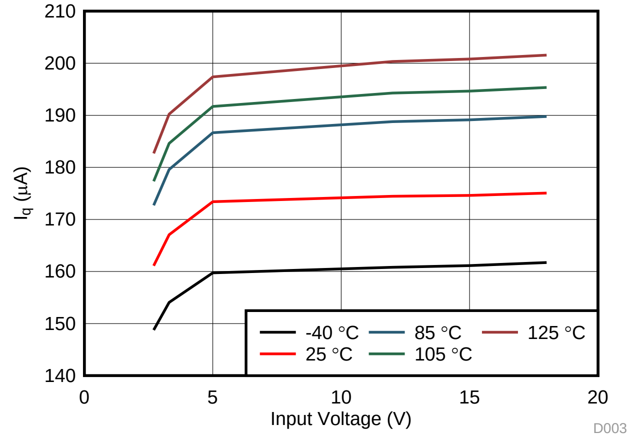
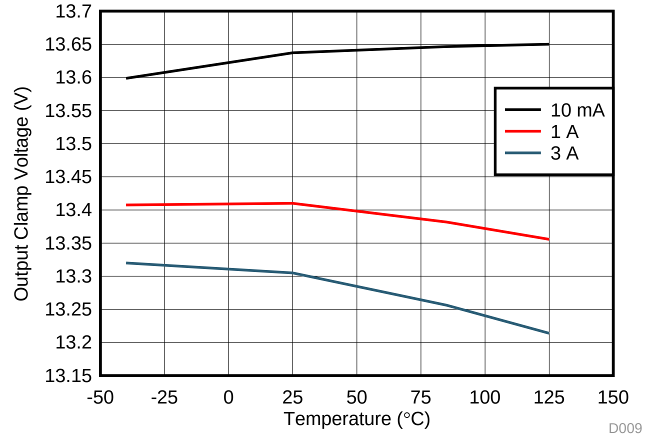
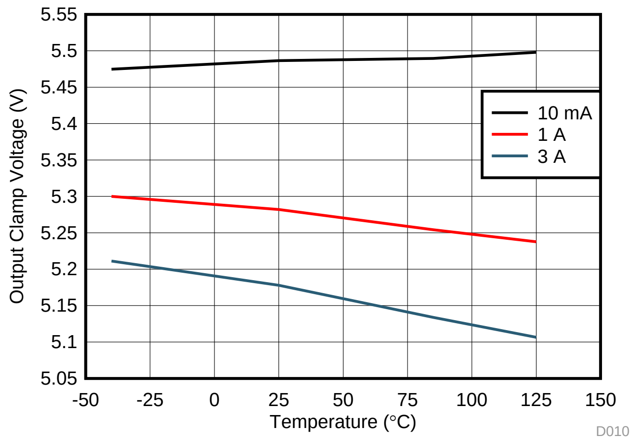


图 9. Quiescent Current vs Input Voltage



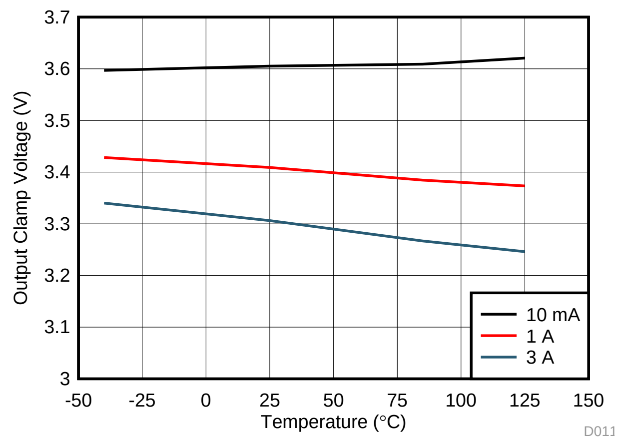
TPS25954x, Different Output Load Currents

图 10. OVC Threshold vs Temperature



TPS25953x, Different Output Load Currents

图 11. OVC Threshold vs Temperature



TPS25952x, Different Output Load Currents

图 12. OVC Threshold vs Temperature

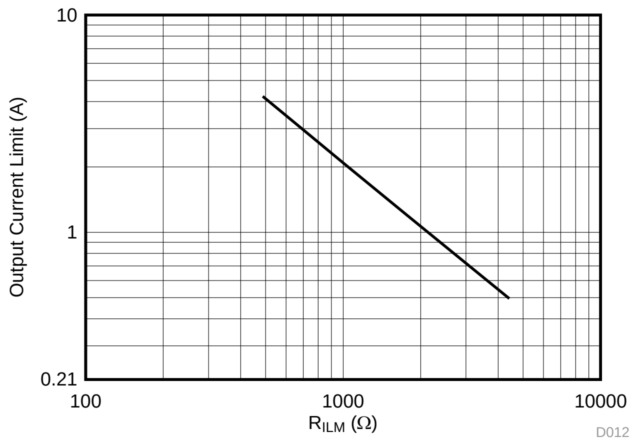
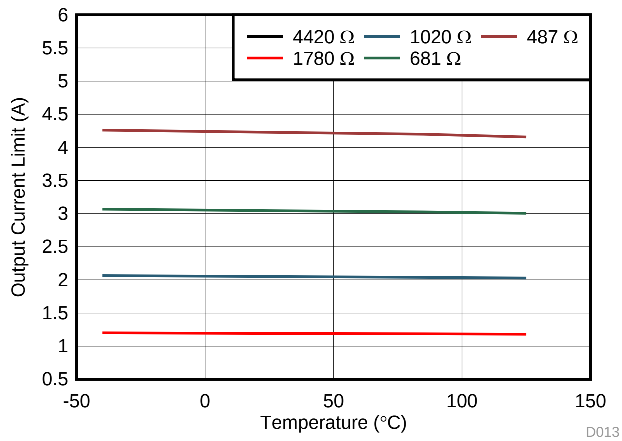


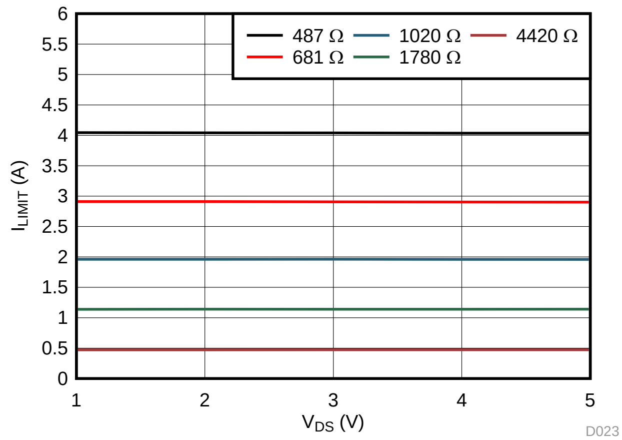
图 13. Output Current Limit (I_{LIMIT}) vs R_{ILM}



V_{IN} = 12V, Different R_{ILM} values

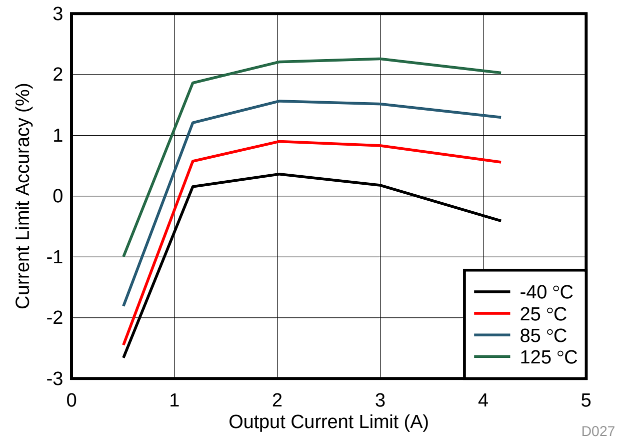
图 14. Output Current Limit (I_{LIMIT}) vs Temperature

Typical Characteristics (接下页)



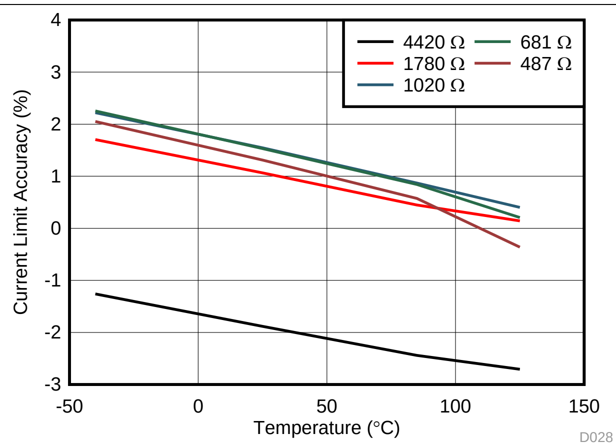
Different R_{ILM} values

图 15. Output Current Limit vs V_{DS}



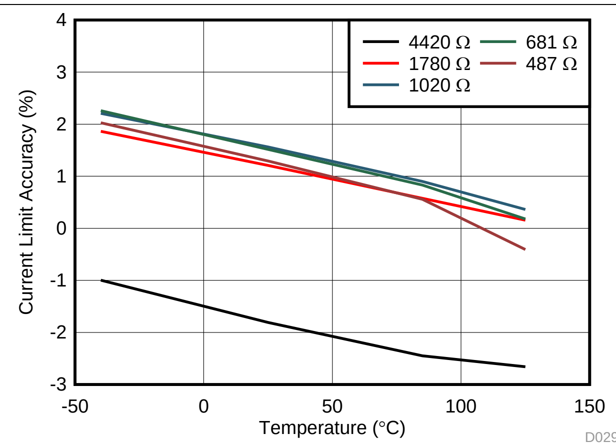
V_{IN} = 5 V

图 16. Output Current Limit Accuracy vs Output Current Limit



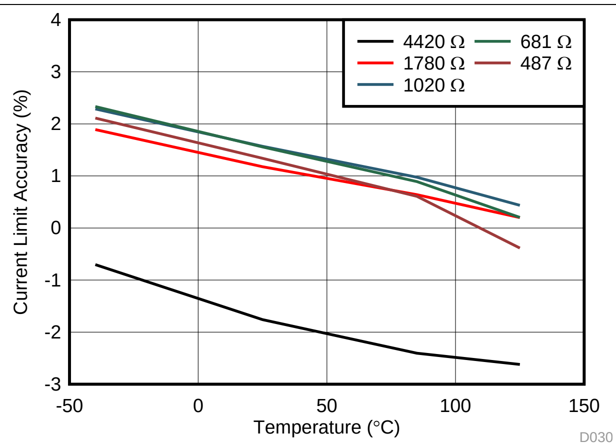
V_{IN} = 3.3 V, Different R_{ILM} values

图 17. Output Current Limit Accuracy vs Temperature



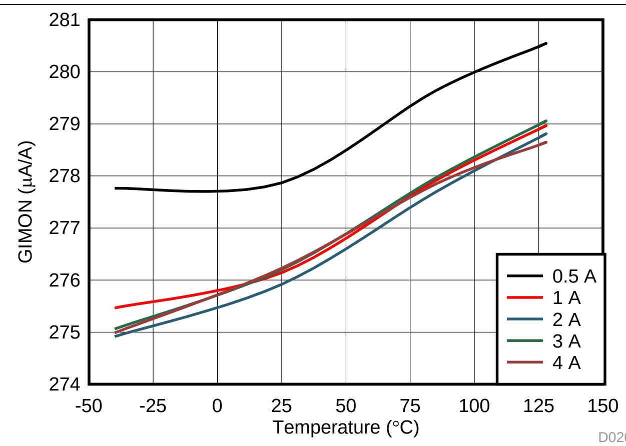
V_{IN} = 5 V, Different R_{ILM} values

图 18. Output Current Limit Accuracy vs Temperature



V_{IN} = 12 V, Different R_{ILM} values

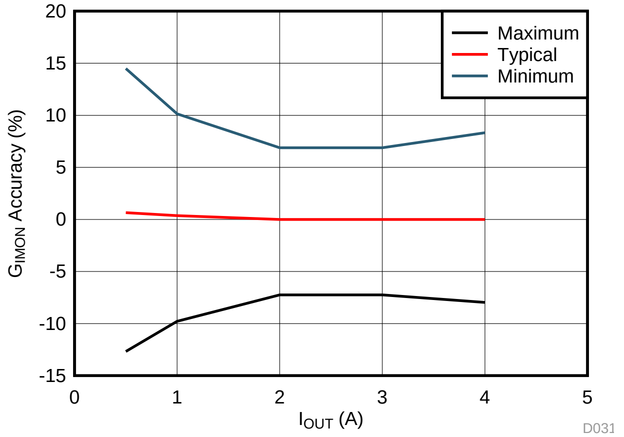
图 19. Output Current Limit Accuracy vs Temperature



Different Output Load Currents

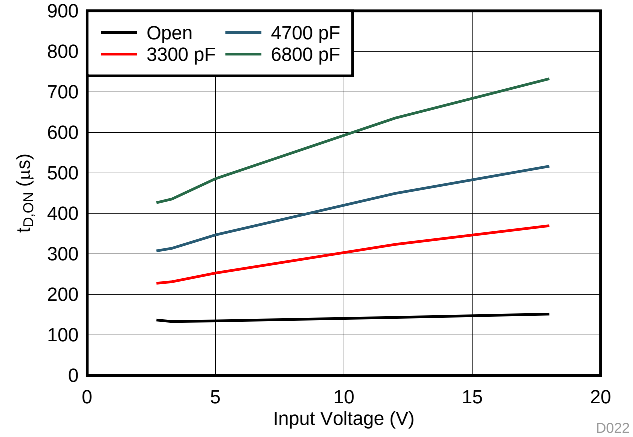
图 20. Load Current Monitor Gain vs Temperature

Typical Characteristics (接下页)



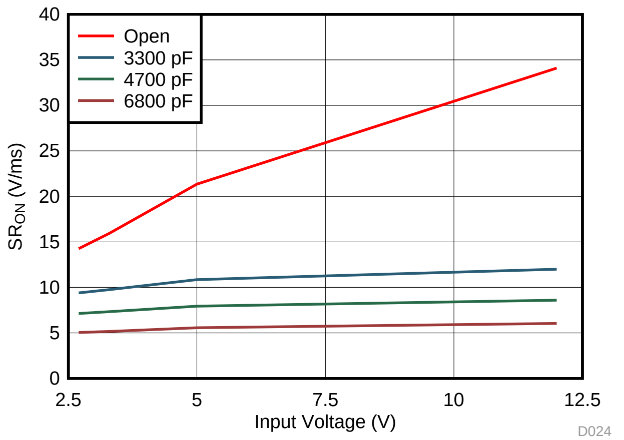
Normalized to reference value of G_{IMON} = 276uA/A

图 21. Load Current Monitor Gain Accuracy vs Load Current



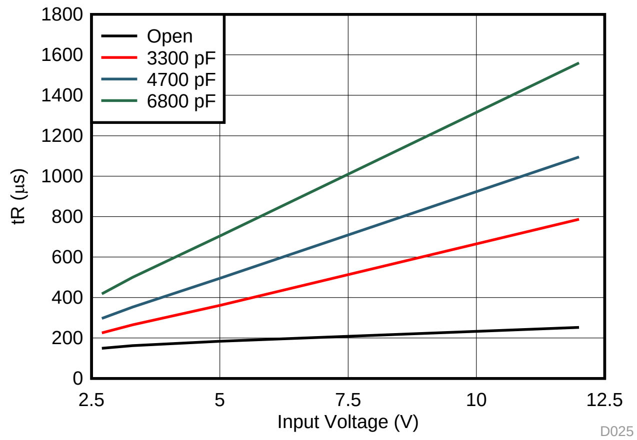
Different C_{dVdt} values

图 22. Turn on Delay vs Input Voltage



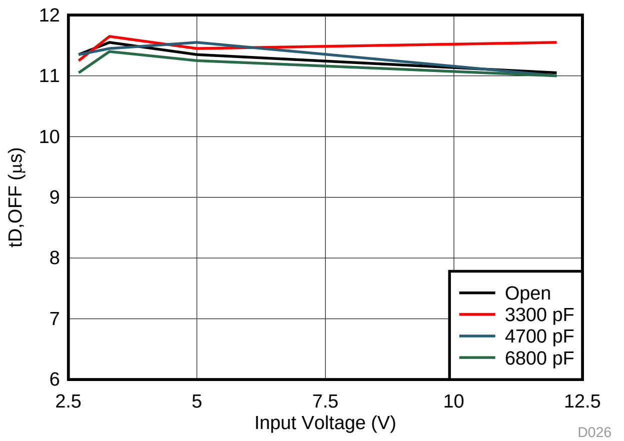
Different C_{dVdt} values

图 23. ON Slew Rate vs Input Voltage



Different C_{dVdt} values

图 24. Rise Time vs Input Voltage



Different C_{dVdt} values

图 25. Turn OFF Delay vs Input Voltage

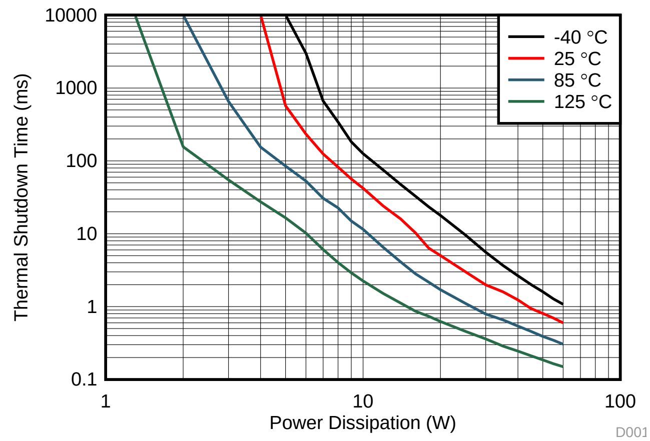
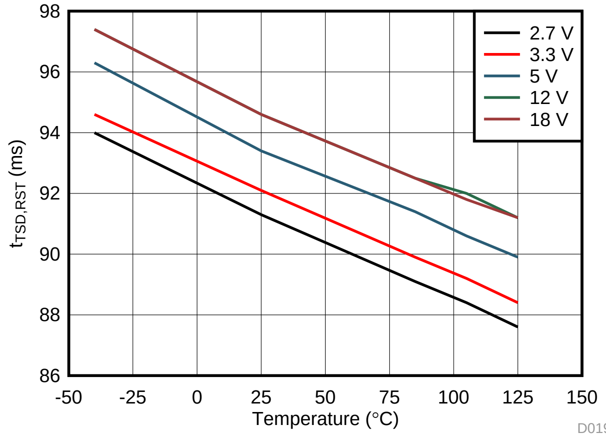


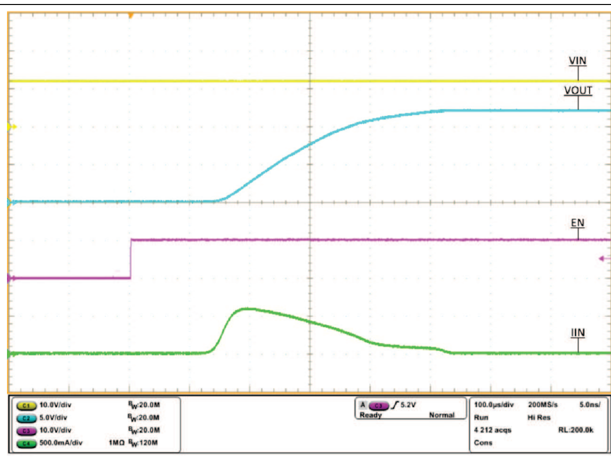
图 26. Thermal Shutdown Time vs Power Dissipation

Typical Characteristics (接下页)



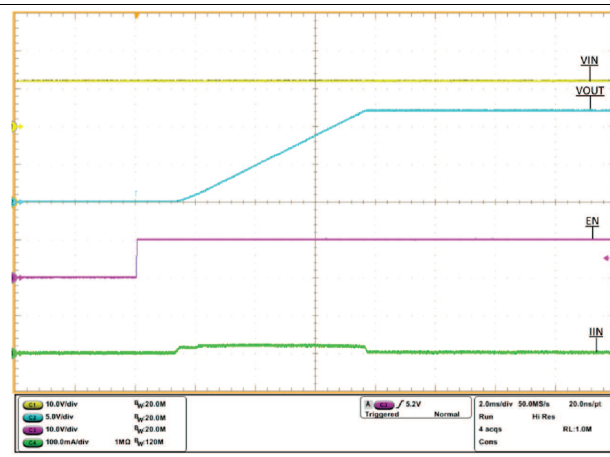
TPS2595x1/3/5, Different Input Voltages

图 27. Thermal Shutdown Auto-Retry Interval vs Temperature



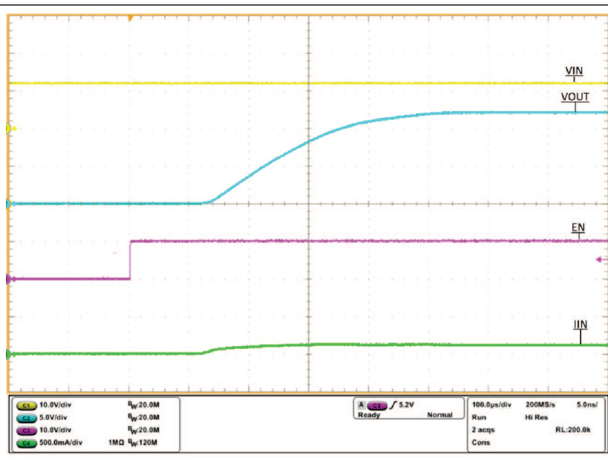
V_{IN} = 12 V, C_{OUT} = 10 µF, R_{ILM} = 487 Ω, V_{EN} = 5 V

图 28. Output Voltage Ramp and Inrush Current at Start Up, C_{dVdT} = Open



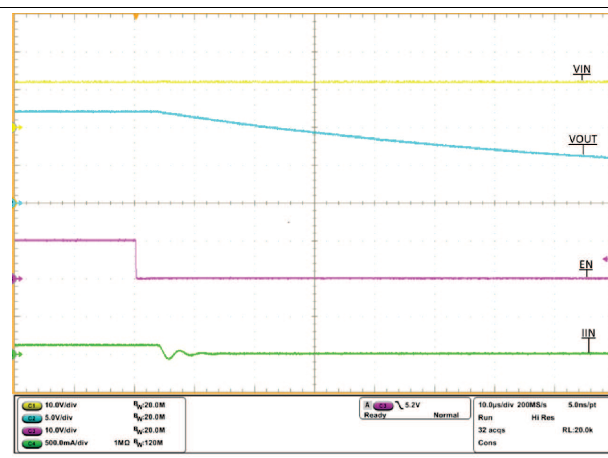
V_{IN} = 12 V, C_{OUT} = 10 µF, R_{ILM} = 487 Ω, V_{EN} = 5 V

图 29. Output Voltage Ramp and Inrush Current at Start Up, C_{dVdT} = 22 nF



V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, R_{OUT} = 100 Ω

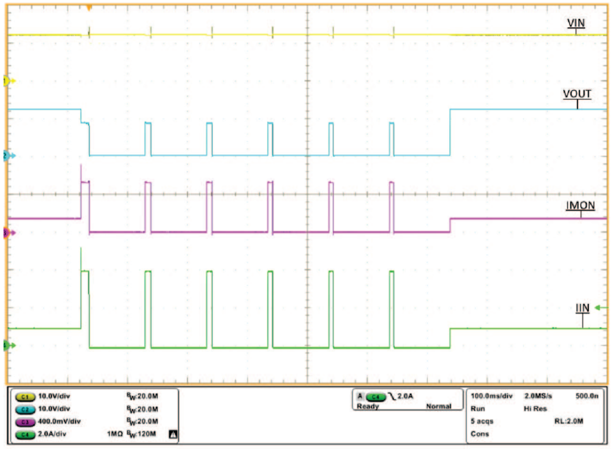
图 30. Turn ON Delay



V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, R_{OUT} = 100 Ω

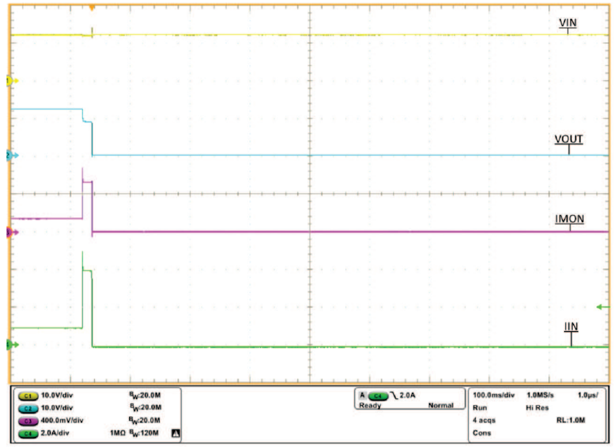
图 31. Turn OFF Delay

Typical Characteristics (接下页)



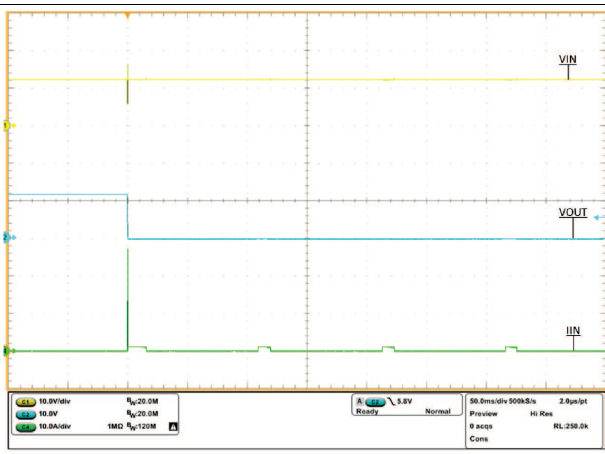
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, R_{OUT} varied from 12 Ω to 2 Ω to 12 Ω

图 32. TPS2595x1, TPS2595x3, TPS2595x5 OverCurrent Response



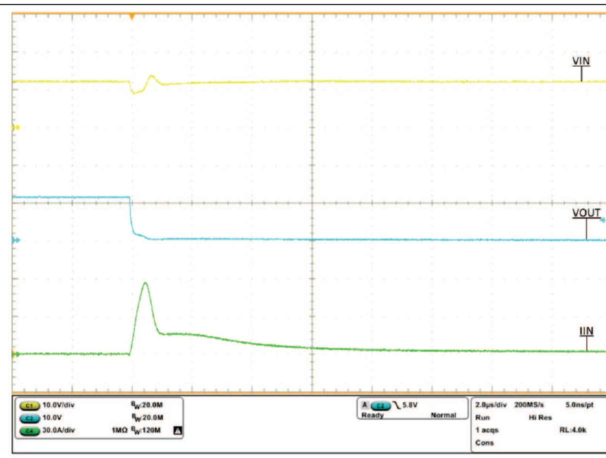
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, R_{OUT} varied from 12 Ω to 2 Ω to 12 Ω

图 33. TPS2595x0 Overcurrent Response



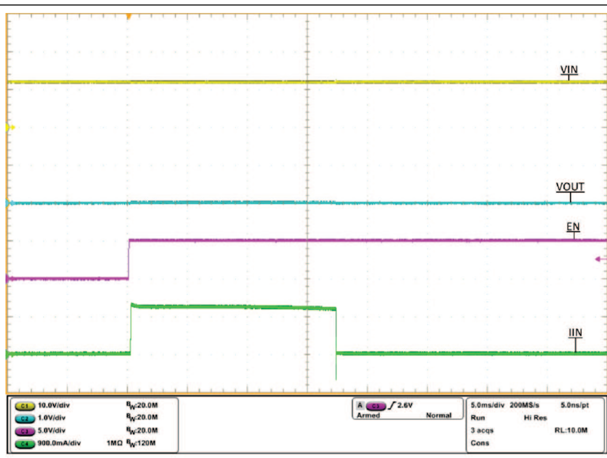
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

图 34. Output Hot Short to GND Response



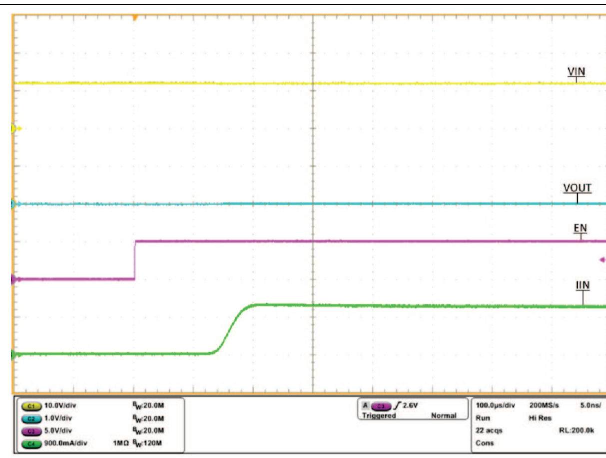
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

图 35. Output Hot Short to GND Response (Zoomed In)



V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

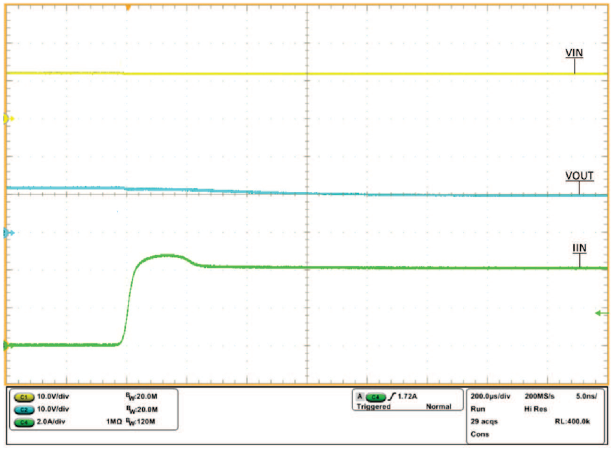
图 36. Wake Up With Output Short to GND



V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

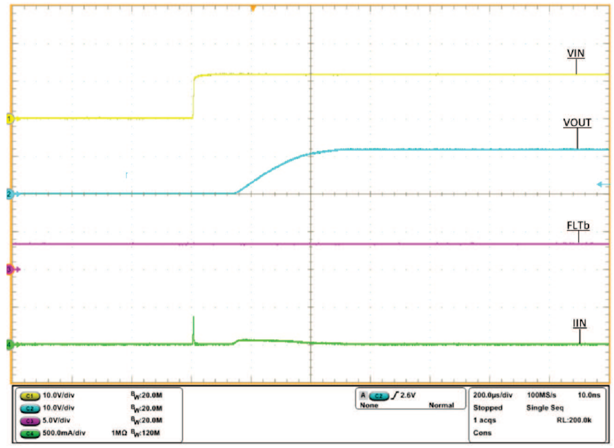
图 37. Wake Up With Output Short to GND (Zoomed In)

Typical Characteristics (接下页)



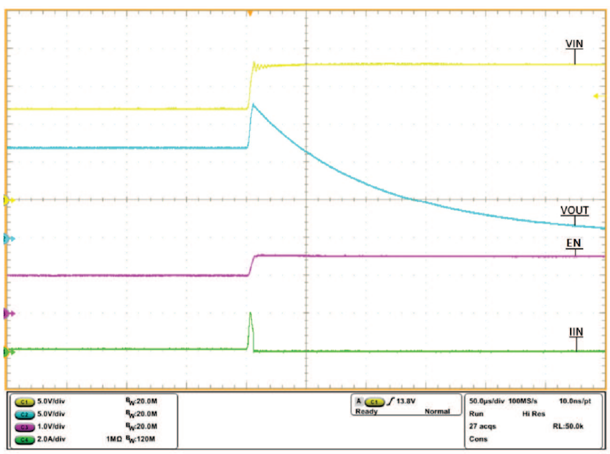
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, I_{OUT} stepped from 4 A to 4.8 A

图 38. Output Load Transient Response



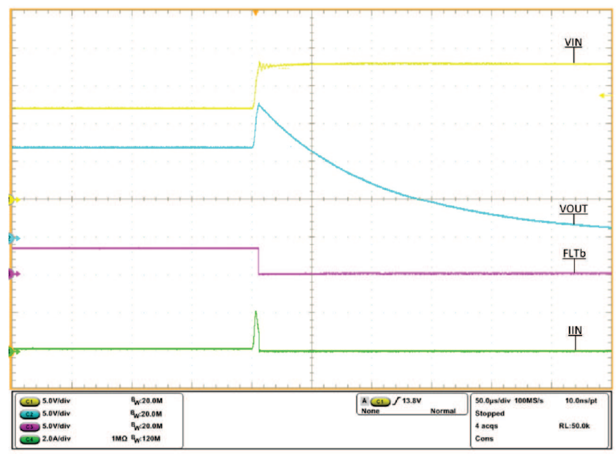
V_{IN} = 12 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ

图 39. Hot Plug Response



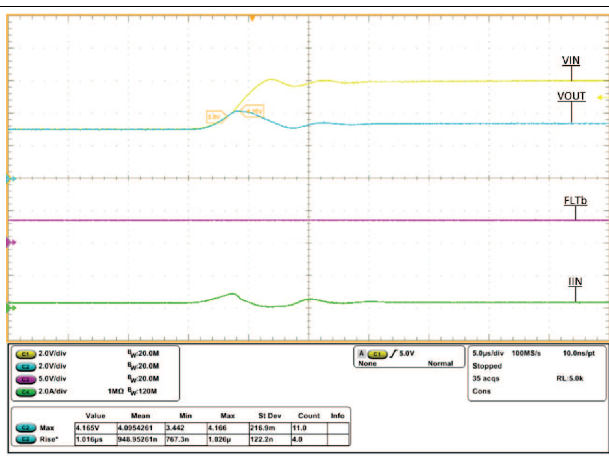
V_{IN} stepped from 12 V to 18 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ, R_{OUT} = 100 Ω

图 40. TPS259573 Overvoltage Lockout Response



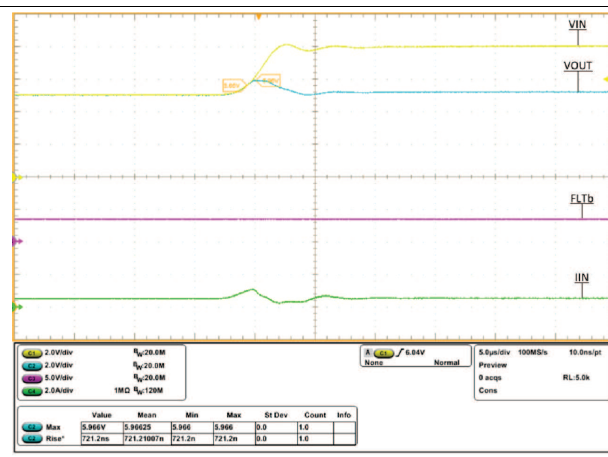
V_{IN} stepped from 12 V to 18 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ, R_{OUT} = 100 Ω

图 41. TPS259573 Overvoltage Lockout $\overline{FLT}$ Response



V_{IN} stepped from 3 V to 6 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$= 3.3 V through 10 kΩ, R_{OUT} = 10 Ω

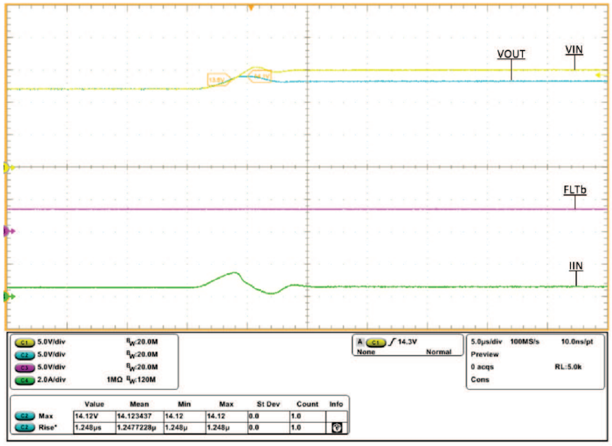
图 42. TPS25952x Overvoltage Clamp Response



V_{IN} stepped from 5 V to 8 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ, R_{OUT} = 10 Ω

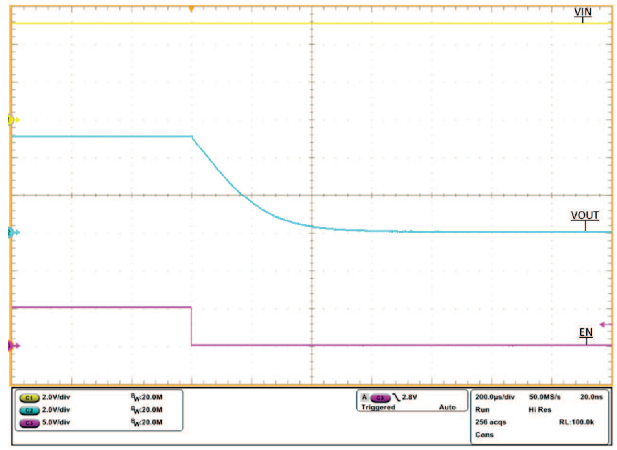
图 43. TPS25953x Overvoltage Clamp Response

Typical Characteristics (接下页)



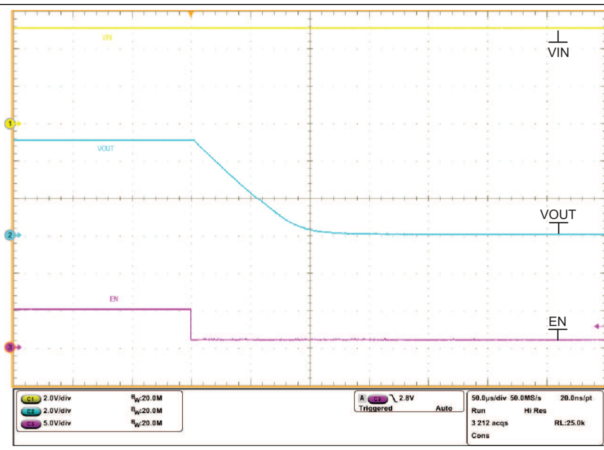
V_{IN} Stepped from 12 V to 15 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω, $\overline{FLT}$ = 3.3 V through 10 kΩ, R_{OUT} = 20 Ω

图 44. TPS25954x Overvoltage Clamp Response



V_{IN} = 5 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

图 45. TPS2595x5 Quick Output Discharge, EN stepped from 5 V to 0 V



V_{IN} = 5 V, C_{OUT} = 1 µF, R_{ILM} = 487 Ω

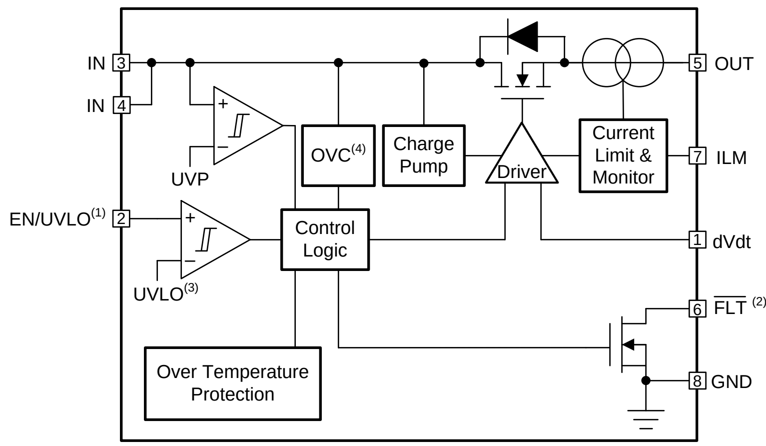
图 46. TPS2595x5 Quick Output Discharge, EN stepped from 5 V to 1 V

8 Detailed Description

8.1 Overview

The TPS2595xx devices are integrated eFuse that are used to manage load voltage and load current. The device provides various factory programmed settings and user manageable settings, which allow device configuration for handling different transient and steady state supply and load fault conditions, thereby protecting the input supply and the downstream circuits connected to the device. The device also uses an in-built thermal shutdown mechanism to protect itself during these fault events.

8.2 Functional Block Diagram



(1) For TPS2595x3, this pin is $\overline{EN}$/OVLO
(2) For TPS2595x5, this pin is QOD
(3) For TPS2595x3, this voltage is OVLO
(4) This block is not available in the TPS25957x

8.3 Feature Description

8.3.1 Undervoltage Protection (UVP) and Undervoltage Lockout (UVLO)

All the TPS2595xx devices constantly monitor the input supply to ensure that the load is powered up only when the voltage is at a sufficient level. During the start-up condition, the device waits for the input supply to rise above a fixed threshold V_{UVP} before it proceeds to turn ON the FET. Similarly, during the ON condition, if the input supply falls below the UVP threshold, the FET is turned OFF. The UVP rising and falling thresholds are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The TPS2595x0, TPS2595x1, TPS2595x5 devices provide an user programmable UVLO mechanism to ensure that the load is powered up only when the voltage is at a sufficient level. This can be achieved by dividing the input supply and feeding it to the EN/UVLO pin. Whenever the voltage at the EN/UVLO pin falls below a threshold V_{UVLO}, the device turns OFF the FET. The FET is turned ON again when the voltage rises above the threshold. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

The user must choose the resistor divider values appropriately to map the desired input undervoltage level to the UVLO threshold of the part. See 图 47.

Feature Description (接下页)

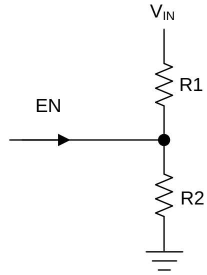


图 47. Undervoltage Lockout

$$V_{SUPPLY} = \frac{V_{UVLO} \times (R1 + R2)}{R2} \quad (1)$$

8.3.2 Overvoltage Protection

The TPS2595xx devices provide 2 ways to handle an input overvoltage condition.

8.3.2.1 Overvoltage Lockout (OVLO)

The TPS259573 device provides an user programmable OVLO mechanism to ensure that the supply to the load is cut off if the input supply voltage exceeds a certain level. This can be achieved by dividing the input supply and feeding it to the $\overline{EN}$/OVLO pin. Whenever the voltage at the $\overline{EN}$/OVLO pin rises above a threshold V_{OVLO}, the device turns OFF the FET. When the voltage at the $\overline{EN}$/OVLO pin falls below the threshold, the FET is turned ON again.

The user should choose the resistor divider values appropriately to map the desired input overvoltage level to the OVLO threshold of the part.

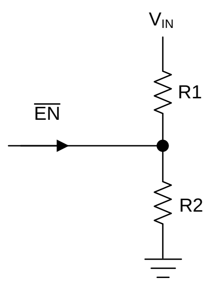


图 48. Overvoltage Lockout

8.3.2.2 Overvoltage Clamp (OVC)

The TPS25952x, TPS25953x, TPS25954x devices provide a mechanism to clamp the output voltage to a predefined level quickly if the input voltage crosses a certain threshold. This ensures the load is not exposed to high voltages on any overvoltage at the input supply, and lowers the dependency on external protection devices (such as TVS/Zener diodes) in this condition. Once the input supply voltage rises above the OVC threshold voltage V_{OVC}, the device responds by clamping the voltage to V_{CLAMP} within a very short response time t_{OVC}. As long as an overvoltage condition is present on the input, the output voltage will be clamped to V_{CLAMP}. When the input drops below the output clamp threshold V_{OVC}, the clamp releases the output voltage. See 图 49.

During the overvoltage clamp condition, there could be significant heat dissipation in the internal FET depending on the V_{IN} - V_{OUT} voltage drop and the current through the FET leading to a thermal shutdown if the condition persists for an extended period of time. In this case, the device would either stay latched-off or start a auto retry cycle as explained in the *Overtemperature Protection (OTP)* section.

Feature Description (接下页)

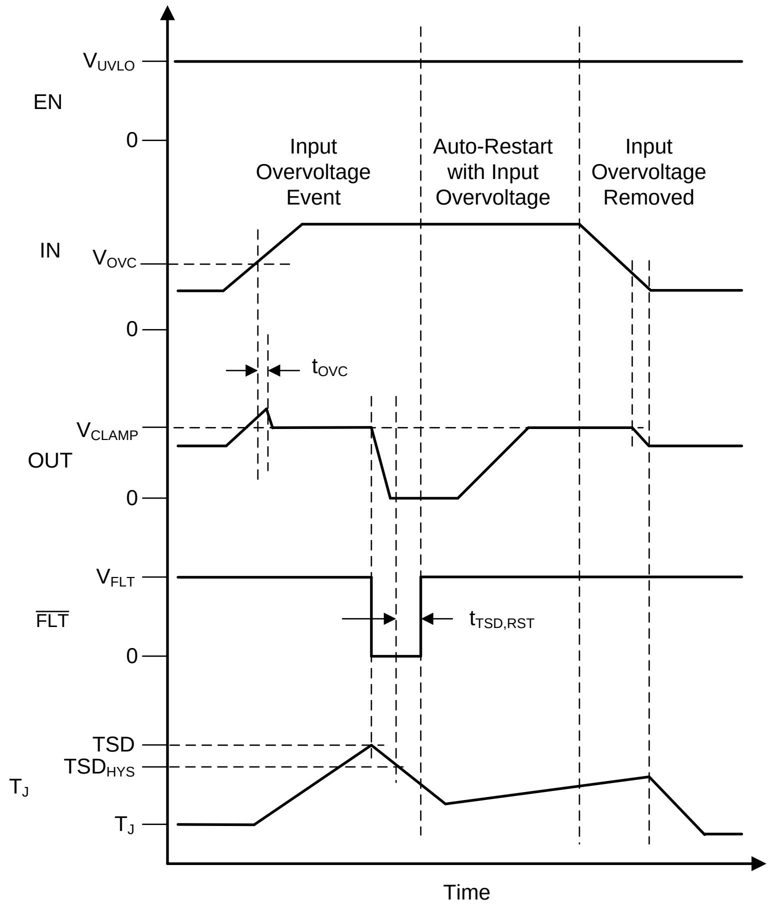


图 49. TPS2595xx Overvoltage Clamp Response (Auto-Retry)

Multiple device options are offered with different clamping voltage thresholds. See the *Device Comparison Table* for list of available voltage clamp options.

8.3.3 Inrush Current, Overcurrent and Short Circuit Protection

The TPS2595xx devices incorporates three levels of protection against overcurrent:

- Adjustable slew rate for inrush current control (dVdt).
- Active current limiting (I_{LIMIT}) for overcurrent protection.
- A fast short circuit limit (I_{SC}) to protect against hard short circuits.

8.3.3.1 Slew Rate and Inrush Current Control (dVdt)

The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. 公式 2 can be used to find the slew rate SR_{ON} required to limit the inrush current I_{INRUSH} for a given load capacitance C_{OUT}.

$$SR_{ON}\left(\frac{V}{ms}\right)=\frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{2}$$

For loads requiring a slower rising slew rate, a capacitance can be added to the dVdt pin to adjust the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using 公式 3.

Feature Description (接下页)

$$C_{dVdt}\,(pF) = \frac{42000}{SR_{ON}\left(\frac{V}{ms}\right)} \tag{3}$$

8.3.3.2 Active Current Limiting

The load current is monitored during start-up and normal operation. When the load current exceeds the current limit trip point I_{LIMIT} programmed by R_{ILM} resistor, the device regulates the current to the set limit I_{LIMIT} within t_{LIM}. The device exits current limiting when the load current falls below limit. 公式 4 can be used to find the R_{ILM} value for a desired current limit.

$$R_{ILM} = \frac{2000}{(I_{LIMIT} - 0.04)} \tag{4}$$

In the current limiting state, the output voltage drops resulting in increased power dissipation in the internal FET leading to a thermal shutdown if the condition persists for an extended period of time. In this case, the device either stays latched-off or starts an auto retry cycle as explained in the *Overtemperature Protection (OTP)* section.

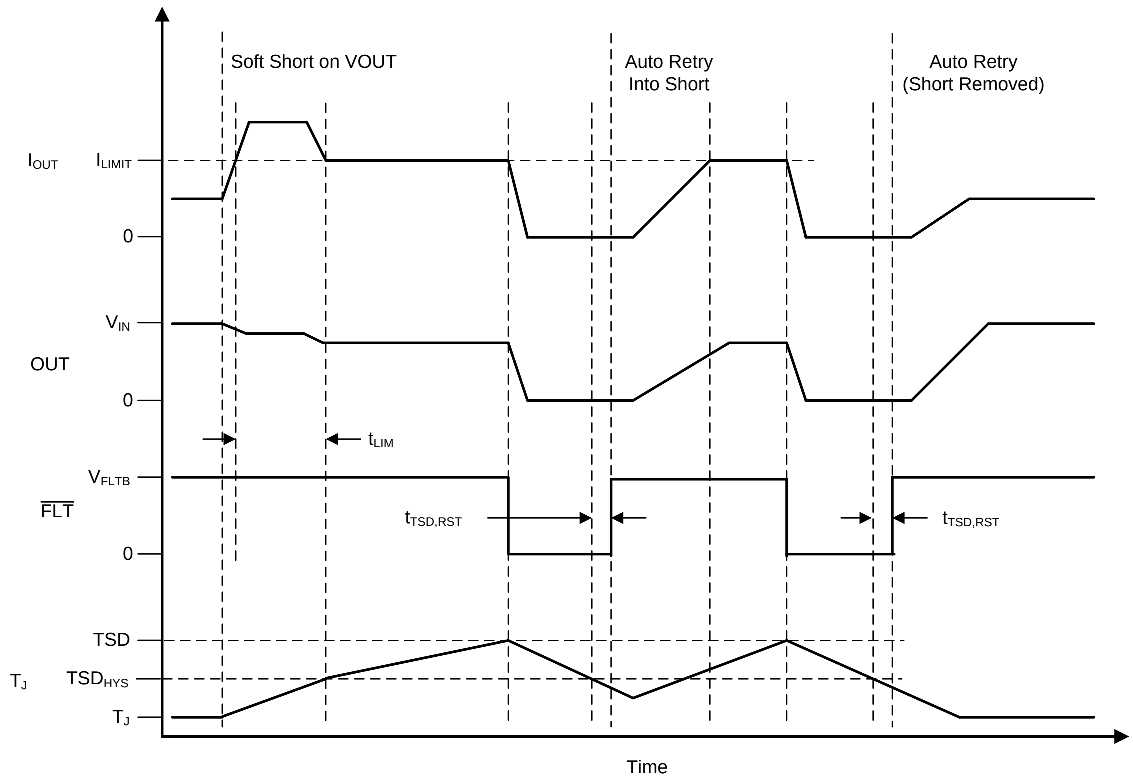


图 50. TPS2595x1, TPS2595x3, TPS2595x5 Overcurrent Response (Auto-Retry)

Feature Description (接下页)

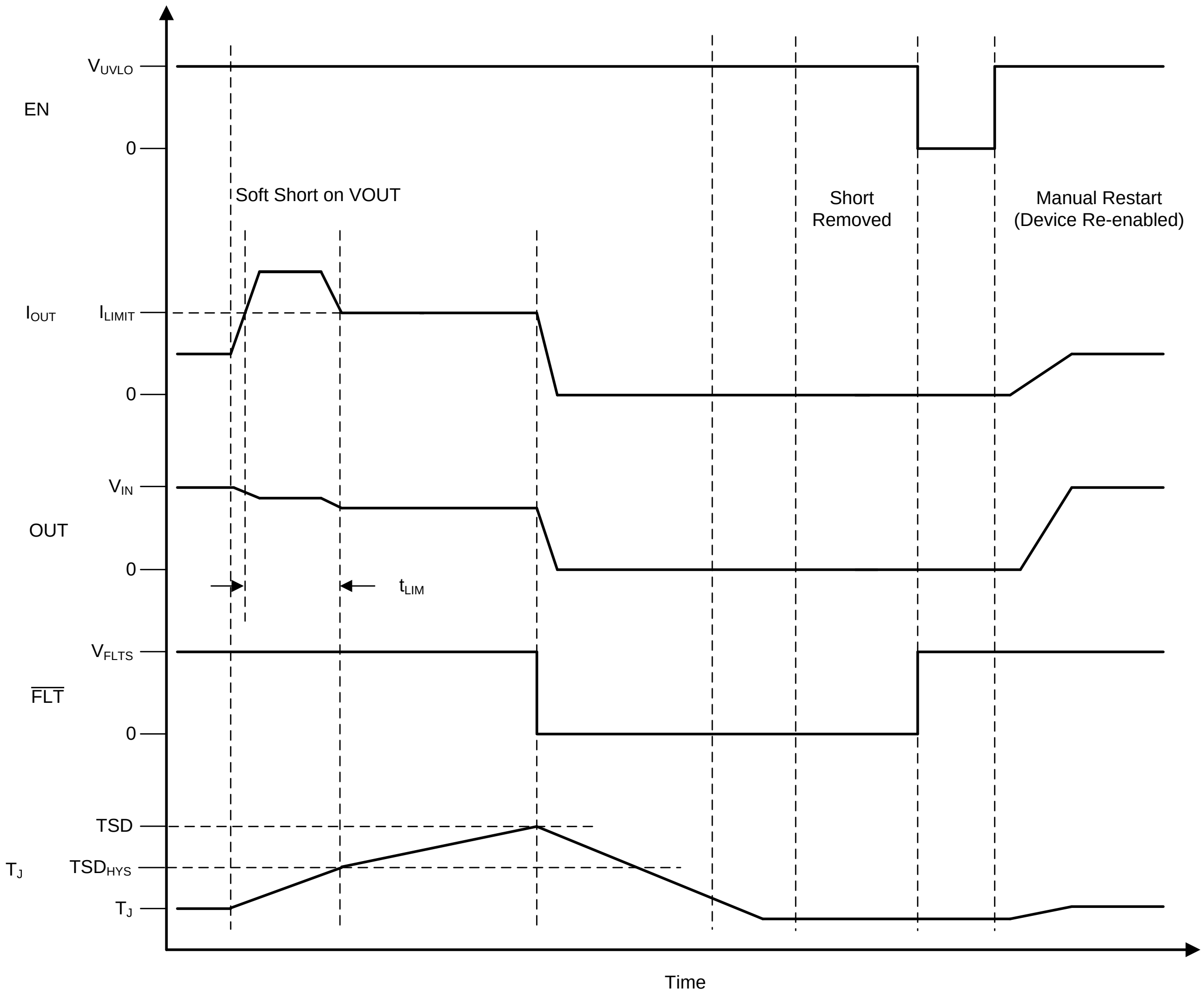


图 51. TPS2595x0 Overcurrent Response (Latch-Off)

8.3.3.3 Short Circuit Protection

The current through the device increases very rapidly during a transient short circuit event. The short circuit threshold I_{SC} is adjusted based on the selected current limit. When a short circuit is detected, the device quickly limits the current to I_{LIMIT}. The device stops limiting the current once the load current falls below the programmed I_{LIMIT} threshold. See 图 52.

The output voltage drops in the current limiting state, resulting in increased power dissipation in the internal FET and leads to a thermal shutdown if the condition persists for an extended period of time. In this case, the device either stays latched-off or starts an auto retry cycle as explained in the *Overtemperature Protection (OTP)* section.

Feature Description (接下页)

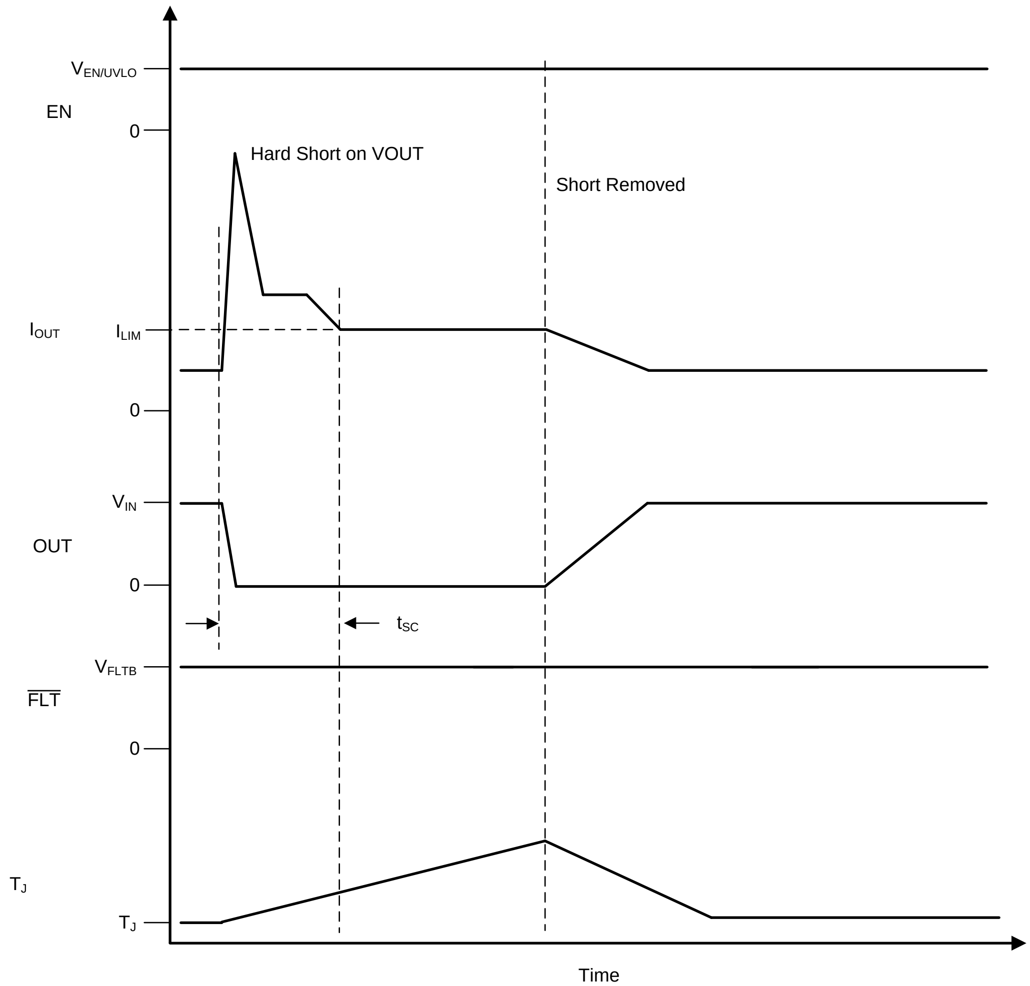


图 52. TPS2595xx Short Circuit Response

8.3.4 Overtemperature Protection (OTP)

Thermal shutdown occurs when the junction temperature T_J exceeds TSD. When the TPS2595x0 detects a thermal overload, it shuts down and remains latched off until the device is re-enabled or power cycled. When the TPS2595x1, TPS2595x3, TPS2595x5 devices detects a thermal overload, it remains off until the T_J decreases by TSD_{HYS} and then waits for an additional delay of $t_{TSD,RST}$ after which it automatically retries to turn on if it is still enabled. See 表 1.

表 1. TPS2595xx Thermal Shutdown

Device	Enter TSD	Exit TSD
TPS2595x0 (Latch-off)	$T_J \geq$ TSD	T_J < TSD and Device Power Cycled or re-enabled using EN/UVLO pin
TPS2595x1, TPS2595x3, TPS2595x5 (Auto-retry)	$T_J \geq$ TSD	T_J < TSD – TSD_{HYS} and $t_{TSD,RST}$ Timer Expired

8.3.5 Fault Indication ($\overline{FLT}$)

表 2 summarizes the protection response to various fault conditions.

表 2. TPS2595x0, TPS2595x1, TPS2595x3 Fault Summary

EVENT / FAULT	PROTECTION RESPONSE	$\overline{FLT}$ INDICATION
Overtemperature	Shutdown	Yes
Overvoltage	Output Voltage Clamp (OVC) (TPS25952x,TPS25953x,TPS25954x only)	No
Overvoltage	Shutdown (OVLO) (TPS259573 only)	Yes
Undervoltage	Shutdown (UVP or UVLO)	No
Overcurrent	Current Limiting	No
Short circuit	Current Limiting	No
ILM pin open	Shutdown	No
ILM pin short	Shutdown If $I_{OUT} > I_{CB}$	Yes If $I_{OUT} > I_{CB}$

When the TPS2595x0, TPS2595x1, TPS2595x3 devices are turned off as a result of a fault as described in the table above, the $\overline{FLT}$ pin is pulled low.

All faults will be cleared if the device loses power or if it is re-enabled using the EN/UVLO (or $\overline{EN}$/OVLO) pin.

8.3.6 Quick Output Discharge (QOD)

Some applications require the output capacitor to be discharged quickly when the eFuse is turned off. This prevents any unpredictable behavior from the downstream devices as the capacitor discharges slowly. The TPS2595x5 device provides a Quick Output Discharge feature that can be enabled by connecting OUT pin to QOD pin. An internal FET provides a fast discharge path for the output capacitor resulting in the OUT voltage falling to 0 V in a short time. The FET initially operates in saturation region and provides a constant current discharge. After the FET enters linear region, it offers a discharge path similar to a resistor.

It is possible to model this as a simple equivalent resistance, which would discharge a given capacitor charged to a given voltage in the same time as the overall discharge circuit. This parameter is specified as the effective QOD resistance R_{QOD} for the device. It takes a time equivalent to 5 time constants ($\tau = R \times C$) to discharge a capacitor by 99.3%. For example, with an effective QOD resistance of 19 Ω, the time taken to discharge a 100-µF capacitor from 5 V to 35 mV can be calculated as in 公式 5.

$$t_{Discharge} = 5 \times 19\ \Omega \times 100\ \mu F = 9.5\ ms \quad (5)$$

8.4 Device Functional Modes

The features of the device depend on the operating mode.

8.4.1 Enable and Fault Pin Functional Mode 1: Single Device, Self-Controlled

In this mode of operation, the device is enabled by the V_{IN} voltage without the need of an external processor to drive the ENABLE pin. The $\overline{FLT}$ pin is optionally monitored by an external host. See 图 53.

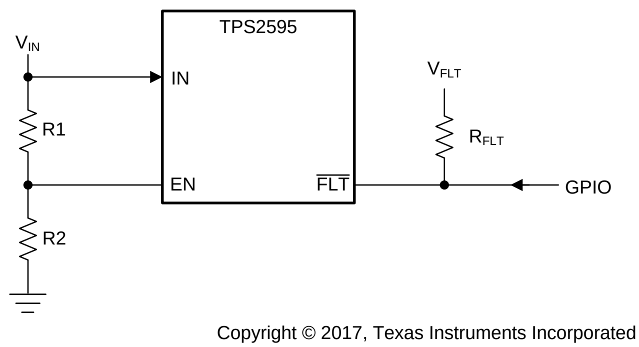


图 53. Single Device, Self-Controlled

8.4.2 Enable and Fault Pin Functional Mode 2: Single Device, Host-Controlled

In this mode of operation, the device enable pin is driven by an external host. The pin can be driven directly from a GPIO without the need for any glue logic. The $\overline{FLT}$ pin is optionally monitored by the host. See 图 54.

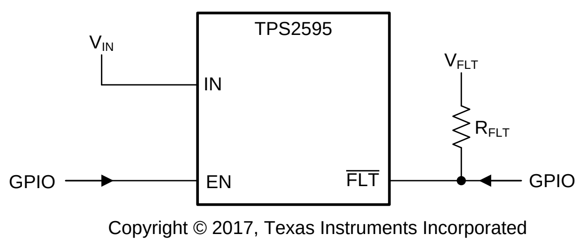


图 54. Single Device, Host-Controlled

8.4.3 Enable and Fault Pin Functional Mode 2: Multiple Devices, Self-Controlled

In this mode of operation, the devices are self-controlled (no host present). The EN and $\overline{FLT}$ pins are shorted together, and connected with up to three total devices as shown in 图 55. In this configuration, when any one of the TPS2595xx devices detects a fault, it automatically disables the other TPS2595xx devices in the system.

注

This configuration is only applicable to the Active High Enable variants TPS2595x0, TPS2595x1, TPS2595x5.

Device Functional Modes (接下页)

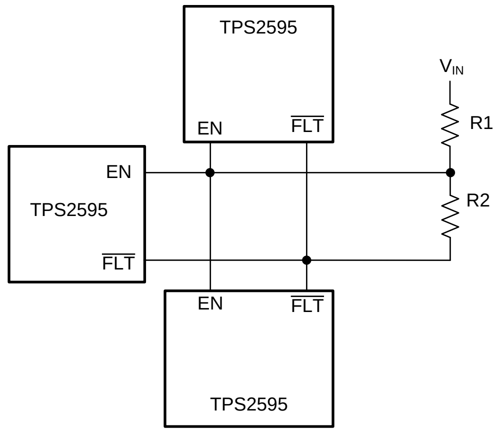


图 55. Multiple Devices, Self-Controlled

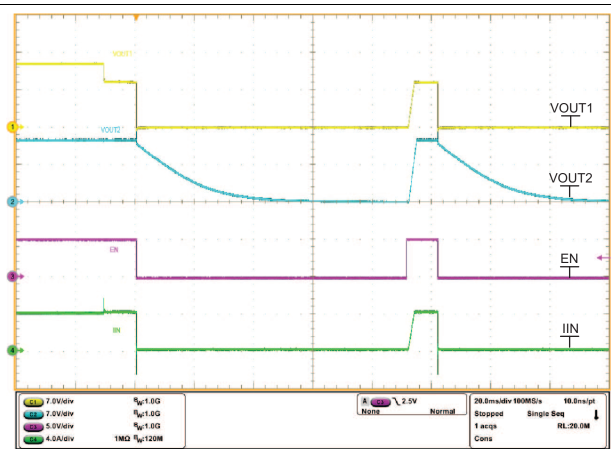


图 56. TPS259541 Self-controlled Mode Response with Overload Fault on OUT1 Followed by Auto-retry with Persistent Fault

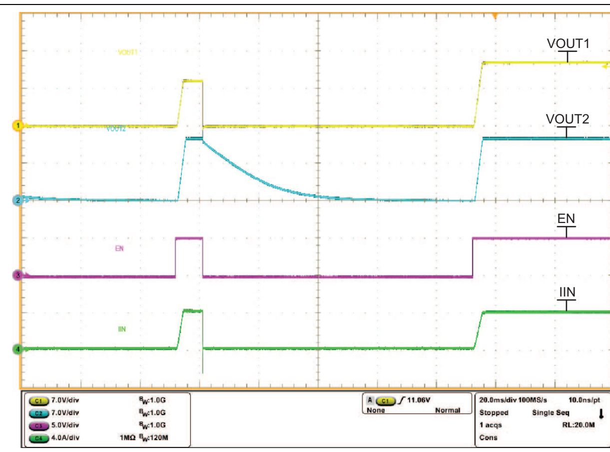


图 57. TPS259541 Self-controlled Mode Response with Overload on OUT1 Followed by Recovery with Fault Removed

9 Application and Implementation

注

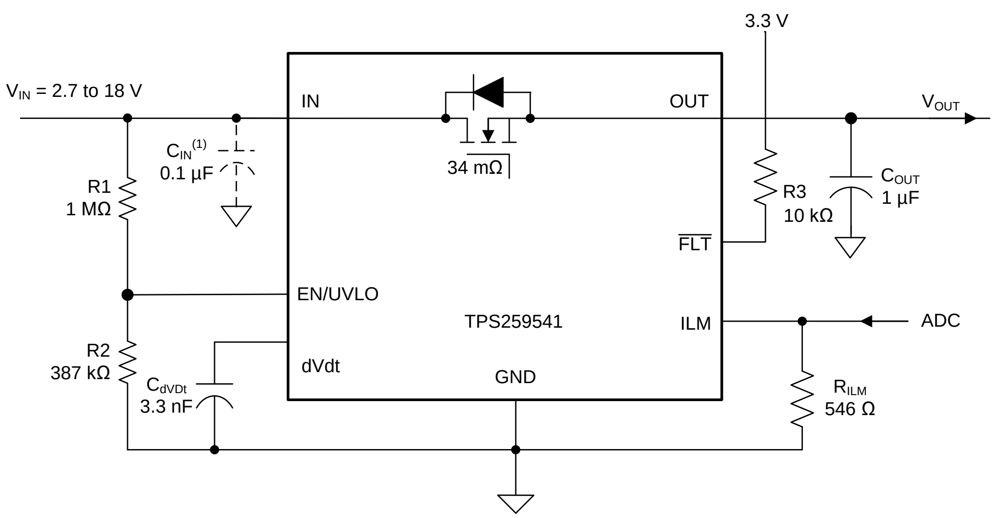
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2595xx device is an integrated eFuse that is typically used for hot-swap and power rail protection applications. The device operates from 2.7 V to 18 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as set-top box, DTVs, gaming consoles, SSDs, HDDs, and smart meters. The device also provides robust protection for multiple faults on the sub-system rail.

The following design procedure can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool *TPS2595xx Design Calculation Tool* is available.

9.2 Typical Application



(1) C_{IN} is optional and 0.1 µF is recommended to suppress transients due to the inductance of PCB routing or from input wiring.

图 58. Typical Application Schematic: Simple e-Fuse for Set-Top Boxes

9.2.1 Design Requirements

表 3 lists the TPS25954x design requirements.

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage , V_{IN}	12 V
Undervoltage lockout set point, V_{UV}	4.3 V
Overvoltage protection set point , V_{OV}	Default: V_{OVC} = 13.7 V
Load at start-up, $R_{L(SU)}$	4 Ω
Current limit, I_{LIMIT}	3.7 A
Load capacitance, C_{OUT}	1 µF
Maximum ambient temperatures, T_A	85°C

9.2.2 Detailed Design Procedure

The designer must know the following:

- Normal input operation voltage
- Maximum output capacitance
- Maximum current Limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

9.2.2.1 Programming the Current-Limit Threshold: R_{ILM} Selection

The R_{ILM} resistor at the ILM pin sets the over load current limit, this can be set using 公式 6.

$$R_{ILM} = \frac{2000}{I_{LIMIT} - 0.04} \quad (6)$$

For I_{LIMIT} = 3.7 A, from 公式 6, R_{ILM} is 546 Ω, choose closest standard value resistor with 1% tolerance.

9.2.2.2 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R_1 and R_2 as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving 公式 7.

$$V_{UV} = \frac{R1 + R2}{R2} \times V_{UVLO(R)} \quad (7)$$

Where $V_{UVLO(R)}$ is UVLO rising threshold (1.2 V). Because R1 and R2 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}.

The current drawn by R1 and R2 from the power supply is $I_{R12} = V_{IN} / (R1 + R2)$.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{R12} must be chosen to be 20 times greater than the leakage current expected.

To set the UVLO at V_{UVR} = 4.3 V, select R2 = 387 kΩ, and R1 = 1 MΩ.

9.2.2.3 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The required ramp-up capacitor C_{dVdT} is calculated considering the two possible cases (see Case 1: Start-Up Without Load. Only Output Capacitance C_{OUT} Draws Current and Case 2: Start-Up With Load. Output Capacitance C_{OUT} and Load Draw Current).

9.2.2.3.1 Case 1: Start-Up Without Load. Only Output Capacitance C_{OUT} Draws Current

During start-up, as the output capacitor charges, the voltage drop as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using 公式 9.

For TPS2592xx device, the inrush current is determined as shown in 公式 8.

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN}}{T_{dVdT}} \quad (8)$$

Power dissipation during start-up is shown in 公式 9.

$$P_{D(INRUSH)} = 0.5 \times V_{IN} \times I_{INRUSH} \tag{9}$$

公式 9 assumes that load does not draw any current until the output voltage has reached its final value.

9.2.2.3.2 Case 2: Start-Up With Load. Output Capacitance C_{OUT} and Load Draw Current

When the load draws current during the turnon sequence, there is additional power dissipated. Considering a resistive load during start-up $R_{L(SU)}$, load current ramps up proportionally with increase in output voltage during T_{dVdT} time. 公式 10 to 公式 13 show the average power dissipation in the internal FET during charging time due to resistive load.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V_{IN}^2}{R_{L(SU)}} \tag{10}$$

Total power dissipated in the device during start-up is 公式 11.

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \tag{11}$$

Total current during start-up is given by 公式 12.

$$I_{STARTUP} = I_{INRUSH} + I_L(t) \tag{12}$$

If $I_{STARTUP} > I_{LIMIT}$, the device limits the current to I_{LIMIT} and the current-limited charging time is determined by 公式 13.

$$T_{dvdT(Current-Limited)} = C_{OUT} \times R_{L(SU)} \times \left[\frac{I_{LIMIT}}{I_{INRUSH}} - 1 + LN\left(\frac{I_{INRUSH}}{I_{LIMIT} - \frac{V_{IN}}{R_{L(SU)}}}\right)\right] \tag{13}$$

The power dissipation, with and without load, for selected start-up time must not exceed the shutdown limits as shown in 图 59.

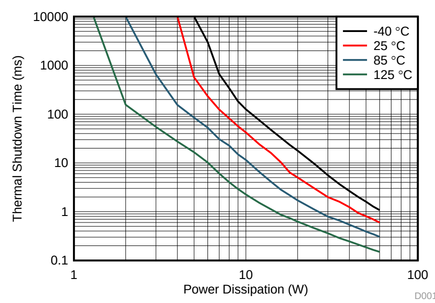


图 59. Thermal Shutdown Limit Plot

For the design example under discussion, select ramp-up capacitor C_{dVdt} = OPEN. The default slew rate for C_{dVdt} = OPEN is 38.2 mV/µs. With slew rate of 38.2 mV/µs, the ramp-up time T_{dVdt} for 12 V input is 248 µs.

The inrush current drawn by the load capacitance C_{OUT} during ramp-up using 公式 14.

$$I_{INRUSH} = \frac{1\,\mu F \times 38.2\,mV}{\mu s} = 38.2\,mA \tag{14}$$

The inrush power dissipation is calculated using 公式 15.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 38.2\,m = 229.2\,mW \tag{15}$$

For 229.2 mW of power loss, the thermal shutdown time of the device must not be less than the ramp-up time T_{dVdt} to avoid the false trip at the maximum operating temperature. 图 59 shows the thermal shutdown limit at T_A = 85°C, for 229.2 mW of power, the shutdown time is infinite. Therefore, it is safe to use 248 µs as the start-up time without any load on the output.

The additional power dissipation when a 4 Ω load is present during start-up is calculated using 公式 10.

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 4} = 6\ W \quad (16)$$

The total device power dissipation during start-up is given in 公式 17.

$$P_{D(STARTUP)} = 6 + 229.2\ m = 6.229\ W \quad (17)$$

The 图 59 shows T_A = 85°C and the thermal shutdown time for 6.229 W is more than 10 ms, which is well within the acceptable limits to not use an external capacitor C_{dVdt} with a start-up load of 4 Ω.

When C_{OUT} is large, there is a need to decrease the power dissipation during start-up. This can be done by increasing the value of the C_{dVdt} capacitor.

9.2.3 Support Component Selection: C_{IN}

C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range from 0.001 µF to 0.1 µF is recommended for C_{IN}.

9.2.4 Application Curves

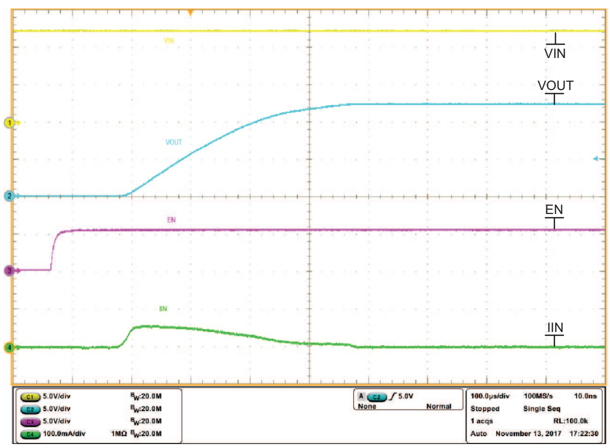


图 60. Output Ramp without Any Load

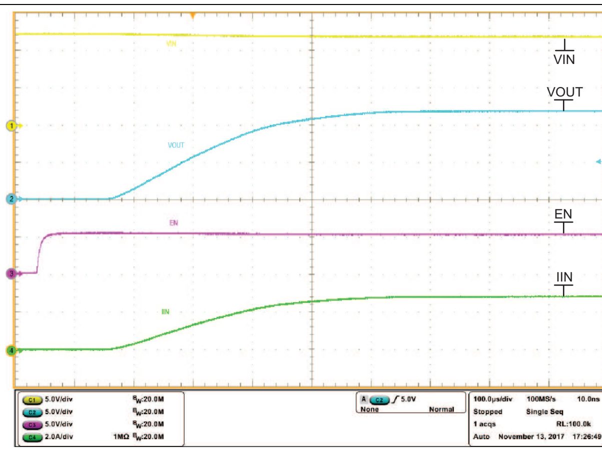


图 61. Output Ramp with 4 Ω Load at Start-up

9.2.5 Controlled Power Down (Quick Output Discharge) using TPS2595x5

When the TPS2595x5 device is disabled, the output voltage is left floating and the power-down profile is entirely dictated by the load. In some applications, this can lead to undesired activity because the load is not powered down to a defined state. Controlled output discharge can ensure the load is completely turned off and is not in an undefined operational state. The QOD pin in the TPS2595x5 device can be connected to the OUT pin to facilitate the Quick Output Discharge function, as shown in 图 62. When the TPS2595x5 device is disabled, the QOD pin is pulled low and provides a quick discharge path for the output capacitor. The output voltage discharge rate is dictated by the output capacitor C_{OUT}, the total discharge path resistance (internal plus external), and the load.

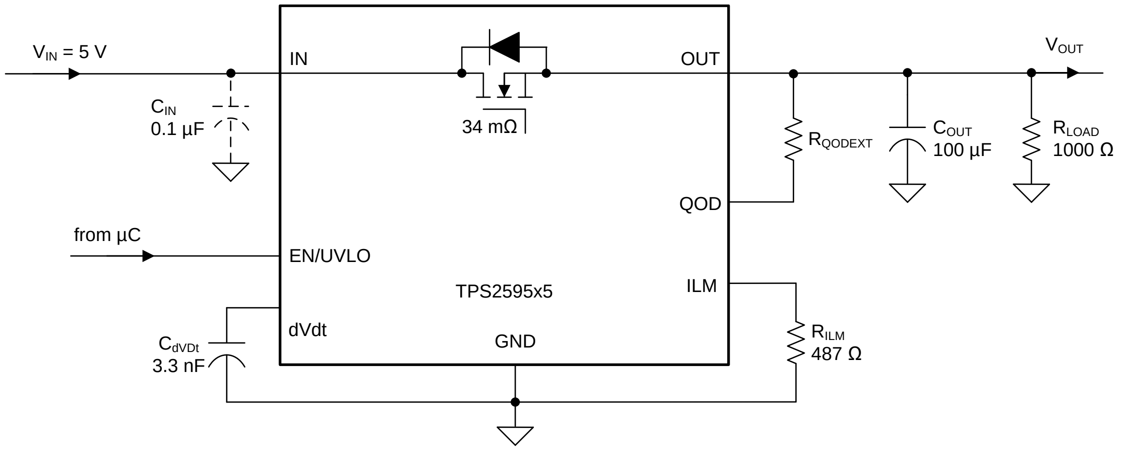


图 62. Circuit Implementation with Quick Output Discharge Function using TPS2595x5

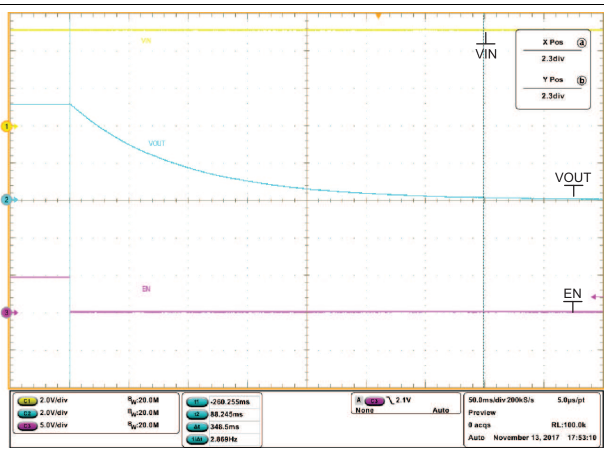


图 63. Output Voltage Discharge using TPS259535 without QOD [V_{IN} = 5 V, EN = H → L, C_{OUT} = 100 µF, R_{LOAD} = 1000 Ω, R_{QODEXT} = OPEN]

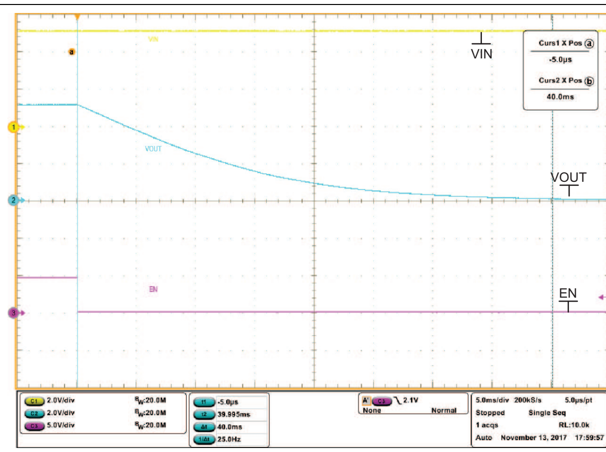


图 64. Output Voltage Discharge using TPS259535 with QOD [V_{IN} = 5 V, EN = H → L, C_{OUT} = 100 µF, R_{LOAD} = 1000 Ω, R_{QODEXT} = Short]

9.2.6 Overvoltage Lockout using TPS259573

The TPS259573 device incorporates a circuit to protect the system during overvoltage conditions. A resistor divider connected from the supply to the EN/OVLO pin to GND (as shown in 图 65) programs the overvoltage threshold. A voltage more than V_{OVLO} on the EN/OVLO pin turns off the internal FET and protects the downstream load. 图 66 shows overvoltage cut-off at the input voltage of 15 V.

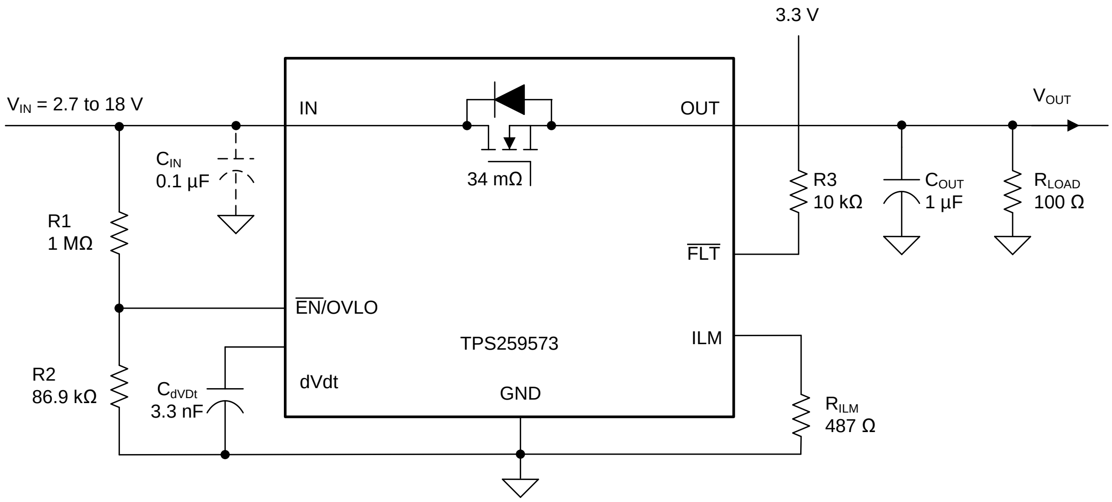


图 65. Circuit Implementation for Overvoltage Lockout using TPS259573

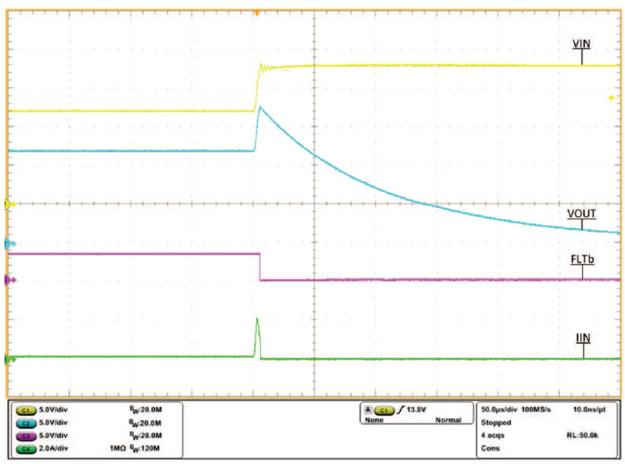


图 66. Overvoltage Lockout Response using TPS259573

10 Power Supply Recommendations

The TPS2595xx devices are designed for a supply voltage range of 2.7 V ≤ VIN ≤ 18 V. An input ceramic bypass capacitor higher than 0.1 μF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

10.1 Transient Protection

In the case of a short circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Use a Schottky diode across the output to absorb negative spikes.
- Use a low-value ceramic capacitor C_{IN} = 0.001 μF to 0.1 μF to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with 公式 18:

$$V_{SPIKE(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}}$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input (18)

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and Schottky diode) is shown in 图 67.

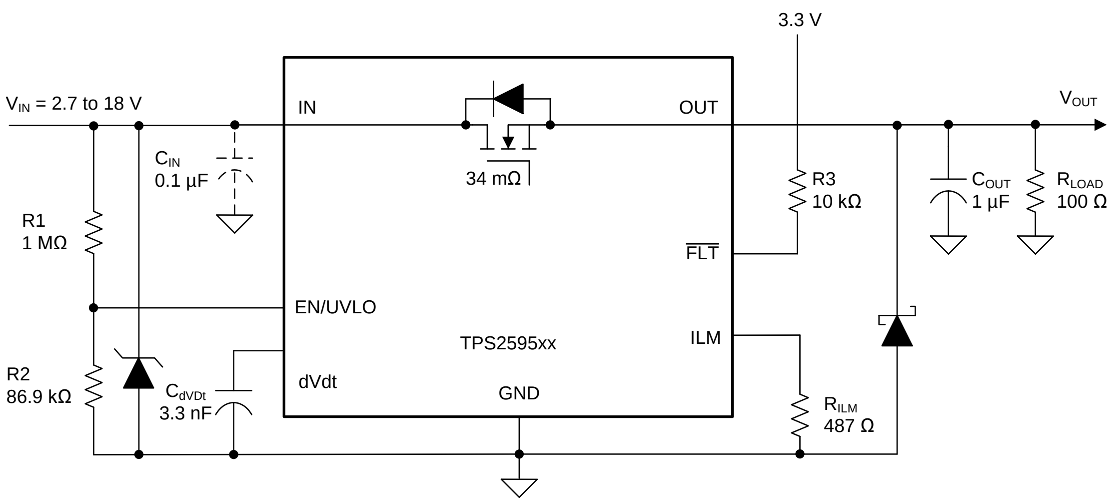


图 67. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

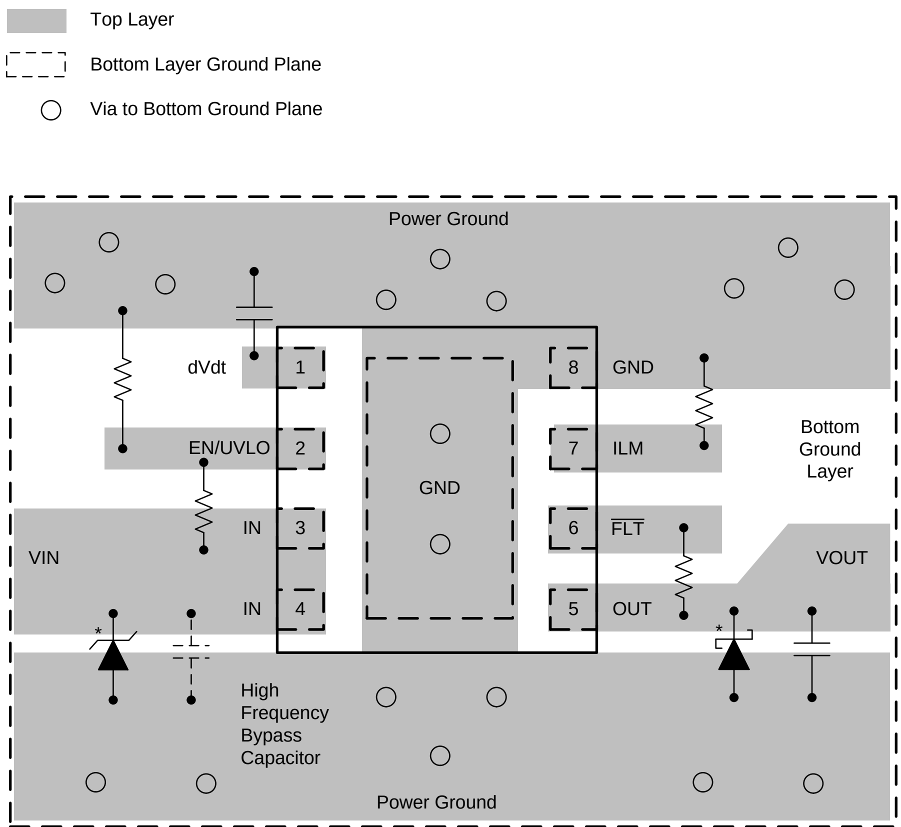
11 Layout

11.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.01 µF or greater is recommended between the IN terminal and GND terminal. For hot-plug applications, where input power-path inductance is negligible, this capacitor can be eliminated or minimized.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See 图 68 for a PCB layout example.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - Resistors for the EN/UVLO (or $\overline{EN}$/OVLO) pin

  Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILM} and C_{dVdT} components to the device must be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible; *Layout Example* has been shown to produce good results and is intended as a guideline.

11.2 Layout Example



(1) Optional: Needed only to suppress the transients caused by inductive load switching

图 68. TPS2595xx Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

TPS2595EVM 电子保险丝评估板
TPS2595xx 设计计算工具

12.1.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 **4.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TPS259520	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259521	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259530	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259531	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259533	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259540	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259541	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259570	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259571	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259573	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259525	单击此处	单击此处	单击此处	单击此处	单击此处
TPS259535	单击此处	单击此处	单击此处	单击此处	单击此处

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS259520DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES20	Samples
TPS259520DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES20	Samples
TPS259521DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES21	Samples
TPS259521DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES21	Samples
TPS259525DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES25	Samples
TPS259525DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES25	Samples
TPS259530DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES30	Samples
TPS259530DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES30	Samples
TPS259531DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES31	Samples
TPS259531DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES31	Samples
TPS259533DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES33	Samples
TPS259533DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES33	Samples
TPS259535DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES35	Samples
TPS259535DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES35	Samples
TPS259540DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES40	Samples
TPS259540DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES40	Samples
TPS259541DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES41	Samples
TPS259541DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES41	Samples
TPS259570DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES70	Samples
TPS259570DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES70	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS259571DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES71	Samples
TPS259571DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES71	Samples
TPS259573DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES73	Samples
TPS259573DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ES73	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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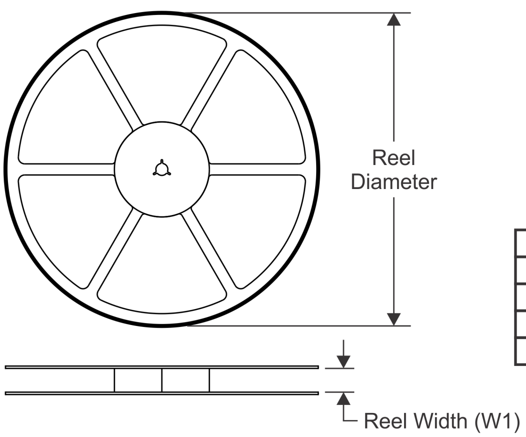
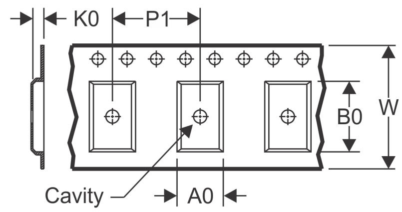
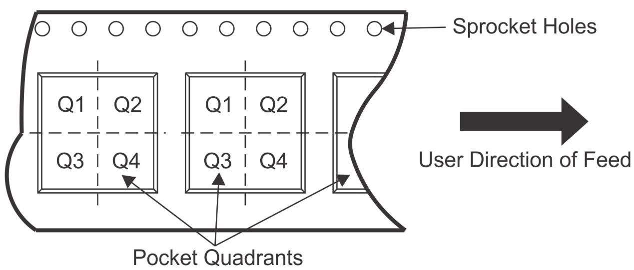
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

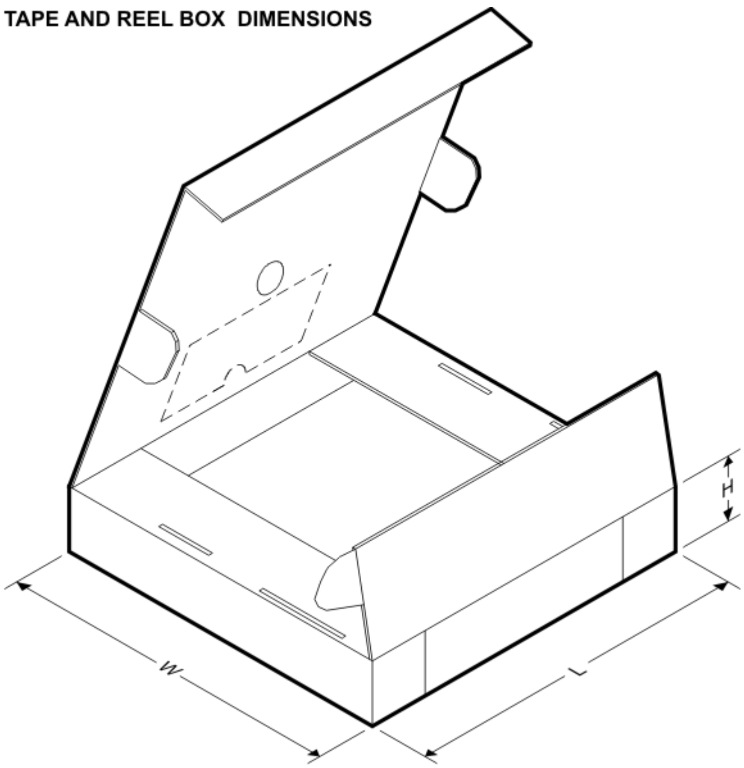


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259520DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259520DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259521DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259521DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259525DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259525DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259530DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259530DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259531DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259531DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259533DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259533DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259535DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259535DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259540DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259540DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259541DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259541DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259570DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259570DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259571DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259571DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259573DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259573DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259520DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259520DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259521DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259521DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259525DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259525DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259530DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259530DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259531DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259531DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259533DSGR	WSON	DSG	8	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259533DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259535DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259535DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259540DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259540DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259541DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259541DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259570DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259570DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259571DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259571DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS259573DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS259573DSGT	WSON	DSG	8	250	210.0	185.0	35.0

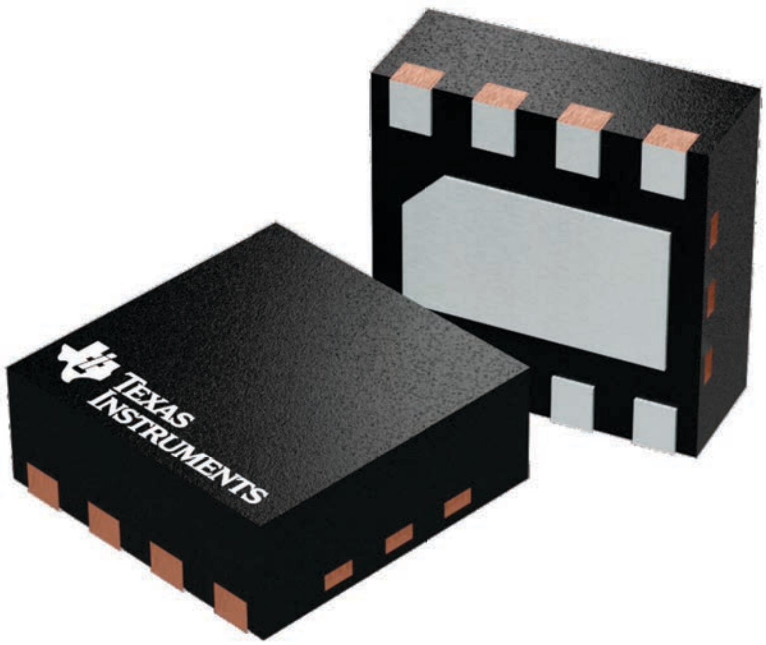
DSG 8

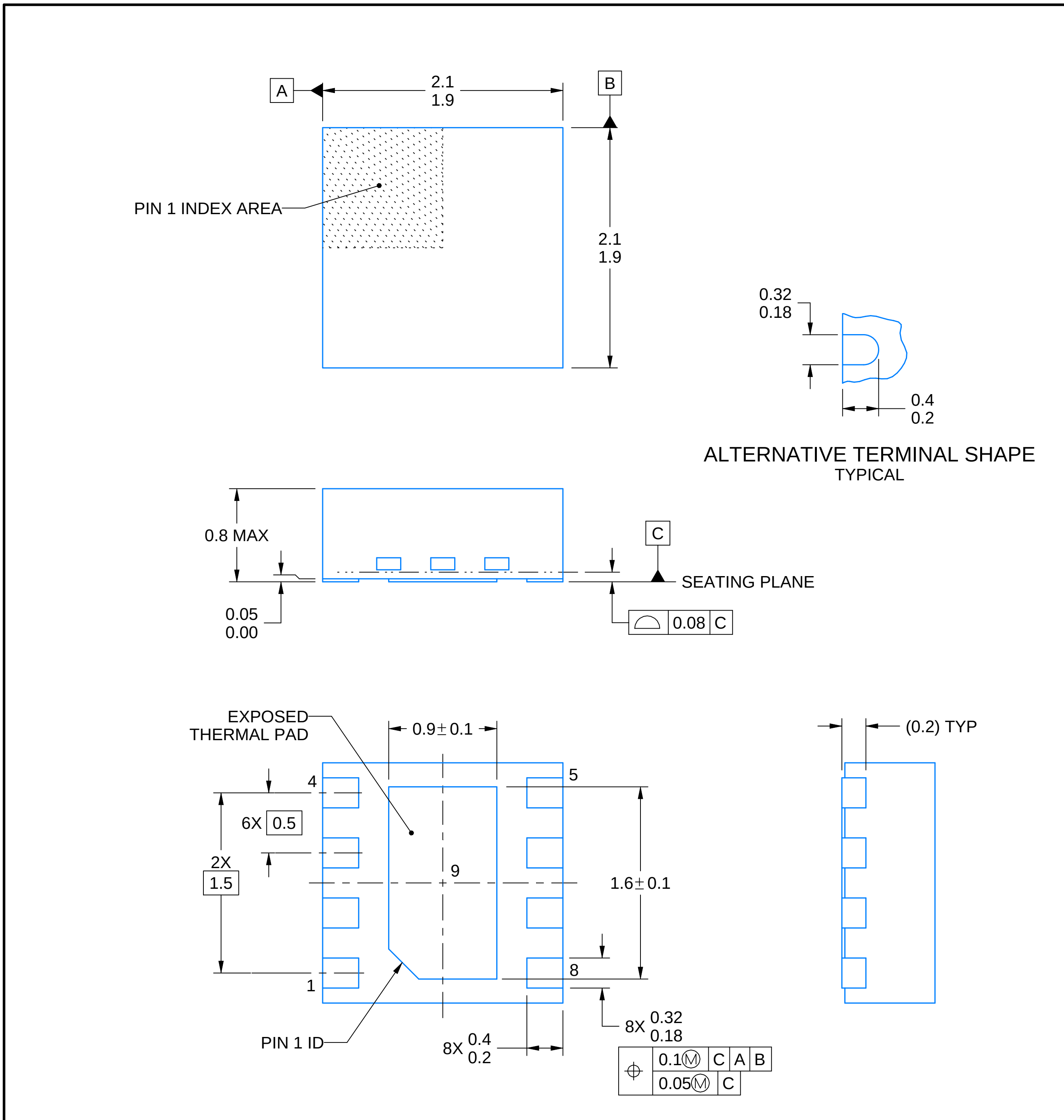
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





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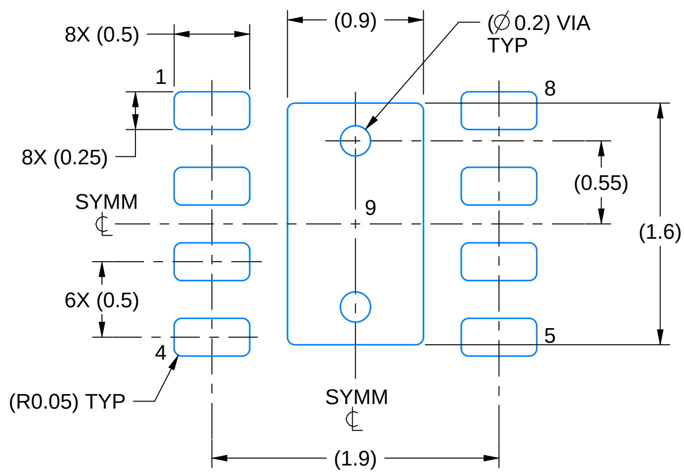
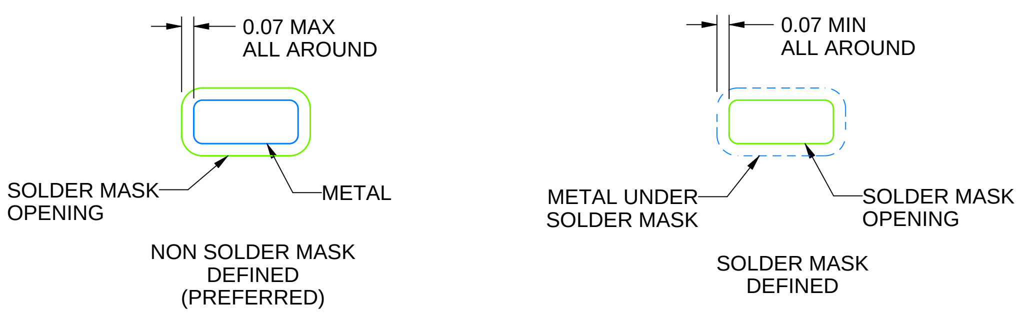
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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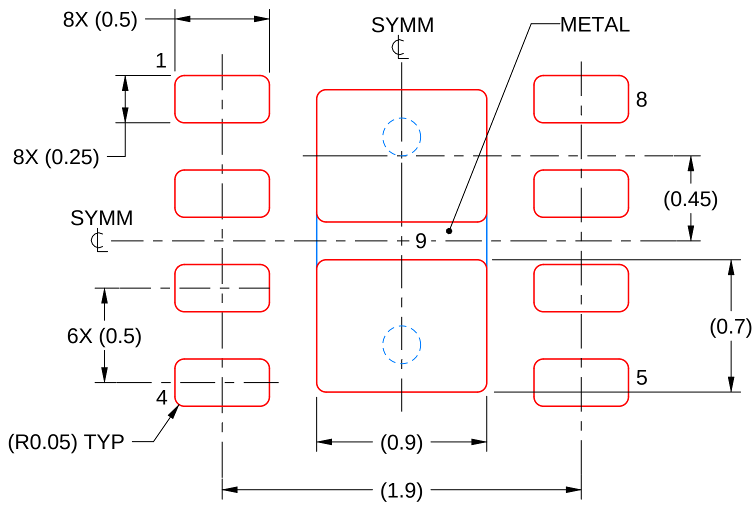
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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