Ultracompact, 1 A Thermoelectric Cooler (TEC) Driver for Digital Control Systems

Data Sheet

ADN8833

FEATURES

- Patented high efficiency single inductor architecture
- Integrated low R_{DSON} MOSFETs for TEC driver
- TEC voltage and current operation monitoring
- No external sense resistor required
- Independent TEC heating and cooling current limit settings
- Programmable maximum TEC voltage
- 2 MHz PWM driver switching frequency
- External synchronization
- Digital thermal control loop compatible
- 2.50 V reference output with 1% accuracy
- Available in a 25-ball, 2.5 mm × 2.5 mm WLCSP or in a 24-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- TEC temperature control
- Optical modules
- Optical fiber amplifiers
- Optical networking systems
- Instruments requiring TEC temperature control

FUNCTIONAL BLOCK DIAGRAM

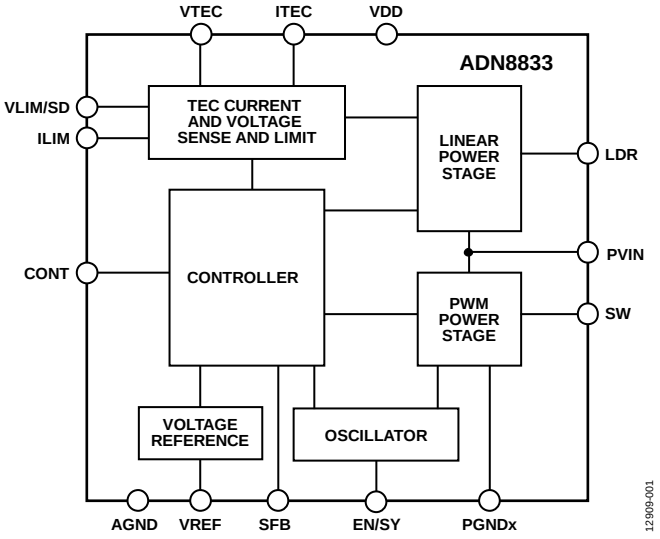

Figure 1.

GENERAL DESCRIPTION

The ADN8833[1] is a monolithic H-bridge TEC driver with integrated 1 A power MOSFETs. It has a linear power stage with the linear driver (LDR) output and a pulse-width modulation (PWM) power stage with the SW output. Depending on the control voltage at the CONT input, the ADN8833 drives current through a TEC to settle the temperature of a laser diode or a passive component attached to the TEC module to the programmed target temperature.

The control voltage applied to the CONT input is generated by a digital-to-analog converter (DAC) closing the digital proportional, integral, derivative (PID) loop of temperature control system.

The internal 2.5 V reference voltage provides a 1% accurate output that is used to bias a voltage divider network to program the maximum TEC current and voltage limits for both the heating and cooling modes. It can also be a reference voltage for the DAC and the temperature sensing circuit, including a thermistor bridge and an analog-to-digital converter (ADC).

Table 1. TEC Family Models

Model	MOSFET	Thermal Loop	Package
ADN8831	Discrete	Digital/analog	LFCSP (CP-32-7)
ADN8833	Integrated	Digital	WLCSP (CB-25-7), LFCSP (CP-24-15)
ADN8834	Integrated	Digital/analog	WLCSP (CB-25-7), LFCSP (CP-24-15)

[1] Product is covered by US Patent No. 6,486,643.

Rev. B
Document Feedback

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REVISION HISTORY

8/2018—Rev. A to Rev. B

Added Patent Information ... 1

8/2015—Rev. 0 to Rev. A

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4/2015—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 2.7 V to 5.5 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A =25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Driver Supply Voltage	V_{PVIN}	WLCSP	2.7		5.5	V
	V_{PVINL}, V_{PVINS}	LFCSP	2.7		5.5	V
Controller Supply Voltage	V_{VDD}		2.7		5.5	V
Supply Current	I_{VDD}	PWM not switching		2.1	3.5	mA
Shutdown Current	I_{SD}	EN/SY = AGND or VLIM/SD = AGND		350	700	µA
Undervoltage Lockout (UVLO)	V_{UVLO}	V_{VDD} rising	2.45	2.55	2.65	V
UVLO Hysteresis	$UVLO_{HYST}$		80	90	100	mV
REFERENCE VOLTAGE	V_{VREF}	I_{VREF} = 0 mA to 10 mA	2.475	2.50	2.525	V
LINEAR OUTPUT						
Output Voltage	V_{LDR}	I_{LDR} = 0 A				
Low				0		V
High				V_{PVIN}		V
Maximum Source Current	I_{LDR_SOURCE}	T_J = −40°C to +125°C	1.0			A
Maximum Sink Current	I_{LDR_SINK}	T_J = −40°C to +125°C			1.0	A
On Resistance		I_{LDR} = 0.6 A				
P-MOSFET	$R_{DS\_PL(ON)}$	WLCSP, V_{PVIN} = 5.0 V		35	50	mΩ
		WLCSP, V_{PVIN} = 3.3 V		44	60	mΩ
		LFCSP, V_{PVIN} = 5.0 V		50	65	mΩ
		LFCSP, V_{PVIN} = 3.3 V		55	75	mΩ
N-MOSFET	$R_{DS\_NL(ON)}$	WLCSP, V_{PVIN} = 5.0 V		31	50	mΩ
		WLCSP, V_{PVIN} = 3.3 V		40	55	mΩ
		LFCSP, V_{PVIN} = 5.0 V		45	70	mΩ
		LFCSP, V_{PVIN} = 3.3 V		50	80	mΩ
Leakage Current						
P-MOSFET	$I_{LDR\_P\_LKG}$			0.1	10	µA
N-MOSFET	$I_{LDR\_N\_LKG}$			0.1	10	µA
Linear Amplifier Gain	A_{LDR}			40		V/V
LDR Short-Circuit Threshold	$I_{LDR\_SH\_GNDL}$	LDR short to PGNDL, enter hiccup		2.2		A
	$I_{LDR\_SH\_PVIN}$	LDR short to PVIN, enter hiccup		−2.2		A
Hiccup Cycle	T_{HICCUP}			15		ms
PWM OUTPUT						
Output Voltage	V_{SFB}	I_{SFB} = 0 A				
Low				0.06 × V_{PVIN}		V
High				0.93 × V_{PVIN}		V
Maximum Source Current	I_{SW_SOURCE}	T_J = −40°C to +125°C		1.0		A
Maximum Sink Current	I_{SW_SINK}	T_J = −40°C to +125°C			1.0	A
On Resistance		I_{SW} = 0.6 A				
P-MOSFET	$R_{DS\_PS(ON)}$	WLCSP, V_{PVIN} = 5.0 V		47	65	mΩ
		WLCSP, V_{PVIN} = 3.3 V		60	80	mΩ
		LFCSP, V_{PVIN} = 5.0 V		60	80	mΩ
		LFCSP, V_{PVIN} = 3.3 V		70	95	mΩ
N-MOSFET	$R_{DS\_NS(ON)}$	WLCSP, V_{PVIN} = 5.0 V		40	60	mΩ
		WLCSP, V_{PVIN} = 3.3 V		45	65	mΩ
		LFCSP, V_{PVIN} = 5.0 V		45	75	mΩ
		LFCSP, V_{PVIN} = 3.3 V		55	85	mΩ

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Leakage Current						
P-MOSFET	$I_{SW\_P\_LKG}$			0.1	10	µA
N-MOSFET	$I_{SW\_N\_LKG}$			0.1	10	µA
SW Node Rise Time[1]	t_{SW_R}	C_{SW} = 1 nF		1		ns
PWM Duty Cycle[2]	D_{SW}		6		93	%
SFB Input Bias Current	I_{SFB}			1	2	µA
PWM OSCILLATOR						
Internal Oscillator Frequency	f_{OSC}	EN/SY high	1.85	2.0	2.15	MHz
EN/SY Input Voltage						
Low	V_{EN/SY_ILOW}				0.8	V
High	V_{EN/SY_IHIGH}		2.1			V
External Synchronization Frequency	f_{SYNC}		1.85		3.25	MHz
Synchronization Pulse Duty Cycle	D_{SYNC}		10		90	%
EN/SY Rising to PWM Rising Delay	t_{SYNC_PWM}			50		ns
EN/SY to PWM Lock Time	t_{SY_LOCK}	Number of SYNC cycles			10	Cycles
EN/SY Input Current	$I_{EN/SY}$			0.3	0.5	µA
Pull-Down Current				0.3	0.5	µA
DRIVER CONTROL INPUT						
Input Voltage Range	V_{CONT}		0		V_{VREF}	V
Input Resistance	R_{CONT}			40		kΩ
Input Capacitance[1]	C_{CONT}			40		pF
TEC CURRENT LIMIT						
ILIM Input Voltage Range						
Cooling	V_{ILIMC}		1.3		V_{VREF} − 0.2	V
Heating	V_{ILIMH}		0.2		1.2	V
Current-Limit Threshold						
Cooling	V_{ILIMC_TH}	V_{ITEC} = 0.5 V	1.98	2.0	2.02	V
Heating	V_{ILIMH_TH}	V_{ITEC} = 2 V	0.48	0.5	0.52	V
ILIM Input Current						
Heating	I_{ILIMH}		−0.2		+0.2	µA
Cooling	I_{ILIMC}	Sourcing current	37.5	40	42.5	µA
Cooling to Heating Current Detection Threshold	$I_{COOL\_HEAT\_TH}$			40		mA
TEC VOLTAGE LIMIT						
Voltage Limit Gain	A_{VLIM}	$(V_{LDR} - V_{SFB})/V_{VLIM}$		2		V/V
VLIM/SD Input Voltage Range[1]	V_{VLIM}		0.2		$V_{VDD}/2$	V
VLIM/SD Input Current						
Cooling	I_{ILIMC}	$V_{OUT2} < V_{VREF}/2$	−0.2		+0.2	µA
Heating	I_{ILIMH}	$V_{OUT2} > V_{VREF}/2$, sinking current	8	10	12.2	µA
TEC CURRENT MEASUREMENT (WLCSP)						
Current Sense Gain	R_{CS}	V_{PVIN} = 3.3 V		0.525		V/A
		V_{PVIN} = 5 V		0.535		V/A
Current Measurement Accuracy	I_{LDR_ERROR}	700 mA ≤ I_{LDR} ≤ 1 A, V_{PVIN} = 3.3 V	−10		+10	%
		800 mA ≤ I_{LDR} ≤ 1 A, V_{PVIN} = 5 V	−10		+10	%
ITEC Voltage Accuracy	$V_{ITEC\_@\_700\_mA}$	V_{PVIN} = 3.3 V, cooling, $V_{VREF}/2 + I_{LDR} \times R_{CS}$	1.455	1.618	1.779	V
	$V_{ITEC\_@\_-700\_mA}$	V_{PVIN} = 3.3 V, heating, $V_{VREF}/2 - I_{LDR} \times R_{CS}$	0.794	0.883	0.971	V
	$V_{ITEC\_@\_800\_mA}$	V_{PVIN} = 5 V, cooling, $V_{VREF}/2 + I_{LDR} \times R_{CS}$	1.510	1.678	1.846	V
	$V_{ITEC\_@\_-800\_mA}$	V_{PVIN} = 5 V, heating, $V_{VREF}/2 - I_{LDR} \times R_{CS}$	0.739	0.822	0.905	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TEC CURRENT MEASUREMENT (LFCSP)						
Current Sense Gain	R_{CS}	V_{PVIN} = 3.3 V		0.525		V/A
		V_{PVIN} = 5 V		0.525		V/A
Current Measurement Accuracy	I_{LDR_ERROR}	700 mA ≤ I_{LDR} ≤ 1 A, V_{PVIN} = 3.3 V	−15		+15	%
		800 mA ≤ I_{LDR} ≤ 1 A, V_{PVIN} = 5 V	−15		+15	%
ITEC Voltage Accuracy	$V_{ITEC\_@\_700\_mA}$	V_{PVIN} = 3.3 V, cooling, $V_{VREF}/2 + I_{LDR} \times R_{CS}$	1.374	1.618	1.861	V
	$V_{ITEC\_@\_-700\_mA}$	V_{PVIN} = 3.3 V, heating, $V_{VREF}/2 - I_{LDR} \times R_{CS}$	0.750	0.883	1.015	V
	$V_{ITEC\_@\_800\_mA}$	V_{PVIN} = 5 V, cooling, $V_{VREF}/2 + I_{LDR} \times R_{CS}$	1.419	1.678	1.921	V
	$V_{ITEC\_@\_-800\_mA}$	V_{PVIN} = 5 V, heating, $V_{VREF}/2 - I_{LDR} \times R_{CS}$	0.705	0.830	0.955	V
ITEC Voltage Output Range	V_{ITEC}	I_{TEC} = 0 A	0		V_{VREF} − 0.05	V
ITEC Bias Voltage	V_{ITEC}	I_{LDR} = 0 A	1.225	1.250	1.285	V
Maximum ITEC Output Current	I_{ITEC}		−2		+2	mA
TEC VOLTAGE MEASUREMENT						
Voltage Sense Gain	A_{VTEC}		0.24	0.25	0.26	V/V
Voltage Measurement Accuracy	$V_{VTEC\_@\_1\_V}$	$V_{LDR} - V_{SFB}$ = 1 V, $V_{VREF}/2 + A_{VTEC} \times (V_{LDR} - V_{SFB})$	1.475	1.50	1.525	V
VTEC Output Voltage Range	V_{VTEC}		0.005		2.625	V
VTEC Bias Voltage	V_{VTEC_B}	$V_{LDR} = V_{SFB}$	1.225	1.250	1.285	V
Maximum VTEC Output Current	R_{VTEC}		−2		+2	mA
INTERNAL SOFT START						
Soft Start Time	t_{SS}			150		ms
VLIM/SD SHUTDOWN						
VLIM/SD Low Voltage Threshold	V_{VLIM/SD_THL}				0.07	V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN_TH}			170		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			17		°C

[1] This specification is guaranteed by design.
[2] This specification is guaranteed by characterization.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
PVIN to PGNDL (WLCSP)	−0.3 V to +5.75 V
PVIN to PGNDS (WLCSP)	−0.3 V to +5.75 V
PVINL to PGNDL (LFCSP)	−0.3 V to +5.75 V
PVINS to PGNDS (LFCSP)	−0.3 V to +5.75 V
LDR to PGNDL (WLCSP)	−0.3 V to V_{PVIN}
LDR to PGNDL (LFCSP)	−0.3 V to V_{PVINL}
SW to PGNDS	−0.3 V to +5.75 V
SFB to AGND	−0.3 V to V_{VDD}
AGND to PGNDL	−0.3 V to +0.3 V
AGND to PGNDS	−0.3 V to +0.3 V
VLIM/SD to AGND	−0.3 V to V_{VDD}
ILIM to AGND	−0.3 V to V_{VDD}
VREF to AGND	−0.3 V to +3 V
VDD to AGND	−0.3 V to +5.75 V
EN/SY to AGND	−0.3 V to V_{VDD}
ITEC to AGND	−0.3 V to +5.75 V
VTEC to AGND	−0.3 V to +5.75 V
Maximum Current	
VREF to AGND	20 mA
ITEC to AGND	50 mA
VTEC to AGND	50 mA
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages, and is based on a 4-layer standard JEDEC board.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
25-Ball WLCSP	48	0.6	°C/W
24-Lead LFCSP	37	1.65	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

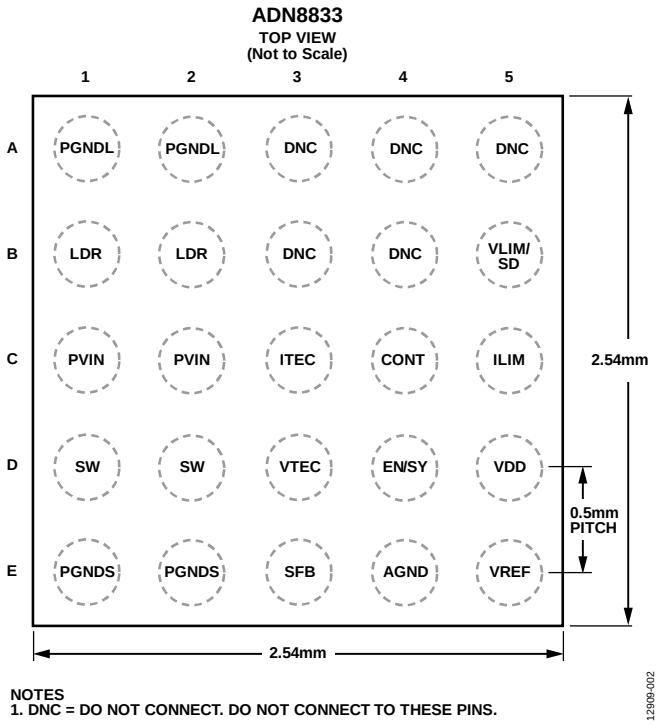


Figure 2. WLCSP Pin Configuration (Top View)

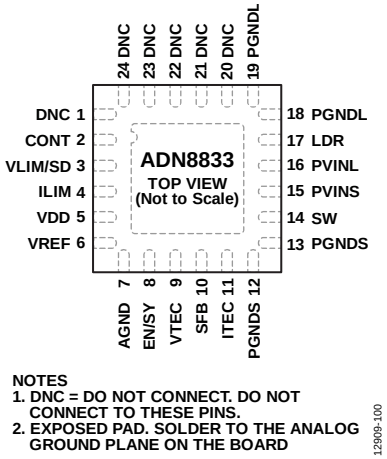


Figure 3. LFCSP Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.			
WLCSP	**LFCSP**	**Mnemonic**	**Description**
A1, A2	18, 19	PGNDL	Power Ground of the Linear TEC Driver.
A3 to A5, B3, B4	1, 20 to 24	DNC	Do Not Connect. Do not connect to these pins.
B1, B2	17	LDR	Output of the Linear TEC Driver.
B5	3	VLIM/SD	Voltage Limit/Shutdown. This pin sets the cooling and heating TEC voltage limits. When this pin is pulled low, the device shuts down.
C1, C2	N/A[1]	PVIN	Power Input for the TEC Driver.
N/A[1]	16	PVINL	Power input for the linear TEC driver
N/A[1]	15	PVINS	Power input for the PWM TEC driver
C3	11	ITEC	TEC Current Output.
C4	2	CONT	Control Input of the TEC Driver. Apply a control signal from the DAC to this pin to close the thermal loop.
C5	4	ILIM	Current Limit. This pin sets the TEC cooling and heating current limits.
D1, D2	14	SW	Switch Node Output of the PWM TEC Driver.
D3	9	VTEC	TEC Voltage Output.
D4	8	EN/SY	Enable/Synchronization. Set this pin high to enable the device. An external synchronization clock input can be applied to this pin.
D5	5	VDD	Power for the Driver Circuits.
E1, E2	12, 13	PGNDS	Power Ground of the PWM TEC Driver.
E3	10	SFB	Feedback of the PWM TEC Driver Output.
E4	7	AGND	Signal Ground.
E5	6	VREF	2.5 V Reference Output.
N/A[1]	0	EP	Exposed Pad. Solder to the analog ground plane on the board.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

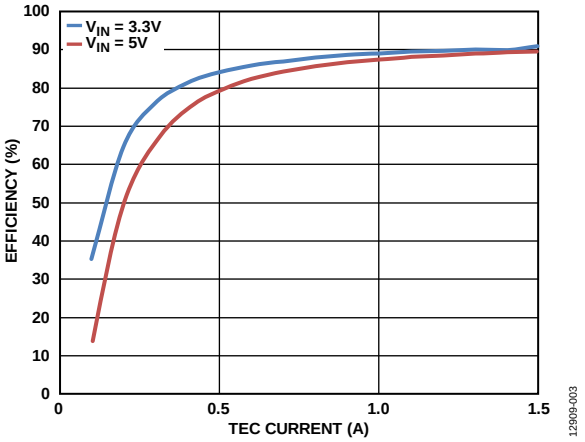


Figure 4. Efficiency vs. TEC Current at V_{IN} = 3.3 V and 5 V in Cooling Mode with 2 Ω Load

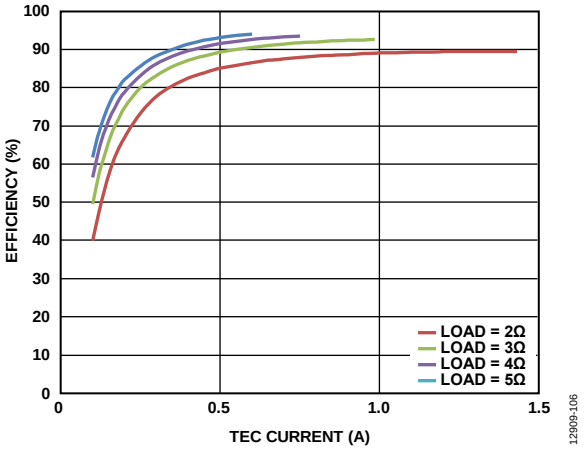


Figure 7. Efficiency vs. TEC Current at V_{IN} = 3.3 V with Different Loads in Heating Mode

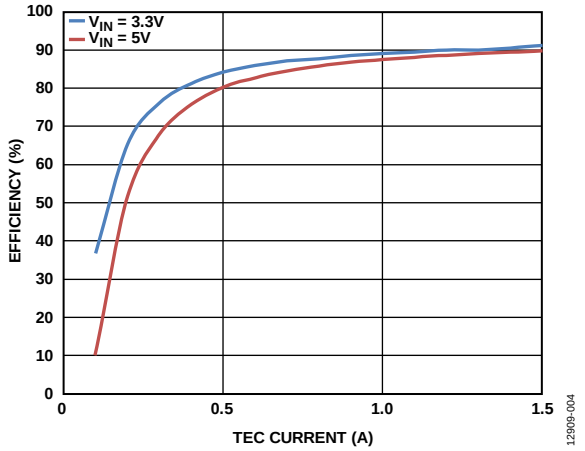


Figure 5. Efficiency vs. TEC Current at V_{IN} = 3.3 V and 5 V in Heating Mode with 2 Ω Load

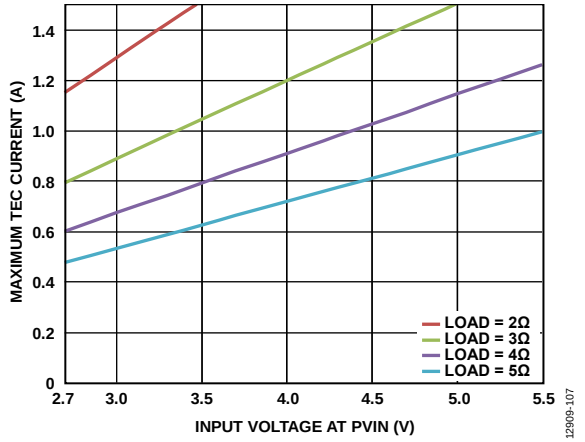


Figure 8. Maximum TEC Current vs. Input Voltage at PVIN (V_{IN} = 3.3 V), Without Voltage and Current Limit in Cooling Mode

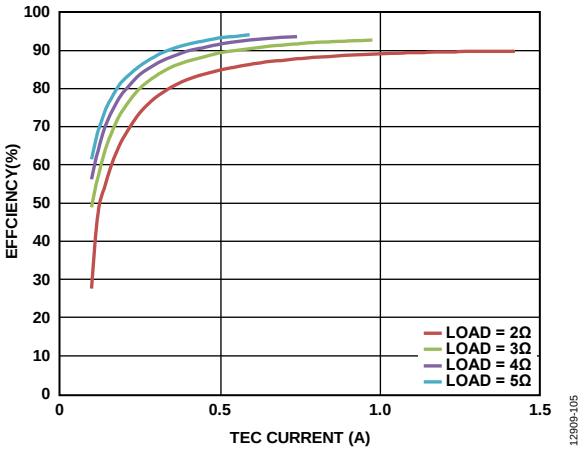


Figure 6. Efficiency vs. TEC Current at V_{IN} = 3.3 V with Different Loads in Cooling Mode

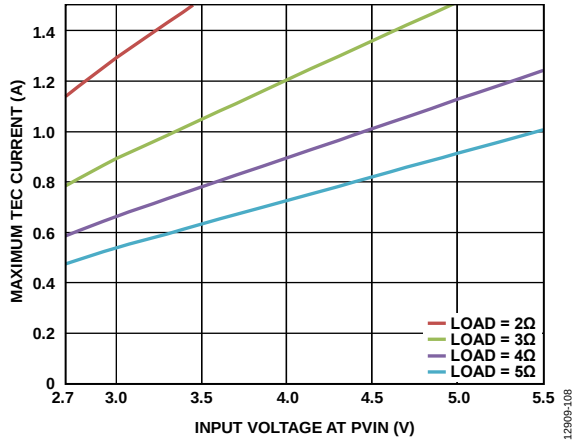


Figure 9. Maximum TEC Current vs. Input Voltage at PVIN (V_{IN} = 3.3 V), Without Voltage and Current Limit in Heating Mode

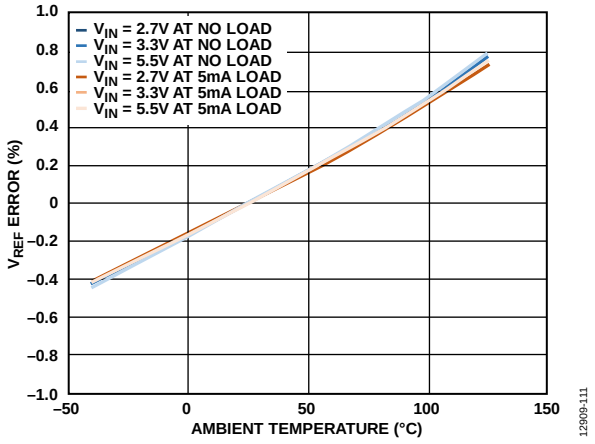


Figure 10. V_{REF} Error vs. Ambient Temperature

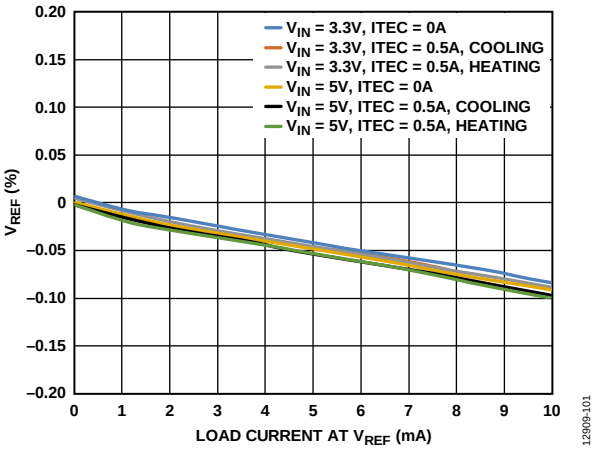


Figure 11. V_{REF} Load Regulation

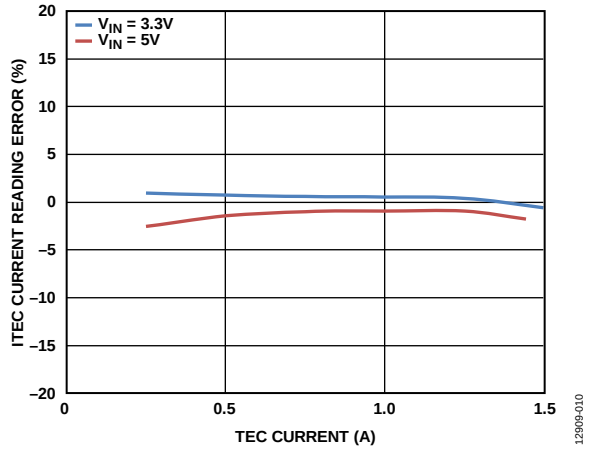


Figure 12. ITEC Current Reading Error vs. TEC Current in Heating Mode

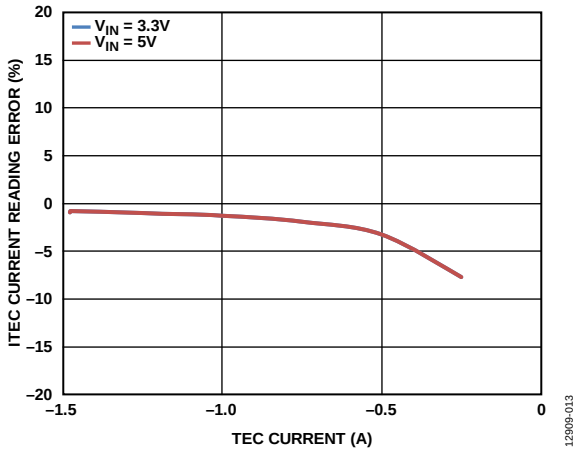


Figure 13. ITEC Current Reading Error vs. TEC Current in Cooling Mode

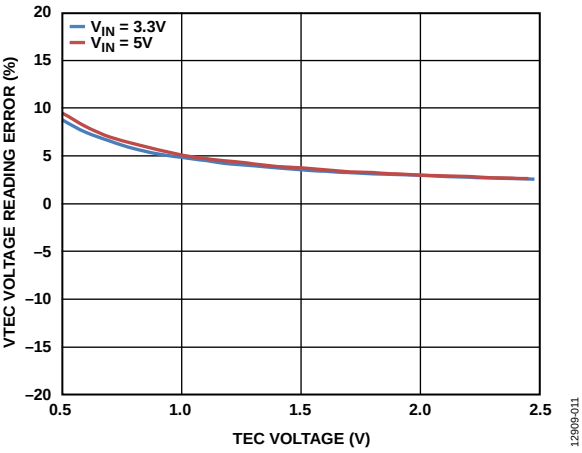


Figure 14. VTEC Voltage Reading Error vs. TEC Voltage in Cooling Mode

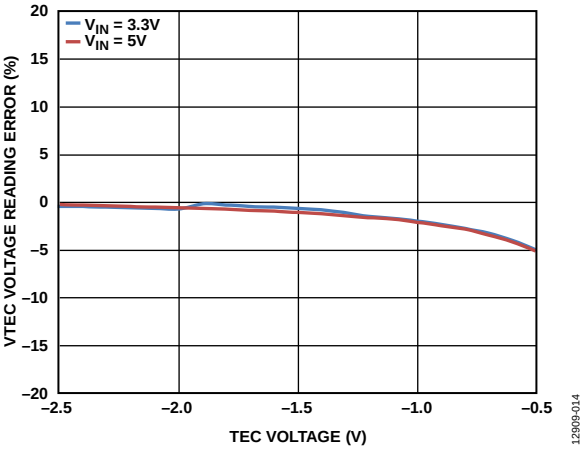


Figure 15. VTEC Voltage Reading Error vs. TEC Voltage in Heating Mode

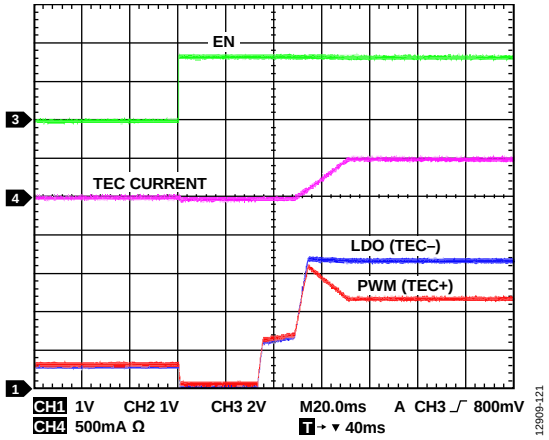


Figure 16. Typical Enable Waveforms in Cooling Mode, V_{IN} = 3.3 V, Load = 2 Ω, TEC Current = 1 A

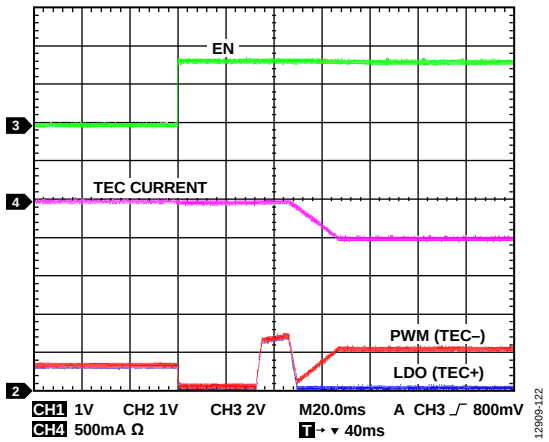


Figure 17. Enable Waveforms in Heating Mode, V_{IN} = 3.3 V, Load = 2 Ω, TEC Current = 1 A

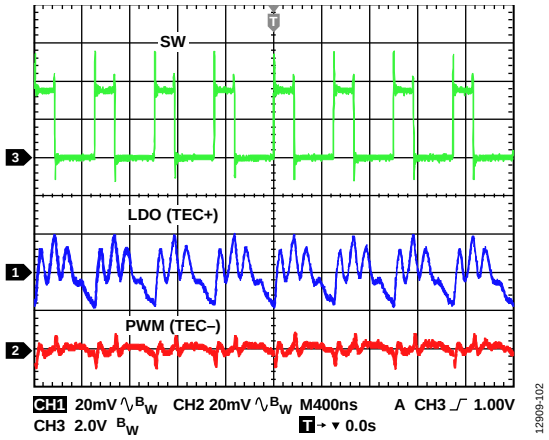


Figure 18. Typical Switch and Voltage Ripple Waveforms in Cooling Mode, V_{IN} = 3.3 V, Load = 2 Ω, TEC Current = 1 A

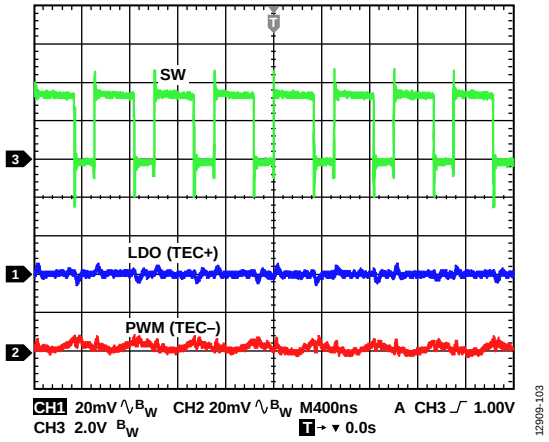


Figure 19. Typical Switch and Voltage Ripple Waveforms in Heating Mode, V_{IN} = 3.3 V, Load = 2 Ω, TEC Current = 1 A

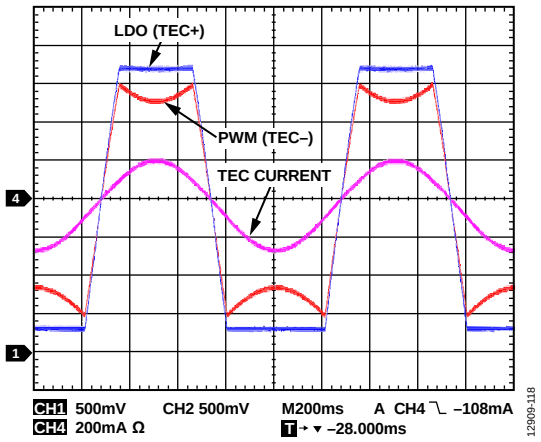


Figure 20. Cooling to Heating Transition

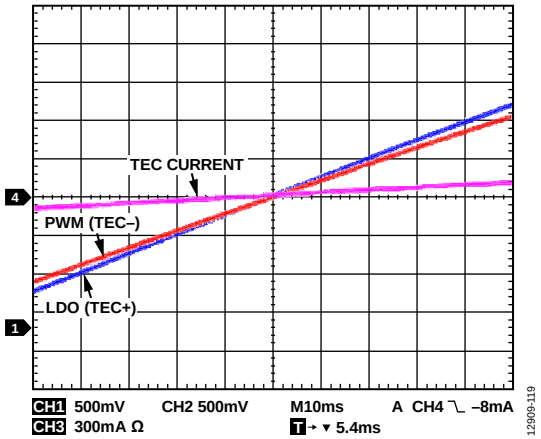


Figure 21. Zero Crossing TEC Current Zoom in from Heating to Cooling

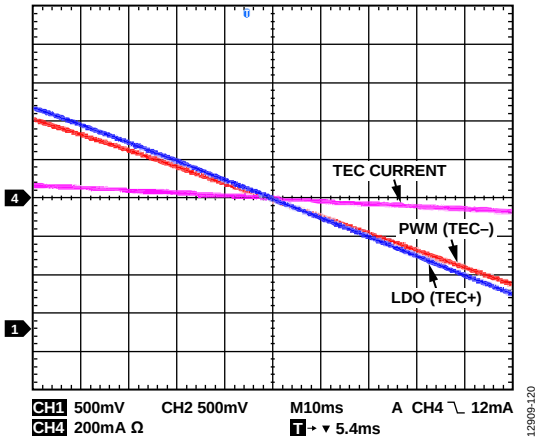


Figure 22. Zero Crossing TEC Current Zoom in from Cooling to Heating

DETAILED FUNCTIONAL BLOCK DIAGRAM

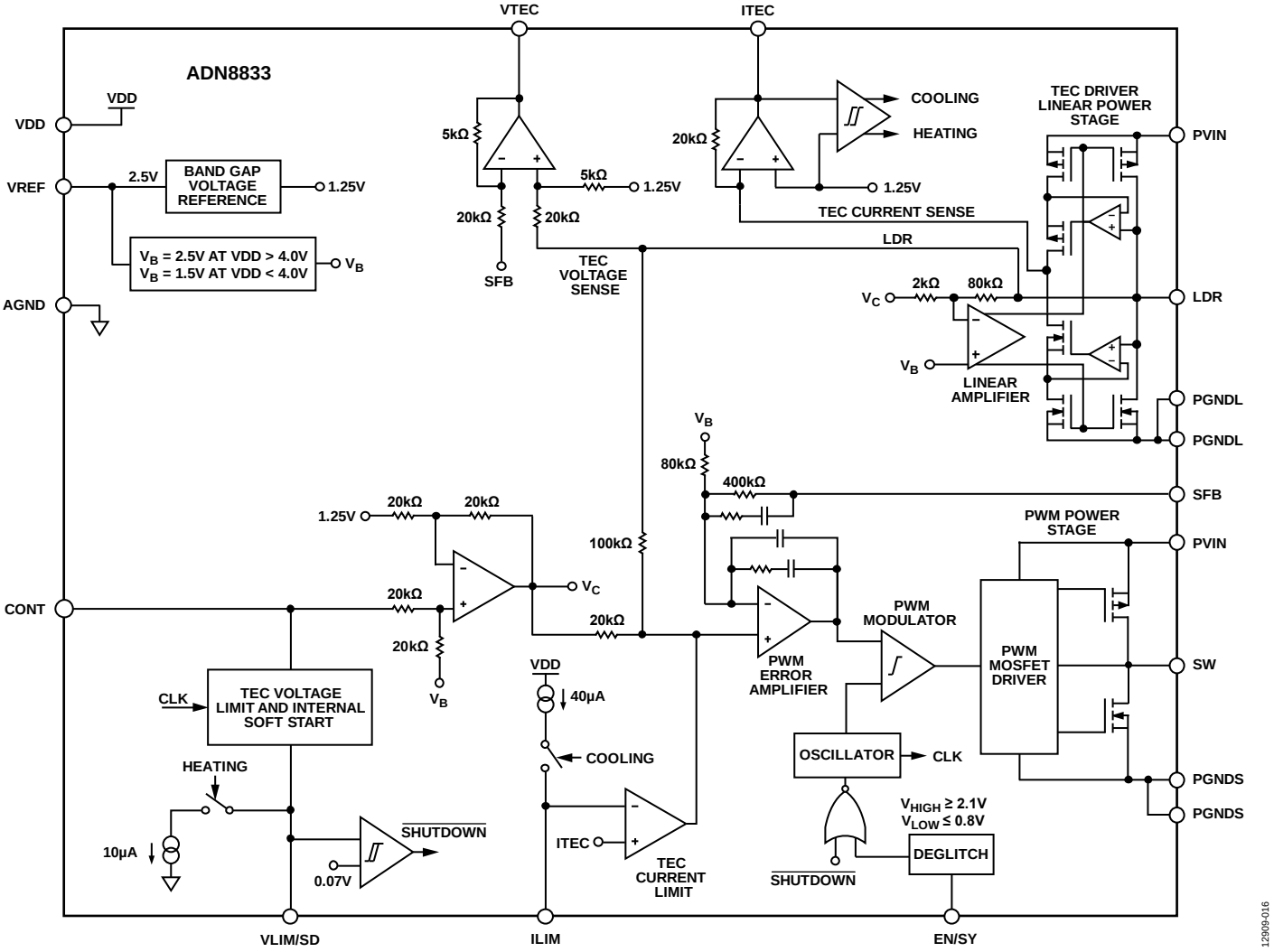


Figure 23. Detailed Functional Block Diagram of the ADN8833 in the WLCSP

THEORY OF OPERATION

The ADN8833 is a single chip TEC driver that sets and stabilizes a TEC temperature. A control voltage from a DAC applied to the CONT input of the ADN8833 corresponds to the temperature setpoint of the target object attached to the TEC. The ADN8833 controls an internal FET H-bridge whereby the direction of the current fed through the TEC can be either positive (for cooling mode) to pump heat away from the object attached to the TEC, or negative (for heating mode), to pump heat into the object attached to the TEC.

The objective temperature is measured with a thermal sensor attached to the TEC and the sensed temperature (voltage) is fed back to an ADC to close digital thermal control loop of the TEC. For the best overall stability, couple the thermal sensor close to the TEC. In most laser diode modules, a TEC and a NTC thermistor are already mounted in the same package to regulate the laser diode temperature.

The TEC is differentially driven in an H-bridge configuration. The ADN8833 drives its internal MOSFET transistors to provide the TEC current. To further improve the power efficiency of the system, only one side of the H-bridge uses a PWM driver. Only one inductor and one capacitor are required to filter out the switching frequency. The other side of the H-bridge uses a linear output without requiring any additional circuitry. This proprietary configuration allows the ADN8833 to provide efficiency of >90%. For most applications, a 1 µH inductor, a 10 µF capacitor, and a switching frequency of 2 MHz maintain less than 1% of the worst-case output voltage ripple across a TEC.

The maximum voltage across the TEC and the current flowing through the TEC are set by using the VLIM/SD and ILIM pins. The maximum cooling and heating currents can be set independently to allow asymmetric heating and cooling limits. For additional details, see the Maximum TEC Voltage Limit section and the Maximum TEC Current Limit section.

DIGITAL PID CONTROL

The ADN8833 is used in a software controlled PID loop. An amplifier conditions the signal from the thermistor and connects to an external temperature measurement ADC.

The signal from an external DAC that controls the temperature setpoint is applied to the CONT input pin.

POWERING THE DRIVER

The ADN8833 operates at an input voltage range of 2.7 V to 5.5 V that is applied to the VDD pin and the PVIN pin for the WLCSP (or the PVINS pin and PVINL pin for the LFCSP). The VDD pin is the input power for the driver and internal reference. The PVIN input power pins are combined for both the linear and the switching driver. Apply the same input voltage to all power input pins: VDD and PVIN. In some circumstances, an RC low-pass filter can be optionally added between the PVIN for the WLCSP (PVINS and PVINL for the LFCSP) and VDD pins to prevent high frequency noise from entering VDD, as shown in Figure 24. The capacitor and resistor values are typically 10 Ω and 100 nF, respectively.

When configuring power supply to the ADN8833, keep in mind that at high current loads, the input voltage may drop substantially due to a voltage drop on the wires between the front-end power supply and the PVIN for the WLCSP (PVINS and PVINL for the LFCSP) pin. Leave a proper voltage margin when designing the front-end power supply to maintain the performance. Minimize the trace length from the power supply to the PVIN for the WLVSP (PVINS and PVINL for the LFCSP) pin to help mitigate the voltage drop.

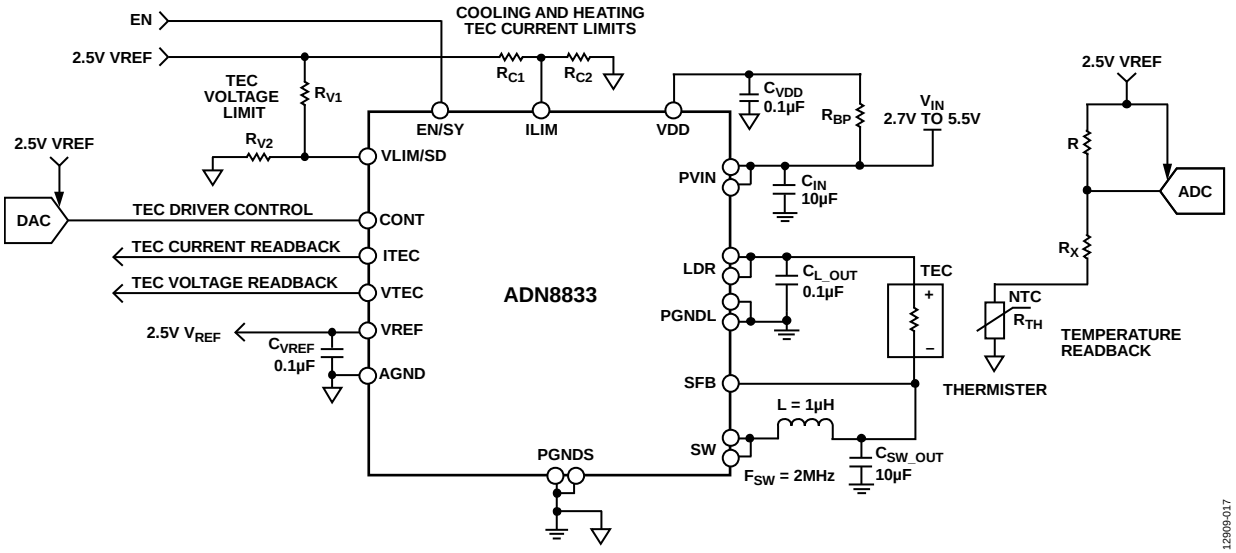


Figure 24. TEC Driver in a Digital Temperature Control Loop (WLCSP)

ENABLE AND SHUTDOWN

To enable the ADN8833, apply a logic high voltage to the EN/SY pin while the voltage at the VLIM/SD pin is above the maximum shutdown threshold of 0.07 V. If either the EN/SY pin voltage is set to logic low or the VLIM/SD voltage is below 0.07 V, the driver goes into an ultralow current state. The current drawn in shutdown mode is 350 µA typically. Most of the current is consumed by the VREF circuit block, which is always on even when the device is disabled or shut down. The device can also be enabled when an external synchronization clock signal is applied to the EN/SY pin and the voltage at VLIM/SD input is above 0.07 V. Table 6 shows the combinations of the two input signals that are required to enable the ADN8833.

Table 6. Enable Pin Combinations

EN/SY Input	VLIM/SD Input	Driver
>2.1 V	>0.07 V	Enabled
Switching between high >2.1 V and low < 0.8 V	>0.07 V	Enabled
<0.8 V	No effect[1]	Shutdown
Floating	No effect[1]	Shutdown
No effect[1]	≤0.07 V	Shutdown

[1] No effect means this signal has no effect in shutting down or in enabling the device.

OSCILLATOR CLOCK FREQUENCY

The ADN8833 has an internal oscillator that generates a 2.0 MHz switching frequency for the PWM output stage. This oscillator is active when the enabled voltage at the EN/SY pin is set to a logic level higher than 2.1 V and the VLIM/SD pin voltage is greater than the shutdown threshold of 0.07 V.

External Clock Operation

The PWM switching frequency of the ADN8833 can be synchronized to an external clock from 1.85 MHz to 3.25 MHz applied to the EN/SY input pin as shown on Figure 25.

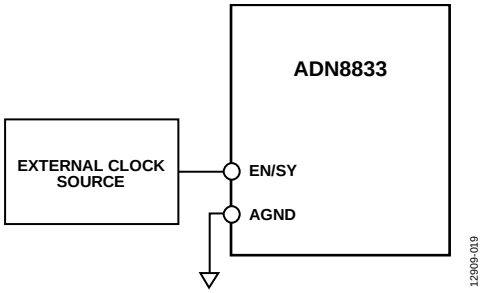


Figure 25. Synchronize to an External Clock

Connecting Multiple ADN8833 Devices

Multiple ADN8833 devices can be driven from a single master clock signal by connecting the external clock source to the EN/SY pin of each slave device. The input ripple can be greatly reduced by operating the ADN8833 devices 180° out of phase from each other by placing an inverter at one of the EN/SY pins, as shown in Figure 26.

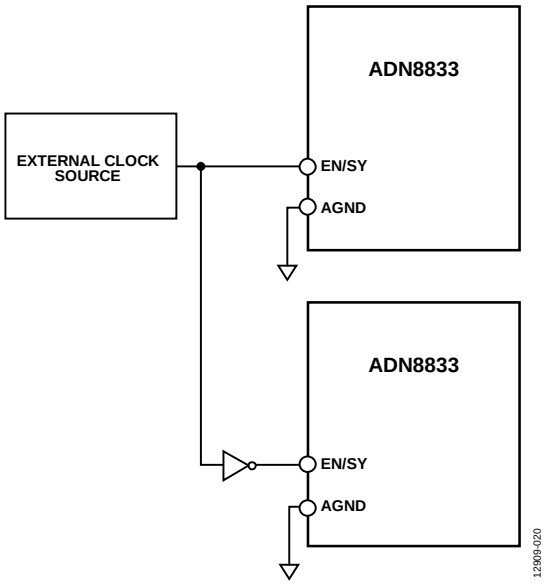


Figure 26. Multiple ADN8833 Devices Driven from a Master Clock

SOFT START ON POWER-UP

The ADN8833 has an internal soft start circuit that generates a ramp with a typical 150 ms profile to minimize inrush current during power-up. The settling time and the final voltage across the TEC depends on the TEC voltage required by the control voltage of voltage loop. The higher the TEC voltage is, the longer it requires to be built up.

When the ADN8833 is first powered up, the linear side discharges the output of any prebias voltage. As soon as the prebias is eliminated, the soft start cycle begins. During the soft start cycle, both the PWM and linear outputs track the internal soft start ramp until they reach midscale, where the control voltage, V_C, is equal to the bias voltage, V_B. From the midscale voltage, the PWM and linear outputs are then controlled by V_C and diverge from each other until the required differential voltage is developed across the TEC or the differential voltage reaches the voltage limit. The voltage developed across the TEC depends on the control point at that moment in time. Figure 27 shows an example of the soft start in cooling mode. Note that, as both the LDR and SFB voltages increase with the soft start ramp and approach V_B, the ramp slows down to avoid possible current overshoot at the point where the TEC voltage starts to build up.

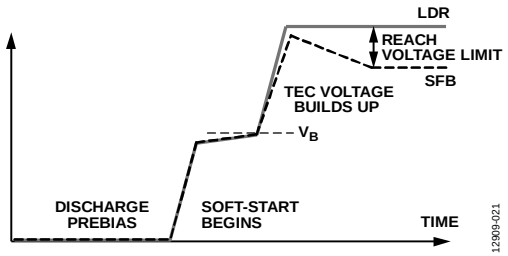


Figure 27. Soft Start Profile in Cooling Mode

TEC VOLTAGE/CURRENT MONITOR

The TEC real-time voltage and current are detectable at VTEC and ITEC, respectively.

Voltage Monitor

VTEC is an analog voltage output pin with a voltage proportional to the actual voltage across the TEC. A center VTEC voltage of 1.25 V corresponds to 0 V across the TEC. Convert the voltage at VTEC and the voltage across the TEC using the following equation:

$$V_{VTEC} = 1.25\ V + 0.25 \times (V_{LDR} - V_{SFB})$$

Current Monitor

ITEC is an analog voltage output pin with a voltage proportional to the actual current through the TEC. A center ITEC voltage of 1.25 V corresponds to 0 A through the TEC. Convert the voltage at ITEC and the current through the TEC using the following equations:

$$V_{ITEC\_COOLING} = 1.25\ V + I_{LDR} \times R_{CS}$$

where the current sense gain (R_{CS}) is 0.525 V/A.

$$V_{ITEC\_HEATING} = 1.25\ V - I_{LDR} \times R_{CS}$$

MAXIMUM TEC VOLTAGE LIMIT

The maximum TEC voltage is set by applying a voltage divider at the VLIM/SD pin to protect the TEC. The voltage limiter operates bidirectionally and allows the cooling limit to be different from the heating limit.

Using a Resistor Divider to Set the TEC Voltage Limit

Separate voltage limits are set using a resistor divider. The internal current sink circuitry connected to VLIM/SD draws a current when the ADN8833 drives the TEC in a heating direction, which lowers the voltage at VLIM/SD. The current sink is not active when the TEC is driven in a cooling direction; therefore, the TEC heating voltage limit is always lower than the cooling voltage limit.

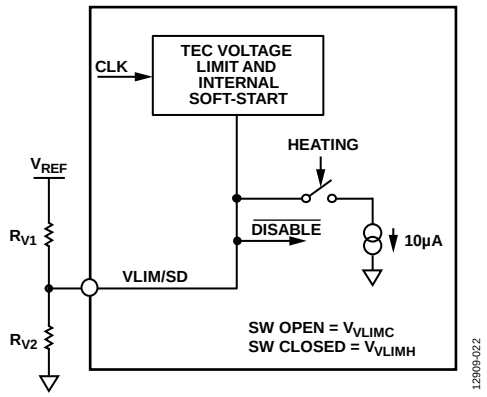


Figure 28. Using a Resistor Divider to Set the TEC Voltage Limit

Calculate the cooling and heating limits using the following equations:

$$V_{VLIM\_COOLING} = V_{REF} \times R_{V2}/(R_{V1} + R_{V2})$$

where V_{REF} = 2.5 V.

$$V_{VLIM\_HEATING} = V_{VLIM\_COOLING} - I_{SINK\_VLIM} \times R_{V1}||R_{V2}$$

where I_{SINK_VLIM} = 10 µA.

$$V_{TEC\_MAX\_COOLING} = V_{VLIM\_COOLING} \times A_{VLIM}$$

where A_{VLIM} = 2 V/V.

$$V_{TEC\_MAX\_HEATING} = V_{VLIM\_HEATING} \times A_{VLIM}$$

MAXIMUM TEC CURRENT LIMIT

To protect the TEC, separate maximum TEC current limits in cooling and heating directions are set by applying a voltage combination at the ILIM pin.

Using a Resistor Divider to Set the TEC Current Limit

The internal current sink circuitry connected to ILIM draws a 40 µA current when the ADN8833 drives the TEC in a cooling direction, which allows a high cooling current. Use the following equations to calculate the maximum TEC currents:

$$V_{ILIM\_HEATING} = V_{REF} \times R_{C2}/(R_{C1} + R_{C2})$$

where V_{REF} = 2.5 V.

$$V_{ILIM\_COOLING} = V_{ILIM\_HEATING} + I_{SINK\_ILIM} \times R_{C1}||R_{C2}$$

where I_{SINK_ILIM} = 40 µA.

$$I_{TEC\_MAX\_COOLING} = \frac{V_{ILIM\_COOLING} - 1.25\ V}{R_{CS}}$$

where R_{CS} = 0.525 V/A.

$$I_{TEC\_MAX\_HEATING} = \frac{1.25\ V - V_{ILIM\_HEATING}}{R_{CS}}$$

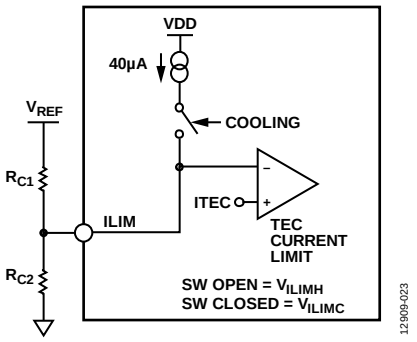


Figure 29. Using a Resistor Divider to Set the TEC Current Limit

$V_{ILIM\_HEATING}$ must not exceed 1.2 V and $V_{ILIM\_COOLING}$ must be more than 1.3 V to leave proper margins between the heating and the cooling modes.

APPLICATIONS INFORMATION

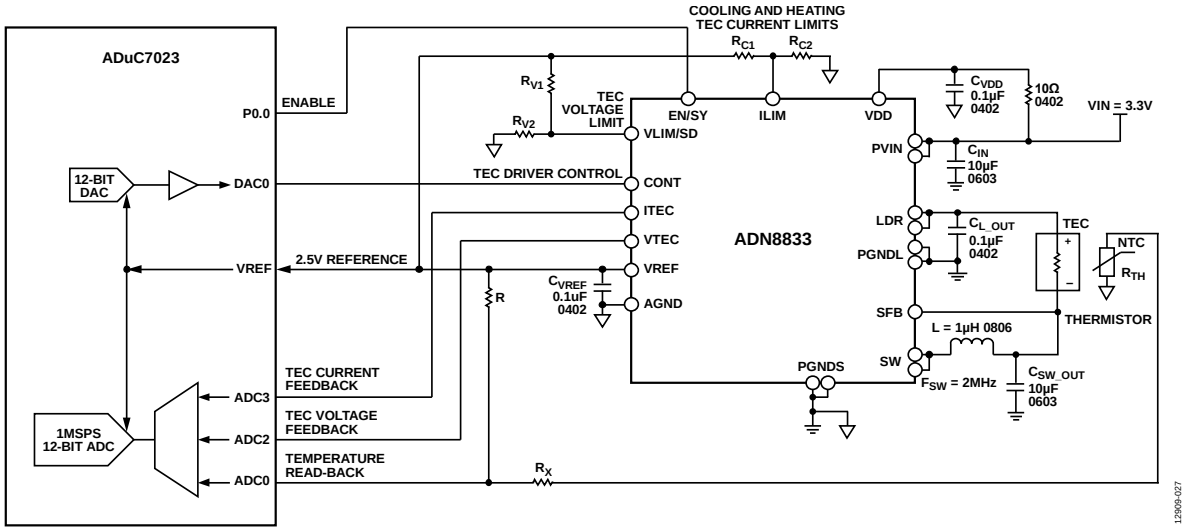


Figure 30. TEC Driver with Digital PID Based on the ADuC7023

TYPICAL APPLICATION WITH DIGITAL PID USING A DAC

The ADN8833 is designed for digital control systems. The thermistor input amplifier and compensation amplifier are to be implemented by the DAC, and the output from the compensation loop is fed to the CONT pin to close the temperature control loop. An example of an application circuit with the ADuC7023 is shown in Figure 30.

THERMISTOR SETUP

The thermistor has a nonlinear relationship to temperature; near optimal linearity over a specified temperature range can be achieved with the proper value of R_X placed in series with the thermistor.

First, the resistance of the thermistor must be known, where

- $R_{LOW} = R_{TH}$ at T_{LOW}
- $R_{MID} = R_{TH}$ at T_{MID}
- $R_{HIGH} = R_{TH}$ at T_{HIGH}

T_{LOW} and T_{HIGH} are the endpoints of the temperature range and T_{MID} is the average. In some cases, with only the β constant available, calculate R_{TH} using the following equation:

$$R_{TH} = R_R \exp\left\{\beta\left(\frac{1}{T} - \frac{1}{T_R}\right)\right\}$$

where:
R_{TH} is a resistance at T (K).
R_R is a resistance at T_R (K).

Calculate R_X using the following equation:

$$R_X = \left(\frac{R_{LOW}R_{MID} + R_{MID}R_{HIGH} - 2R_{LOW}R_{HIGH}}{R_{LOW} + R_{HIGH} - 2R_{MID}}\right)$$

MOSFET DRIVER AMPLIFIERS

The ADN8833 has two separate MOSFET drivers: a switched output or pulse-width modulated (PWM) amplifier, and a high gain linear amplifier. Each amplifier has a pair of outputs that drive the gates of the internal MOSFETs, which, in turn, drive the TEC as shown in Figure 33. A voltage across the TEC is monitored via the SFB and LDR pins. Although both MOSFET drivers achieve the same result, to provide constant voltage and high current, their operation is different. The exact equations for the two outputs are

$$V_{LDR} = V_B - 40(V_{CONT} - 1.25\text{ V})$$

$$V_{SFB} = V_{LDR} + 5(V_{CONT} - 1.25\text{ V})$$

where:
V_{CONT} is the voltage at CONT.
V_B is determined by V_{VDD} as

$V_B = 1.5$ V for $V_{VDD} < 4.0$ V

$V_B = 2.5$ V for $V_{VDD} > 4.0$ V

The compensation network that receives the temperature set voltage and the thermistor voltage fed by the input amplifier determines the voltage at CONT. V_{LDR} and V_{SFB} have a low limit of 0 V and an upper limit of V_{VDD}. Figure 31, Figure 32, and Figure 33 show the graphs of these equations.

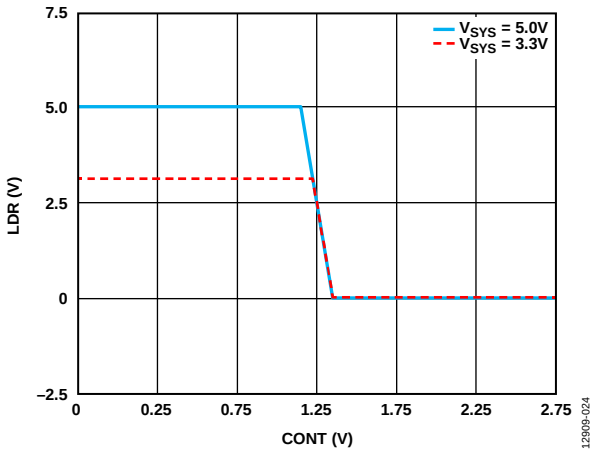


Figure 31. LDR Voltage vs. CONT Voltage

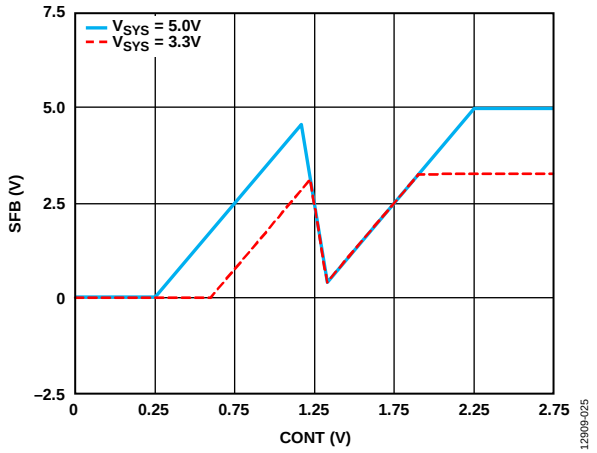


Figure 32. SFB Voltage vs. CONT Voltage

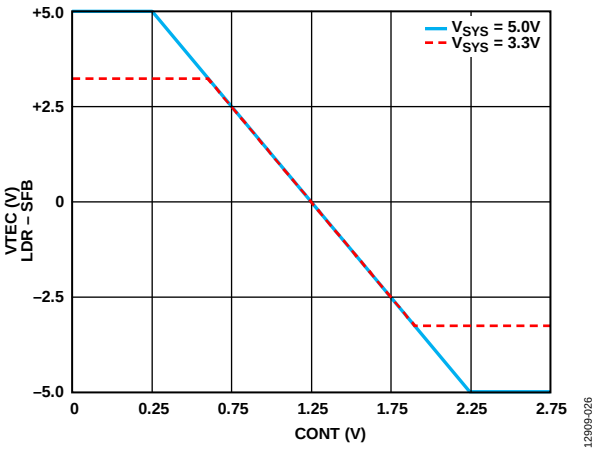


Figure 33. TEC Voltage vs. CONT Voltage

PWM OUTPUT FILTER REQUIREMENTS

A type three compensator internally compensates the PWM amplifier. As the poles and zeros of the compensator are designed by assuming the resonance frequency of the output LC tank being 50 kHz, the selection of the inductor and the capacitor must follow this guideline to ensure system stability.

Inductor Selection

The inductor selection determines the inductor current ripple and loop dynamic response. Larger inductance results in smaller current ripple and slower transient response as smaller inductance results in the opposite performance. To optimize the performance, a trade-off must be made between transient response speed, efficiency, and component size. Calculate the inductor value with the following equation:

$$L = \frac{V_{SW\_OUT} \times (V_{IN} - V_{SW\_OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

where:

V_{SW_OUT} is the PWM amplifier output.
f_{SW} is the switching frequency (2 MHz by default).
ΔI_L is the inductor current ripple.

A 1 µH inductor is typically recommended to allow reasonable output capacitor selection while maintaining a low inductor current ripple. If lower inductance is required, a minimum inductor value of 0.68 µH is suggested to ensure that the current ripple is set to a value between 30% and 40% of the maximum load current, which is 1.5 A.

Except for the inductor value, the equivalent dc resistance (DCR) inherent in the metal conductor is also a critical factor for inductor selection. The DCR accounts for most of the power loss on the inductor by DCR× I_{OUT}^2. Using an inductor with high DCR degrades the overall efficiency significantly. In addition, there is a conduct voltage drop across the inductor because of the DCR. When the PWM amplifier is sinking current in cooling mode, this voltage drives the minimum voltage of the amplifier higher than $0.06 \times V_{IN}$ by at least tenth of millivolts. Similarly, the maximum PWM amplifier output voltage is lower than $0.93 \times V_{IN}$. This voltage drop is proportional to the value of DCR and it reduces the output voltage range at the TEC.

When selecting an inductor, ensure that the saturation current rating is higher than the maximum current peak to prevent saturation. In general, ceramic multilayer inductors are suitable for low current applications due to small size and low DCR. When the noise level is critical, a shielded ferrite inductor may be used to reduce the electromagnetic interference (EMI).

Table 7. Recommended Inductors

Vendor	Value	Device No.	Footprint (mm)
Toko	1.0 µH ± 20%, 2.7 A (typical)	DFE201612P-H-1R0M	2.0 × 1.6
Taiyo Yuden	1.0 µH ± 20%, 2.2 A (typical)	MAKK2016T1R0M	2.0 × 1.6
Murata	1.0 µH ± 20%, 2.3 A (typical)	LQM2MPN1R0MGH	2.0 × 1.6

Capacitor Selection

The output capacitor selection determines the output voltage ripple, transient response, as well as the loop dynamic response of the PWM amplifier output. Use the following equation to select the capacitor:

$$C = \frac{V_{SW\_OUT} \times (V_{IN} - V_{SW\_OUT})}{V_{IN} \times 8 \times L \times (f_{SW})^2 \times \Delta V_{OUT}}$$

Note that the voltage caused by the product of current ripple, ΔI_L, and the capacitor equivalent series resistance (ESR) also add up to the total output voltage ripple. Selecting a capacitor with low ESR can increase overall regulation and efficiency performance.

Table 8. Recommended Capacitors

Vendor	Value	Device No.	Footprint (mm)
Murata	10 µF ± 10%, 10 V	ZRB18AD71A106KE01L	1.6 × 0.8
Murata	10 µF ± 20%, 10 V	GRM188D71A106MA73	1.6 × 0.8
Taiyo Yuden	10 µF ± 20%, 10 V	LMK107BC6106MA-T	1.6 × 0.8

INPUT CAPACITOR SELECTION

On the PVIN pin, the amplifiers require an input capacitor to decouple the noise and to provide the transient current to maintain stable input and output voltage. A 10 µF ceramic capacitor rated at 10 V is the minimum recommended value. Increasing the capacitance reduces the switching ripple that couples into the power supply but increases the capacitor size. Because the current at the input terminal of the PWM amplifier is discontinuous, a capacitor with low effective series inductance (ESL) is preferred to reduce voltage spikes.

In most applications, a decoupling capacitor is used in parallel with the input capacitor. The decoupling capacitor is usually a 100 nF ceramic capacitor with very low ESR and ESL, which provides better noise rejection at high frequency bands.

An RC low-pass filter can be optionally added between the PVIN and VDD pins to prevent high frequency noise from entering VDD, as shown in Figure 30. The capacitor and resistor values are typically 10 Ω and 100 nF, respectively.

POWER DISSIPATION

This section provides guidelines to calculate the power dissipation of ADN8833. Approximate the total power dissipation in the device by

$$P_{LOSS} = P_{PWM} + P_{LINEAR}$$

where:
P_{LOSS} is the total power dissipation in the ADN8833.
P_{LINEAR} is the power dissipation in the linear regulator.

PWM Regulator Power Dissipation

The PWM power stage is configured as a buck regulator and its dominant power dissipation (P_{PWM}) includes power switch conduction losses (P_{COND}), switching losses (P_{SW}), and transition losses (P_{TRAN}). Other sources of power dissipation are usually less significant at the high output currents of the application thermal limit and can be neglected in approximation.

Estimate the power dissipation of the buck regulator by

$$P_{LOSS} = P_{COND} + P_{SW} + P_{TRAN}$$

Conduction Loss (P_{COND})

The conduction loss consists of two parts: inductor conduction loss (P_{COND_L}) and power switch conduction loss(P_{COND_S}).

$$P_{COND} = P_{COND\_L} + P_{COND\_S}$$

Inductor conduction loss is proportional to the DCR of the output inductor, L. Using an inductor with low DCR enhances the overall efficiency performance. Use the following equation to estimate the inductor conduction loss:

$$P_{COND\_L} = \text{DCR} \times I_{OUT}^2$$

Power switch conduction losses are caused by the flow of the output current through both the high-side and low-side power switches, each of which has its own internal on resistance (R_{DSON}).

Use the following equation to estimate the amount of power switch conduction loss:

$$P_{COND\_S} = (R_{DSON\_HS} \times D + R_{DSON\_LS} \times (1 - D)) \times I_{OUT}^2$$

where:
R_{DSON_HS} is the on resistance of the high-side MOSFET.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
R_{DSON_LS} is the on resistance of the low-side MOSFET.

Switching Loss (P_{SW})

Switching losses are associated with the current drawn by the driver to turn the power devices on and off at the switching frequency. Each time a power device gate is turned on or off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground. Use the following equation to estimate the switching loss:

$$P_{SW} = (C_{GATE\_HS} + C_{GATE\_LS}) \times V_{IN}^2 \times f_{SW}$$

where:
C_{GATE_HS} is the gate capacitance of the high-side MOSFET.
C_{GATE_LS} is the gate capacitance of the low-side MOSFET.
f_{SW} is the switching frequency.

For the ADN8833, the total of (C_{GATE_HS} + C_{GATE_LS}) is approximately 1 nF.

Transition Loss (P_{TRAN})

Transition losses occur because the high-side MOSFET cannot turn on or off instantaneously. During a switch node transition, the MOSFET provides all the inductor current. The source-to-drain voltage of the MOSFET is half the input voltage, resulting in power loss. Transition losses increase with both load and input voltage and occur twice for each switching cycle. Use the following equation to estimate the transition loss:

$$P_{TRAN} = 0.5 \times V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
t_R is the rise time of the switch node.
t_F is the fall time of the switch node.

For the ADN8833, t_R and t_F are both approximately 1 ns.

Linear Regulator Power Dissipation

The power dissipation of the linear regulator is given by the following equation:

$$P_{LINEAR} = [(V_{IN} - V_{OUT}) \times I_{OUT}] + (V_{IN} \times I_{GND})$$

where:
V_{IN} and V_{OUT} are the input and output voltages of the linear regulator.
I_{OUT} is the load current of the linear regulator.
I_{GND} is the ground current of the linear regulator.

Power dissipation due to the ground current is generally small and can be ignored for the purposes of this calculation.

PCB LAYOUT GUIDELINES

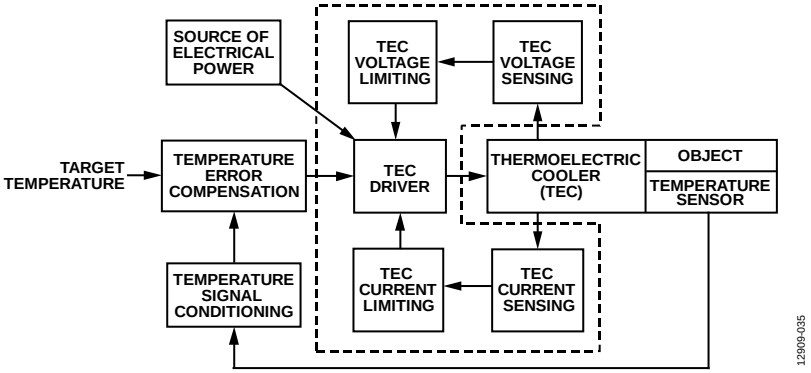


Figure 34. System Block Diagram

BLOCK DIAGRAMS AND SIGNAL FLOW

The ADN8833 integrates analog signal conditioning blocks, a load protection block, and a TEC driver power stage all in a single IC. To achieve the best possible circuit performance, attention must be paid to keep noise of the power stage from contaminating the sensitive analog conditioning and protection circuits. In addition, the layout of the power stage must be performed such that the IR losses are minimized to obtain the best possible electrical efficiency. The system block diagram of the ADN8833 is shown in Figure 34.

GUIDELINES FOR REDUCING NOISE AND MINIMIZING POWER LOSS

Each printed circuit board (PCB) layout is unique because of the physical constraints defined by the mechanical aspects of a given design. In addition, several other circuits work in conjunction with the TEC driver; these circuits have their own layout requirements, so there are always compromises that must be made for a given system. However, to minimize noise and keep power losses to a minimum during the PCB layout process, observe the following guidelines.

General PCB Layout Guidelines

Switching noise can interfere with other signals in the system; therefore, the switching signal traces must be placed away from the power stage to minimize the effect. If possible, place the ground plate between the small signal layer and power stage layer as a shield.

Supply voltage drop on traces is also an important consideration because it determines the voltage headroom of the TEC driver at high currents. For example, if the supply voltage from the front-end system is 3.3 V, and the voltage drop on the traces is 0.5 V, PVIN sees only 2.8 V, which limits the maximum voltage of the linear regulator as well as the maximum voltage across the TEC. To mitigate the voltage waste on traces and impedance interconnection, place the ADN8833 and the input decoupling components close to the supply voltage terminal. This placement not only improves the system efficiency, but also provides better regulation performance at the output.

To prevent noise signal from circulating through ground plates, reference all of the sensitive analog signals to AGND and connect AGND to PGNDS using only a single point connection. This ensures that the switching currents of the power stage do not flow into the sensitive AGND node.

PWM Power Stage Layout Guidelines

The PWM power stage consists of a MOSFET pair that forms a switch mode output that switches current from PVIN to the load via an LC filter. The ripple voltage on the PVIN pin is caused by the discontinuous current switched by the PWM side MOSFETs. This rapid switching causes voltage ripple to form at the PVIN input, which must be filtered using a bypass capacitor. Place a 10 µF capacitor as close as possible to the PVIN pin to connect PVIN to PGNDS. Because the 10 µF capacitor is sometimes bulky and has higher ESR and ESL, a 100 nF decoupling capacitor is usually used in parallel with it, placed between PVIN and PGNDS.

Because the decoupling is part of the pulsating current loop, which carries high di/dt signals, the traces must be short and wide to minimize the parasitic inductance. As a result, this capacitor is usually placed on the same side of the board as the ADN8833 to ensure short connections. If the layout requires that 10 µF capacitor be on the opposite side of the PCB, use multiple vias to reduce via impedance.

The layout around the SW node is also critical because it switches between PVIN and ground rapidly, which makes this node a strong EMI source. Keep the copper area that connects the SW node to the inductor small to minimize parasitic capacitance between the SW node and other signal traces. This helps minimize noise on the SW node due to excessive charge injection. However, in high current applications, the copper area may be increased reasonably to provide heat sink and to sustain high current flow.

Connect the ground side of the capacitor in the LC filter as close as possible to PGNDS to minimize the ESL in the return path.

Linear Power Stage Layout Guidelines

The linear power stage consists of a MOSFET pair that forms a linear amplifier, which operates in linear mode for very low output currents, and changes to fully enhanced mode for greater output currents.

Because the linear power stage does not switch currents rapidly like the PWM power stage, it does not generate noise currents. However, the linear power stage still requires a minimum amount of bypass capacitance to decouple its input.

Place a 100 nF capacitor that connects from PVIN to PGNDL as close as possible to the PVIN pin.

EXAMPLE PCB LAYOUT USING TWO LAYERS

Figure 35, Figure 36, and Figure 37 show an example ADN8833 WLCSP PCB layout that uses two layers. This layout example achieves a small solution size of approximately 18 mm^2 with all of the conditioning circuitry and PID included. Using more layers and blind vias allows the solution size to be reduced even further because more of the discrete components can relocate to the bottom side of the PCB.

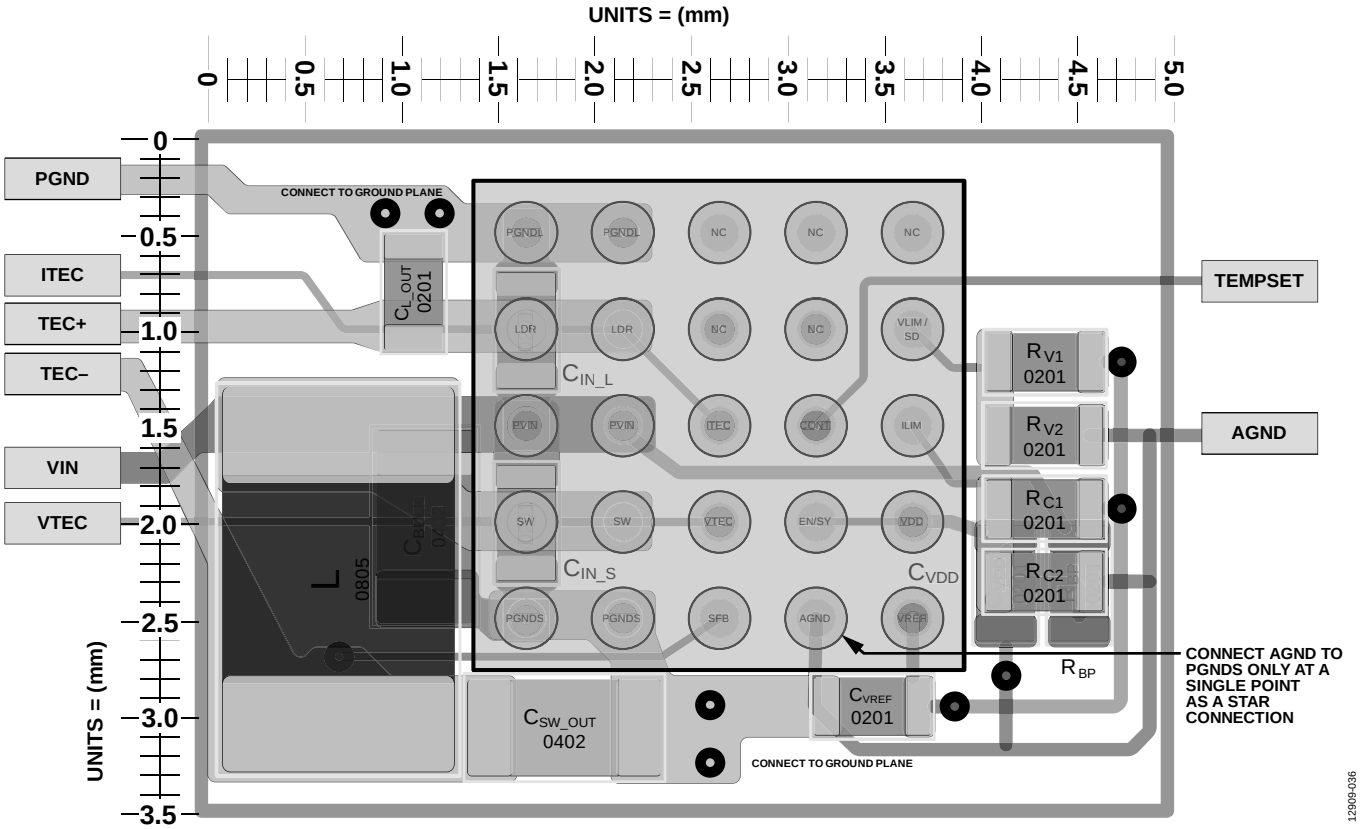


Figure 35. Example PCB Layout Using Two Layers (Top and Bottom Layers)

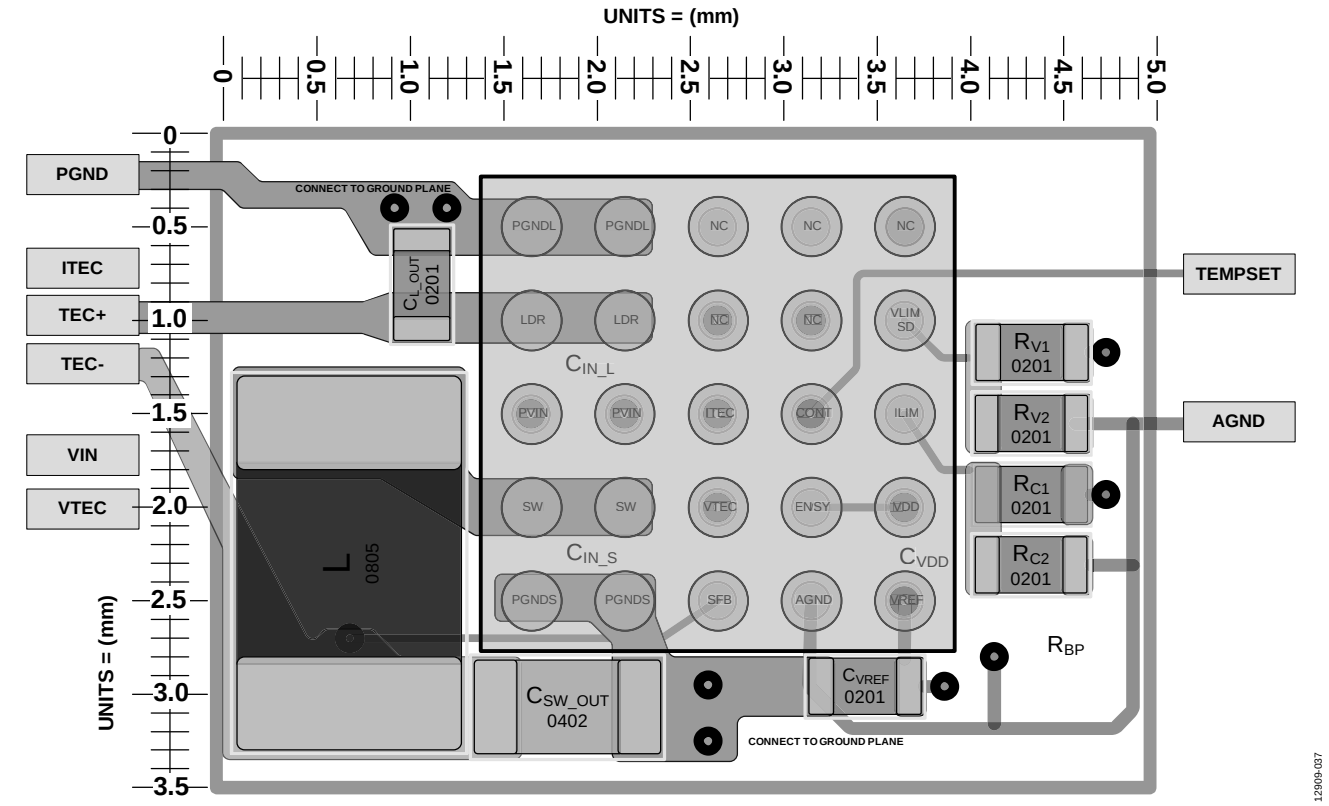


Figure 36. Example PCB Layout Using Two Layers (Top Layer Only)

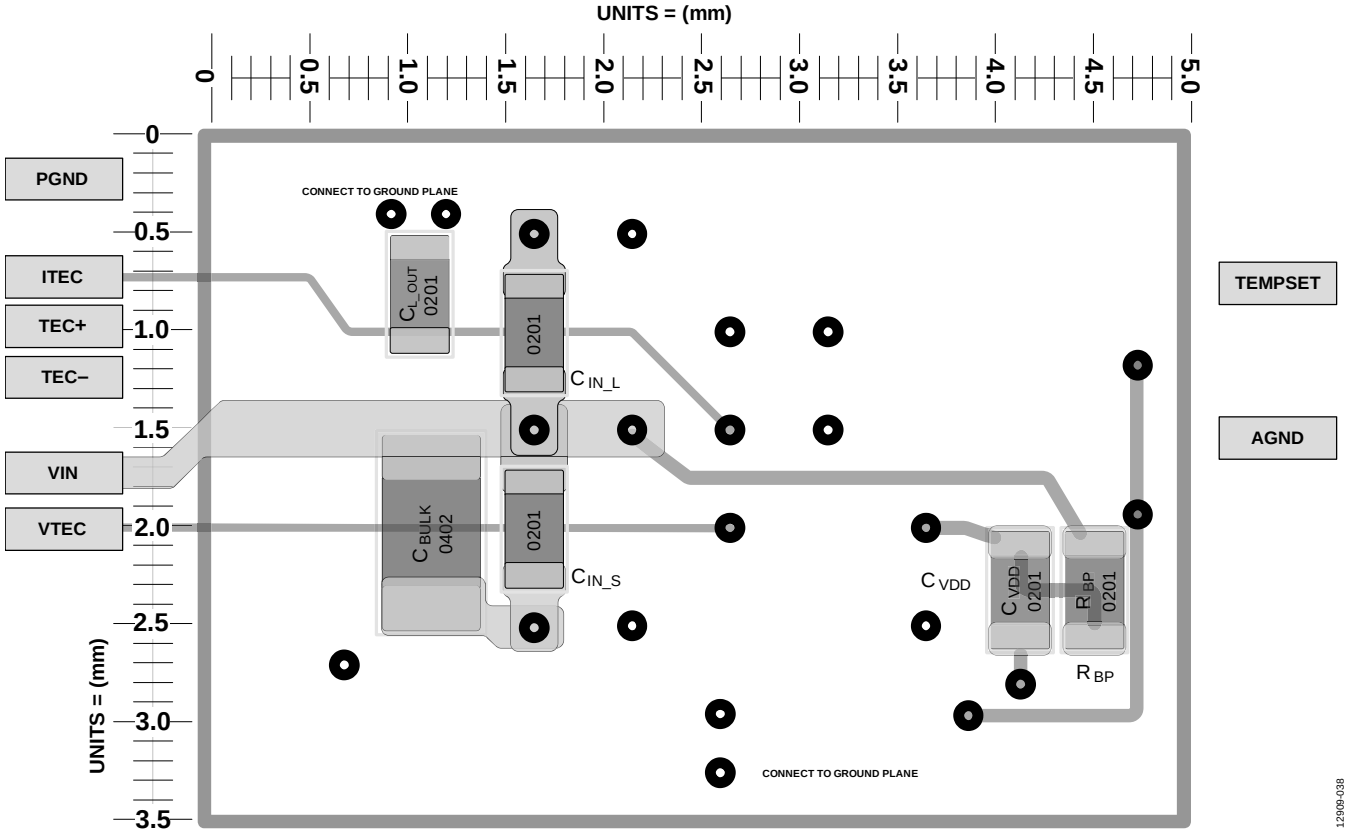


Figure 37. Example PCB Layout Using Two Layers (Bottom Layer Only)

OUTLINE DIMENSIONS

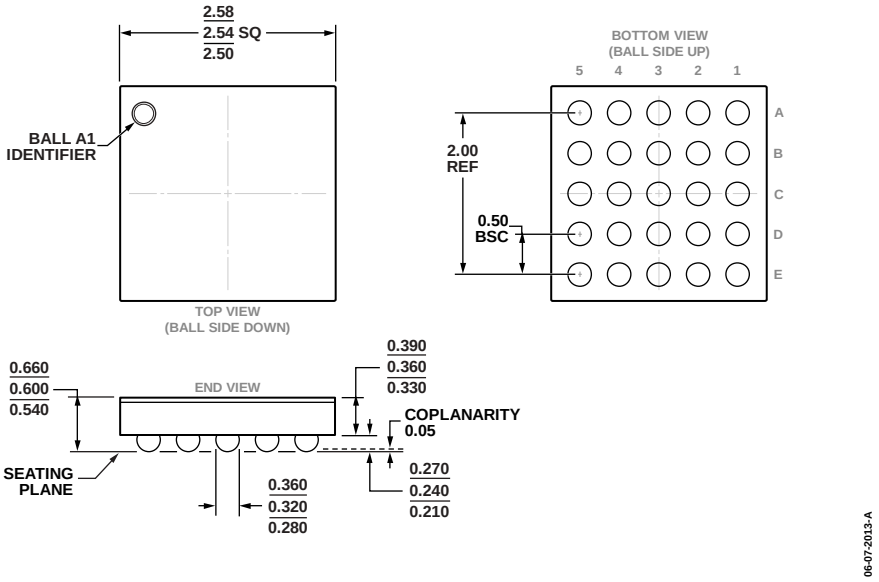
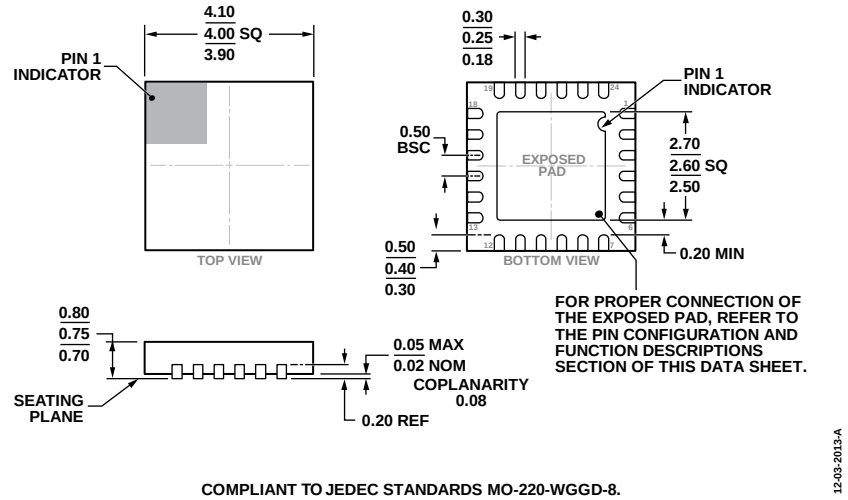


Figure 38. 25-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-25-7)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 39. 24-Lead Lead-frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
ADN8833ACBZ-R7	−40°C to +125°C	25-Ball Wafer Level Chip Scale Package [WLCSP]	CB-25-7
ADN8833CB-EVALZ		25-Ball WLCSP Evaluation Board: ±1 A TEC Current Limit, 3 V TEC Voltage Limit	
ADN8833ACPZ-R2	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-15
ADN8833ACPZ-R7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-15
ADN8833CP-EVALZ		24-Lead LFCSP Evaluation Board: ±1 A TEC Current Limit, 3 V TEC Voltage Limit	

[1] Z = RoHS Compliant Part.
[2] Operating junction temperature range. The ambient operating temperature range is −40°C to +85°C.

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