



# Precision, Low Noise, CMOS, Rail-to-Rail, Input/Output Operational Amplifier

Known Good Die

**AD8608-KGD**

## FEATURES

**Low offset voltage: 65  $\mu$ V maximum**  
**Low input bias currents: 1 pA maximum**  
**Low noise: 8 nV/ $\sqrt{\text{Hz}}$**   
**Wide bandwidth: 10 MHz**  
**High open-loop gain: 1000 V/mV**  
**Unity gain stable**  
**Single-supply operation: 2.7 V to 5.5 V**  
**Known good die (KGD): these die are fully guaranteed to data sheet specifications**

## APPLICATIONS

**Photodiode amplification**  
**Battery-powered instrumentation**  
**Multipole filters**  
**Sensors**  
**Barcode scanners**  
**Audio**

## GENERAL DESCRIPTION

The [AD8608-KGD](#)<sup>1</sup> is a single, rail-to-rail input and output, single-supply amplifier that features very low offset voltage, low input voltage and current noise, and wide signal bandwidth. The [AD8608-KGD](#) uses the Analog Devices, Inc. patented DigiTrim<sup>®</sup> trimming technique, which achieves superior precision without laser trimming.

The combination of low offsets, low noise, very low input bias currents, and high speed makes this amplifier useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion. Applications for this amplifier include optical control loops, portable and loop-powered instrumentation, and audio amplification for portable devices.

The [AD8608-KGD](#) is specified over the extended industrial temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ).

Additional application and technical information can be found in the [AD8605/AD8606/AD8608](#) data sheet.

<sup>1</sup> Protected by U.S. Patent No. 5,969,657.

Rev. 0

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**REVISION HISTORY**

4/15—Revision 0: Initial Version

## SPECIFICATIONS

## 5 V ELECTRICAL SPECIFICATIONS

$V_S = 5\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	$V_S = 3.5\text{ V}$ , $V_{CM} = 2.7\text{ V}$ $V_S = 5\text{ V}$ , $V_{CM} = 0\text{ V to } 5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		20	75	$\mu\text{V}$
				80	300	$\mu\text{V}$
					750	$\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	$\text{pA}$
					300	$\text{pA}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	$\text{pA}$
					75	$\text{pA}$
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		85	100	$\text{dB}$
				75	90	$\text{dB}$
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V to } 4.5\text{ V}$	300	1000		$\text{V/mV}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	6.0	$\mu\text{V}/^\circ\text{C}$
INPUT CAPACITANCE						
Common-Mode Input Capacitance	$C_{COM}$			8.8		$\text{pF}$
Differential Input Capacitance	$C_{DIFF}$			2.6		$\text{pF}$
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.96	4.98		V
			4.7	4.79		V
			4.6			V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $I_L = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		20	40	$\text{mV}$
				170	210	$\text{mV}$
					290	$\text{mV}$
Output Current	$I_{OUT}$		$\pm 80$			$\text{mA}$
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_v = 1$		1		$\Omega$
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	77	92		$\text{dB}$
			70	90		$\text{dB}$
Supply Current/Amplifier	$I_{SY}$	$I_{OUT} = 0\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	1.2	$\text{mA}$
					1.4	$\text{mA}$
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ , $C_L = 16\text{ pF}$		5		$\text{V}/\mu\text{s}$
Settling Time	$t_s$	To 0.01%, 0 V to 2 V step, $A_v = 1$		<1		$\mu\text{s}$
Unity Gain Bandwidth Product	GBP			10		$\text{MHz}$
Phase Margin	$\Phi_M$			65		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.3	3.5	$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		8	12	$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		6.5		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$

**2.7 V ELECTRICAL SPECIFICATIONS**

$V_S = 2.7\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_S = 3.5\text{ V}$ , $V_{CM} = 2.7\text{ V}$ $V_S = 2.7\text{ V}$ , $V_{CM} = 0\text{ V to } 2.7\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		20 80	75 300	$\mu\text{V}$ $\mu\text{V}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	$\mu\text{A}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	$\mu\text{A}$
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.7\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	80	95		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V to } 2.2\text{ V}$	110	350		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	6.0	$\mu\text{V}/^\circ\text{C}$
<b>INPUT CAPACITANCE</b>						
Common-Mode Input Capacitance	$C_{COM}$			8.8		pF
Differential Input Capacitance	$C_{DIFF}$			2.6		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.6 2.6	2.66		V V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		25	40 50	mV mV
Output Current	$I_{OUT}$			$\pm 30$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = 1$		1.2		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	77 70	92 90		dB dB
Supply Current/Amplifier	$I_{SY}$	$I_{OUT} = 0\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.15	1.4 1.5	mA mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$ , $C_L = 16\text{ pF}$		5		V/ $\mu\text{s}$
Settling Time	$t_s$	To 0.01%, 0 V to 1 V step, $A_V = 1$		<0.5		$\mu\text{s}$
Unity Gain Bandwidth Product	GBP			9		MHz
Phase Margin	$\Phi_M$			50		Degrees
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.3	3.5	$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		8	12	nV/ $\sqrt{\text{Hz}}$
	$e_n$	$f = 10\text{ kHz}$		6.5		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.01		pA/ $\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to $V_S$
Differential Input Voltage	6 V
Output Short-Circuit Duration to GND	Observe Derating Curves
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

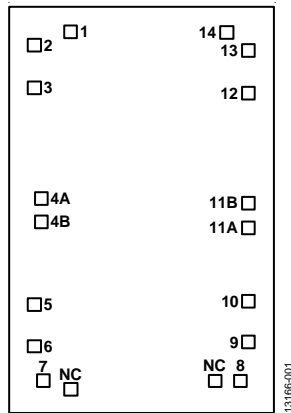


Figure 1. Pad Configuration

Table 4. Pad Function Descriptions

Pad	X-Axis ( $\mu\text{m}$ )	Y-Axis ( $\mu\text{m}$ )	Mnemonic	Pad Type	Description
1	-490	+1239	OUT A	Single	Output Channel A
2	-749	+1153	- IN A	Single	Inverting Input Channel A
3	-749	+853	+ IN A	Single	Noninverting Input Channel A
4A	-703	+85	V+ Supply	Double	Positive Supply Voltage
4B	-703	-84	V+ Supply	Double	Positive Supply Voltage, Double Bond Pad
5	-749	-659	+ IN B	Single	Noninverting Input Channel B
6	-749	-944	- IN B	Single	Inverting Input Channel B
7	-683	-1189	OUTB	Single	Output Channel B
8	+688	-1189	OUTC	Single	Output Channel C
9	+749	-916	- IN C	Single	Inverting Input Channel C
10	+749	-631	+ IN C	Single	Noninverting Input Channel C
11A	+749	-122	V- Supply	Double	Negative Supply Voltage
11B	+749	+47	V- Supply	Double	Negative Supply Voltage, Double Bond Pad
12	+749	+813	+ IN D	Single	Noninverting Input Channel D
13	+749	+1113	- IN D	Single	Inverting Input Channel D
14	+597	+1239	OUT D	Single	Output Channel D

# OUTLINE DIMENSIONS

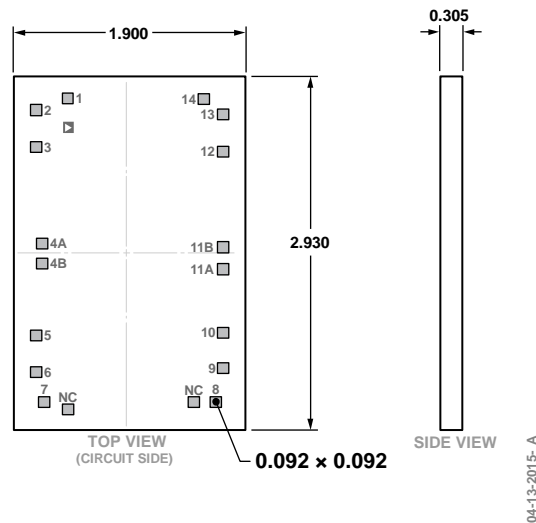


Figure 2. 14-Pad Bare Die [CHIP]  
(C-14-3)  
Dimensions shown in millimeters

## DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

Parameter	Value	Unit
Die Size (Maximum)	1900 × 2930	μm
Bond Pad Composition	AlCu (0.5%)	%
Bond Pad (Minimum)	92 × 92	μm
Passivation Type	OxyNitride	Not applicable
Thickness	305	μm
Backside Bias	GND	Not applicable
Scribe Line (Street) Width	100 × 150	μm
ESD	HBM 4000	V

Table 6. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Ablestik 84-1LMIS R4
Bonding Method	1 mil gold

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8608-KGD-CHIP	−40°C to +125°C	14-Pad Bare Die [CHIP]	C-14-3