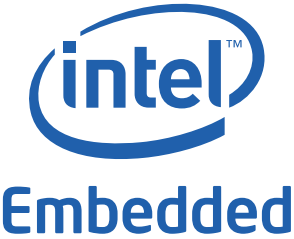

Intel® Platform Controller Hub EG20T

Datasheet

July 2012

Order Number: 324211-009US

Contents

Figures

Tables

Revision History

Date	Revision	Description
July 2012	009	Added Specification Changes and Document Changes from the Specification Update revision 011.
January 2012	008	Added Specification Changes and Document Changes from the Specification Update revision 008.
August 2011	007	Updated bit[3] acronym in Table 38, "78h: PCIe_DCT—PCIe Drive Control Register" on page 73 Added bit[4] description in Table 147, "A4h: BIST Control Register" on page 164 Updated Figure 164, "Intel® Platform Controller Hub EG20T Package (Side View)" on page 759
July 2011	006	Clarified context of "Packet Write Mode" in Section 4.1, "Overview" on page 113 Reworded the note in Section 4.1.2, "Serial ROM Address Map Structure" on page 113 and changed sections 4.2.4 through 4.2.7 to Section 4.2.3.1 through Section 4.2.3.4 Added link to Section 7.0 from Section 4.1.2.1, "Option ROM Space" on page 114 Clarified notes in Section 4.1.2.2, "Initialize Data Space" on page 114 Added note to Section 4.1.2.2.2, "Structure of Initialization of Subsystem ID or Subsystem Vendor ID" on page 115 Added Section 4.1.2.3, "Control Space" on page 116 Added link to the note for Figure 8, "Serial ROM Write Flowchart" on page 118 Updated Table 90, "00h: Status Register" on page 119 and Table 91, "04h: Serial ROM Interface Control Register" on page 120 Changed Data for Serial ROM Address 00Bh to 02h in Section 4.2.3.2, "Only MAC Address Set" on page 120 Clarified Table 92, "Clock Domains (Clock Inputs/Peripheral Clocks)" on page 123 Updated missing access type (RW) for bit[18] in Table 95, "500h: CLKCFG- Clock Configuration Register" on page 125 Added link to Section 6.0 from Section 5.5.1.2, "Internal BUS Clock of Each Function" on page 126 Updated title and bit[5] of Table 139, "00h: HBA Capabilities Register" on page 158 Added bit[4] to Table 144, "14h: Command Completion Coalescing Control" on page 162 Corrected SATA spec revision in Section 7.7.1, "Interoperability with SATA Gen1 Device" on page 206 Corrected default bits in Table 209, "54h: PWR_CNTL_STS - Power Management Control/Status Register" on page 222 Updated bit[3] of Table 329, "000h: Interrupt Status" on page 325 Updated bit[30] of Table 333, "008h: Mode" on page 330 Corrected description for MIIM operation bit in Table 356, "0E8h: MAC Address1 Load" on page 341 Added Section 10.5.1, "Compatibility with Intel® Ethernet Products" on page 367 Defined bit[6] set in Table 475, "00h: Control Register 0 (Enable/Mode/Direction Set)" on page 430 Corrected bit acronyms for bits[14:8] in Table 515, "0Ch: CANBITT- CAN Bit Timing Register" on page 456 Update bit[1] of Table 520, "24h: IFmCMASK: m = 1, 2 - IFm Command Mask Register" on page 460 Corrected examples for CAN bit timing in Section 13.5.11.6, "Calculating the Bit Timing Parameters " on page 497 Changed "massage" to "message" in seven places in Chapter 14.0, "IEEE1588" Updated Revision Identification (Rev ID) for A3 stepping • Table 112, "08h: RID— Revision Identification Register" on page 148 • Table 187, "08h: RID- Revision Identification Register" on page 215 • Table 258, "08h: RID- Revision Identification Register" on page 267 • Table 307, "08h: RID- Revision Identification Register" on page 317 • Table 455, "08h: RID- Revision Identification Register" on page 423 • Table 492, "08h: RID- Revision Identification Register" on page 446 • Table 634, "08h: RID- Revision Identification Register" on page 549 • Table 687, "08h: RID — Revision Identification Register" on page 604 • Table 726, "08h: RID- Revision Identification Register" on page 630 • Table 776, "08h: RID- Revision Identification Register" on page 665

Date	Revision	Description
July 2011 (Continued)	006	Added "BAR: MEM_BASE" to "Memory-Mapped I/O Registers" headings and change sections 9.3.1.2 through 9.3.1.8 to Section 9.3.1.2.1 through Section 9.3.1.2.7 • Table 3.2.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 89 • Table 3.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 100 • Table 7.2.3, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 144 • Table 7.3.3, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 158 • Table 8.2.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 211 • Table 8.3.2, "EHCI Registers (BAR: MEM_BASE)" on page 227 • Table 8.3.3, "OHCI Registers (BAR: MEM_BASE)" on page 242 • Table 9.2.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 262 • Table 9.3.1.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 273 • Table 10.3.3, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 313 • Table 10.4.3, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 325 • Table 11.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 370 • Table 11.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 381 • Table 12.2.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 419 • Table 12.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 430 • Table 13.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 442 • Table 13.4.2, "Memory-Mapped Registers (Control Registers, BAR: MEM_BASE)" on page 453 • Table 13.4.3, "Memory-Mapped Registers (Message Interface Register Sets, BAR: MEM_BASE)" on page 458 • Table 13.4.4, "Memory-Mapped Registers (Message Handler Registers, BAR: MEM_BASE)" on page 469 • Table 14.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 505 • Table 14.5.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 516 • Table 15.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 546 • Table 15.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 555 • Table 16.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 602 • Table 16.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 611 • Table 17.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 627 • Table 17.4.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 637 • Table 18.2.2, "Memory-Mapped Registers (BAR: MEM_BASE)" on page 662 • Table 18.3.2, "Memory-Mapped I/O Registers (BAR: MEM_BASE)" on page 671
June 2011	005	Added note to Section 4.1.2, "Serial ROM Address Map Structure" on page 113 Correct Byte Addr Offset in Section 4.1.2.2.1, "Structure of Initialization of MAC Address of Gigabit Ethernet" on page 115 and Section 4.1.2.2.2, "Structure of Initialization of Subsystem ID or Subsystem Vendor ID" on page 115 Corrected Section 4.2.1, "Operation Mode" on page 116 Added Section 9.5.2, "Hot Unplug/Plug" on page 301 Corrected Section 16.5.2, "Interrupt Setting Procedure" on page 619 Corrected Table 823, "Clock Input Characteristics" on page 711 Corrected Figure 162, "Ballout (Top View - Right Side)" on page 753
February 2011	004	Corrected Section 4.2.3.2, "Only MAC Address Set" on page 120 Corrected Section 4.2.3.4, "MAC Address & Subsystem ID or Subsystem Vendor ID Set" on page 121 Corrected Table 107, "Port Host Register Map" on page 145 Added new Section 7.3.3.39, "Test Register 2 (TESTR2)" on page 191 Added new Section 7.7, "Additional Clarifications" on page 206 Corrected Default Value in Table 710, "10h: IMASK — Interrupt Mask Register" on page 613 Updated Table 816, "DC Current Characteristics" on page 705

Date	Revision	Description
January 2011	003	Section 4.1.2.1, "Option ROM Space" on page 114 Section 4.1.2.2.1, "Structure of Initialization of MAC Address of Gigabit Ethernet" on page 115 Section 13.5.11.6, "Calculating the Bit Timing Parameters " on page 497 Table 750, "05h: LSR- Line Status Register" on page 639
October 2010	002	Section 10.4.2, "Frame Buffer" on page 353 Table 491, "06h: PCISTS- PCI Status Register" on page 445
September 2010	001	Initial release.

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1.0 Overview

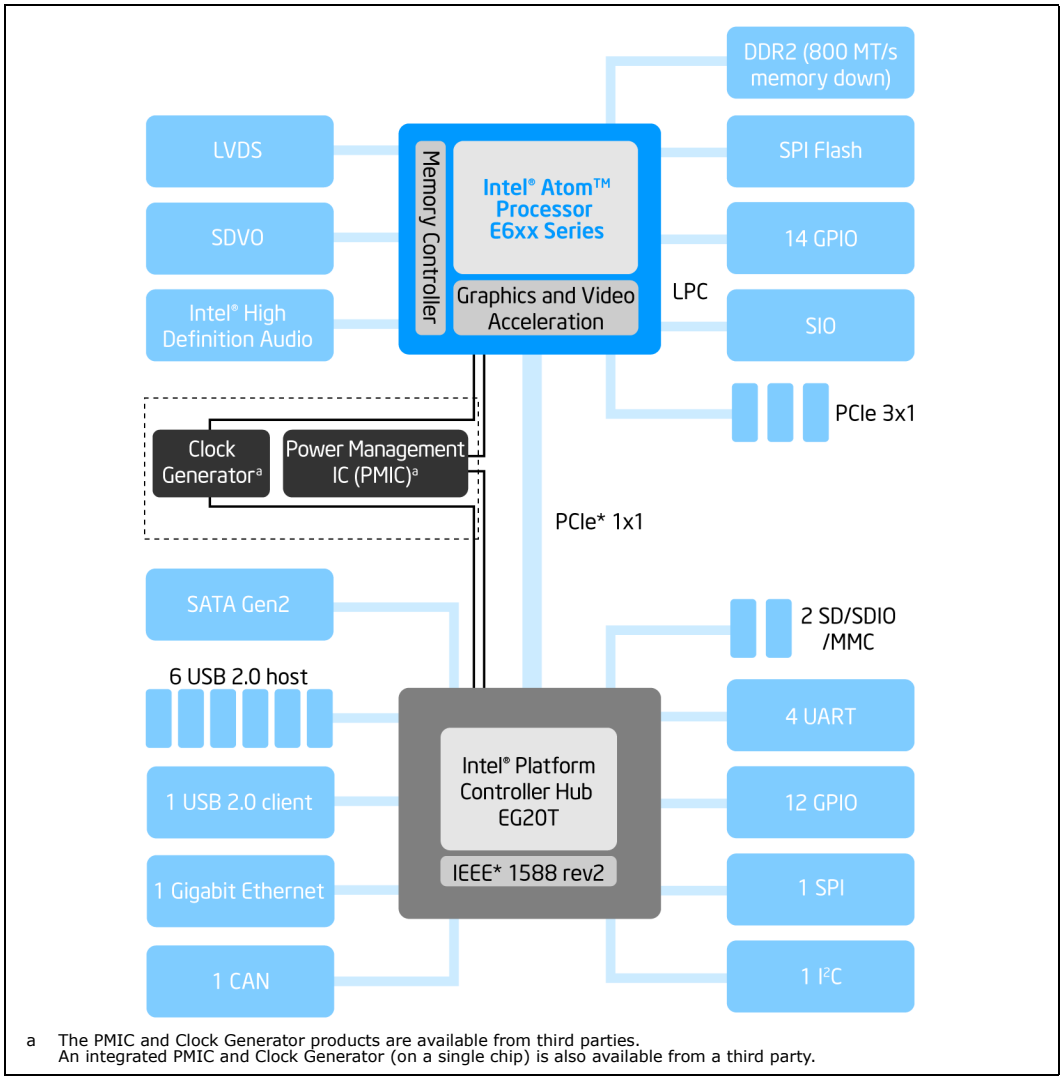
The Intel® Platform Controller Hub EG20T (also referred to as the Intel® PCH EG20T) integrates a range of common I/O blocks required in many market segments such as industrial automation, retail, gaming, and digital signage. These include SATA, USB host and device, SD/SDIO/MMC, Gigabit Ethernet MAC as well as general embedded interfaces such as CAN, IEEE* 1588, SPI, I2C, UART and GPIO. The Intel® PCH EG20T interfaces with the processor via a standard PCI Express* interface.

The Intel® PCH EG20T provides the functionality needed by operating systems such as Linux* or Microsoft Windows*. The Intel® PCH EG20T also provides functionality normally associated with handheld devices, such as support for the Secure Digital Input Output /Multi Media Card (SDIO/MMC) devices and Universal Serial Bus (USB) devices.

The Intel® PCH EG20T can be paired with the Intel® Atom™ Processor E6xx Series, which is the Intel® Architecture CPU for the small form factor ultra low power embedded segments based on a new architecture partitioning. The new architecture partitioning integrates the 3D graphics engine, memory controller and other blocks with the IA CPU core.

Figure 1 shows a system block diagram of an example system pairing the Intel® PCH EG20T with an Intel® Atom™ Processor E6xx Series. Section 1.2 provides an overview of the major features of the Intel® PCH EG20T.

Figure 1. System Block Diagram Example



a The PMIC and Clock Generator products are available from third parties.
An integrated PMIC and Clock Generator (on a single chip) is also available from a third party.

1.1 Reference Documents

Document	Document Number / Location
PCI Express Base Specification*, Rev. 1.0a *PCI Express* Base Specification,* Rev. 1.1 (2.5 Gbps) *PCI Express* to PCI/PCI-X Bridge Specification*, Revision 1.0 *PCI Power Management Specification*, Revision 1.1	http://www.pcisig.com/specifications
Serial ATA Specification, Rev. 2.6	http://www.sata-io.org
Serial ATA Advanced Host Controller Interface (AHCI) Specification, Rev. 1.1	http://www.intel.com/technology/serialata/ahci.htm
SD Host Controller Standard Specification ver. 1.0 *SD Memory Card Specifications Part 1 Physical Layer Specification ver. 2.0* *SDIO Card Specification ver. 1.10*	www.sdcard.org
MMC System Specification, ver. 4.1	www.jedec.org
I^2C Bus Specification, ver 2.1	www.nxp.com
Universal Serial Bus (USB) Specification, Revision 2.0 USB 1.1 specification, Release 1.0a	www.usb.org
USB 2.0 Enhanced Host Controller Interface Specification for Universal Serial Bus, Version 1.0	http://www.intel.com/technology/usb/ehcispec.htm
CAN Specification, Version 2.0	http://www.semiconductors.bosch.de
IEEE1588-2008 protocol IEEE 802.3 specification	http://standards.ieee.org/

1.2 Features

The Intel® PCH EG20T provides extensive I/O support:

- Peripheral Component Interconnect (PCI)-Express*
  - Fully compliant with all the required features of the PCI Express* 1.1 (2.5 Gbps) specification. It is used to connect to the Intel® Atom™ Processor E6xx Series.
  - Supports:
    - One PCI Express port with x1 link width
    - Ultra low transmit and receive latency and high accessible bandwidth
    - Polarity inversion
  - Max Transaction Layer Packet (TLP) payload size is 128 bytes.
- Universal Serial Bus (USB) Host
  - Conforms to Extended Host Controller Interface (EHCI) (1.0) and Open Host Controller Interface (OHCI) (1.0a)
  - Supports:
    - Six ports (2 USB 2.0 Hosts; 3 ports for each host)
    - Four types of data transfer: Control transfer, Bulk transfer, Interrupt transfer, and Isochronous transfer
  - Provides USB port that supports high-speed (480 Mbps), full-speed (12 MBPS), and low-speed (1.5 MBps) operations
  - Direct Memory Controller (DMA) controller is built in to the host controller
- Universal Serial Bus (USB) Device

- — Complies with USB 2.0 and USB 1.1 protocols
- — Supports:
  - — One port (1 USB device controller with 1 port)
  - — High-speed (480 MHz), and full-speed (12 MHz) operations
  - — Up to 4 IN and 4 OUT physical endpoints (EP0-3), which can be tied to different interfaces and configurations to achieve logical endpoints

Gigabit Ethernet Media Access Controller (GbE MAC)

- — Conforms to IEEE802.3
- — Supports:
  - — Auto CRC Adding function and the CRC Check function
  - — Auto Padding function and the Padding remove function
  - — Collision Detect function
  - — Burst Transfer function in the half-duplex mode
  - — Auto Extension function in the half-duplex mode
  - — Auto Transmission Stop function at pause packet reception
  - — Pause Packet Transmission function
  - — DMA function
- — Provides Media Independent Interface (MII) interface (10/100 BASE) and Reduced Gigabit Media Independent Interface (RGMII) or Gigabit Media Independent Interface (GMII) interface (1000 BASE)

- Serial Advanced Technology Attachment (SATA)
  - — Supports:
    - — SATA 1.5 Gbps Generation 1 speed and 3 Gbps Generation 2 speed
    - — Two ports (2 ports with 1 AHCI SATA Controller)
  - — Compliant with Serial ATA Specification 2.6, and AHCI Revision 1.1 specifications
  - — Provides internal DMA engine
- Secure Digital (SD) Host Controller
  - — Conforms to Secure Digital Host Controller (SDHC) speed class 6
  - — Supports:
    - — Two ports (2 SD host controllers; 1 port for each host)
    - — DMA function
    - — Secure Digital Association (SDA) standard (conforms to SD Host Controller Standard Specification ver. 1.0)
  - — Supports the following specifications:
    - — SD memory card: SD Memory Card Specifications Part 1 Physical Layer Specification ver. 2.0
    - — SDIO card: SDIO Card Specification ver. 1.10
    - — MMC: MMC System Specification ver. 4.1
  - — Supports the following transfer modes:
    - — SD memory card/SDIO card
    - — SD bus transfer mode (1-bit/4-bit/high-speed)
    - — MMC transfer mode (1-bit/4-bit/8-bit/high-speed)
  - — Supports the following SD option functions:

  - — Enable block stop, automatic clock stop, Auto_CMD12
  - — Supports the following SDIO option functions:
  - — Suspend, resume, wake-up, read wait
- IEEE1588 block (Clock Synchronization)
  - — Provides the hardware assist logic for achieving precision clock synchronization
  - — Conforms with the IEEE1588-2008 standard
  - — Supports:
    - — IEEE1588 over Ethernet (Interface is MII, GMII or RGMII)
    - — IEEE1588 over CAN
- Serial Peripheral Interface (SPI)
  - — Supports:
    - — Up to 5 Mbps
    - — Bus-master function (includes a shared DMA)
  - — Performs full-duplex data transfer
  - — Operates as master mode or slave mode
  - — Provides 16-stage FIFOs on the transmit side and the receive side
  - — Allows:
    - — Selection of 8-bit or 16-bit transfer size
    - — Interrupts to be set within a range of 1 to 16 according to the number of received bytes (words) and the number of not transmitted bytes (words)
    - — Selection of either LSB first or MSB first
    - — Selection of the polarity and phase of the serial clock
    - — Selection of synchronous clocks obtained by dividing the internal-clock (50 MHz=CLKL) by 2 and up to 2046 (1023 types)
    - — Control of the interval before and after transfer
    - — Detection of a mode fault error to prevent multi-master bus contention
    - — Detection of a write overflow error that occurs when data is written further in the transmit FIFO full state
  - — Indicates completion of transmission/reception and FIFO status with status bits
  - — Generates interrupts to handle various situations such as specific states of the transmit/receive FIFOs and mode fault errors
- Controller Area Network (CAN)
  - — Supports:
    - — CAN Protocol version 2.0B Active
    - — Bit rate up to 1 Mbit/s
    - — 32 message objects
    - — Priority control by each message object
    - — Detection/identification of bit error, stuff error, CRC error, form error, or acknowledge error
    - — Programmable loop-back mode for self-test operation
    - — DAR (Disabled Automatic Retransmission) mode for time triggered CAN applications
  - — No support for Bus-master function (Does not include a local DMA)
  - — Each message object has its own identifier mask

  - Each message object has its own direction mask
  - Each message object has its own extended mask
  - Each message object has its own NewDat mask
  - Provides programmable FIFO mode (concatenation of message objects)
- Inter – Integrated Circuit (I^2C) bus controller
  - Philips I^2C Bus Specification ver 2.1 conformed controller
  - Does not support bus-master function (does not include a local DMA)
  - Supports multi-master mode
  - Supports the following data transfer modes:
    - Standard mode (100 kHz)
    - Fast mode (400 kHz)
  - Compatible with 7-bit/10-bit address
  - Stops clocks to synchronize data between master and slave
  - The I^2C processing supports both transmitter and receiver functions (data width is 16 bits).
  - The I^2C transmitter supports master and slave devices
  - The I^2C receiver supports master and slave devices (selected by setting)
- Universal Asynchronous Receiver-Transmitter (UART) (8-wire interface)
  - SupportsL
    - One port
    - Bus-master function (includes a shared DMA)
    - All status report functions
    - Reduced interrupts to processor because of the use of 256-byte transmit and receive FIFOs
  - Interoperable with 16550
  - Provides full-duplex buffer system
  - Provides transmit, receive, and line-state data set interrupts and independent control of FIFO
  - Modem control signals are configured with CTS (Clear To Send), RTS (Request To Send), DSR (Data Set Ready), DTR (Data Terminal Ready), RI (Ring Indicator), and DCD (Data Carrier Detect)
  - Supports the following programmable serial interface characteristics:
    - 5, 6, 7 or 8-bit per character
    - Odd parity, even parity, and no-parity generation and verification
    - 1, 1.5 or 2 stop bits
  - Supports programmable baud rate generator (max baud rate: 4 Mbps)
- Universal Asynchronous Receiver Transmitter (UART) (2-wire interface)
  - Supports:
    - Three ports
    - Bus-master function (includes a shared DMA)
    - Full-duplex buffer system
    - Reduced interrupts to MPU because of the use of 64-byte transmit and receive FIFOs
    - Programmable baud rate generator (max baud rate: 1 Mbps)
  - Interoperable with 16550

  - — Provides all status report functions
  - — Provides transmit, receive, and line-state data set interrupts and independent control of FIFO
  - — Supports the following programmable serial interface characteristics
    - — 5,6,7 or 8-bit per character
    - — Odd parity, even parity, and no-parity generation and verification
    - — 1 or 1.5 or 2 stop bits
- GPIO
  - — 12–bit General purpose 12 GPIO ports.
  - — Input or output can be specified for each port.
  - — Interrupts can be used for all of the bits.
  - — Interrupt mask and interrupt mode (level/edge, positive logic/negative logic) can be set for all bits.
  - — GPIO0-7 correspond to WAKE-ON (GPIO8-11 does not correspond)
- JTAG
  - — Supports Boundary SCAN mode
- Serial ROM I/F
  - — Supports access to the Option ROM of each function
  - — Loading of a parameter required for initialization of each function (GbE MAC and SATA AHCI initialization)
  - — SPI interface

1.3 Devices and Functions

The Intel® PCH EG20T incorporates a variety of PCI functions as listed in Table 1.

Note: The Intel® PCH EG20T does not support function/port disabled for all the PCI functions listed in Table 1, even if the function/port is unused.

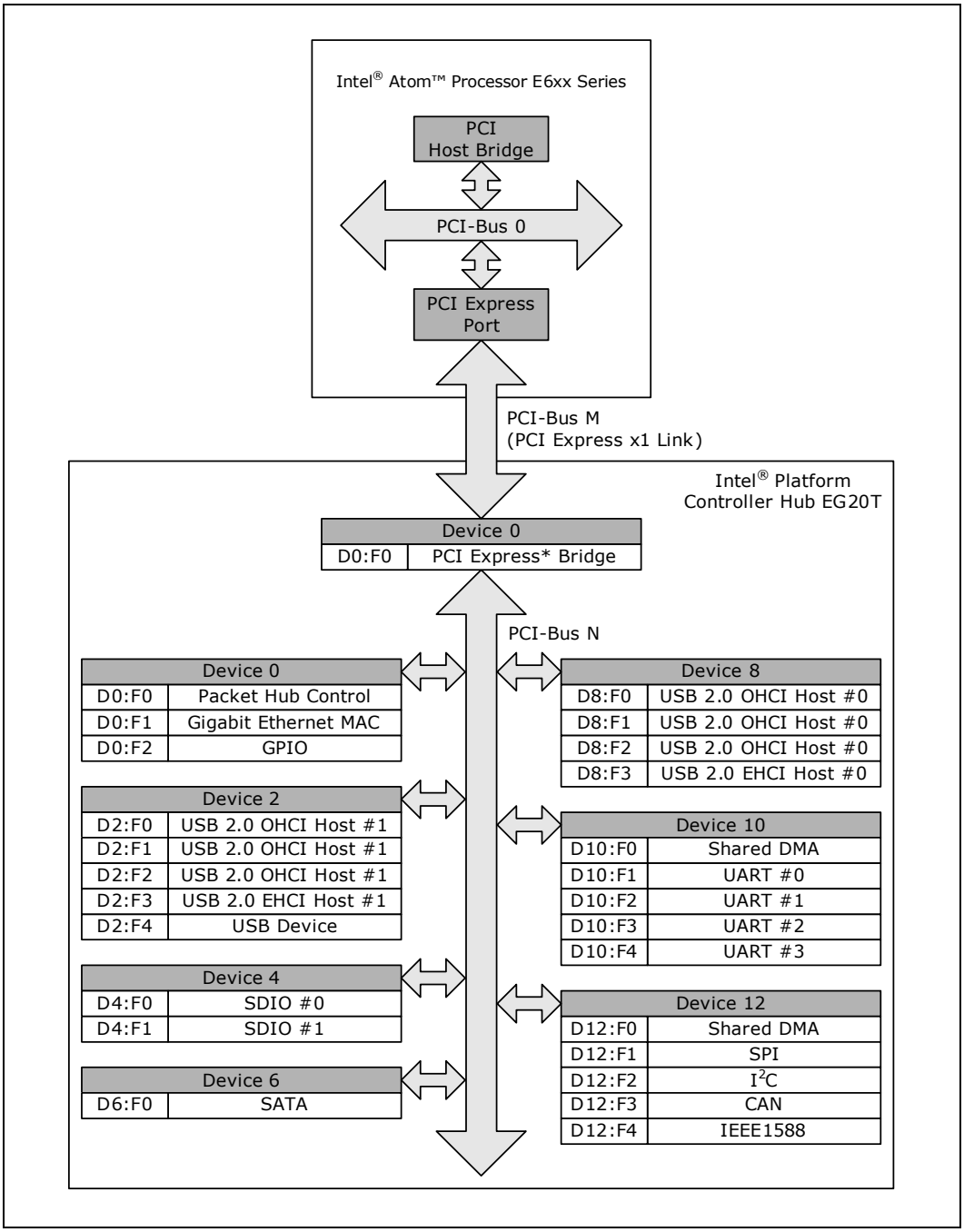
Table 1. PCI Devices and Functions (Sheet 1 of 2)

Vendor ID	8086h							
Function Name	Device No	Function No	BAR	Address Range	Bytes	Device ID	Support Device Power States	INTx
PCIe* Port	-	-	-	-	-	8800h	D0,D3hot	A
Packet Hub	D0	F0	[31:11]	0h - 7FCh	2048	8801h	D0,D3hot	-
GbE	D0	F1	[31:9]	0h - 1FCh	512	8802h	D0,D3hot	A
GPIO	D0	F2	[31:6]	0h - 3Ch	64	8803h	D0,D3hot	A
USB Host #1 (OHCI0)	D2	F0	[31:8]	0h – FCh	256	8804h	D0,D3hot	B
USB Host #1 (OHCI1)	D2	F1	[31:8]	0h – FCh	256	8805h	D0,D3hot	B
USB Host #1 (OHCI2)	D2	F2	[31:8]	0h – FCh	256	8806h	D0,D3hot	B
USB Host #1 (EHCI)	D2	F3	[31:8]	0h – FCh	256	8807h	D0,D3hot	B
USB Device	D2	F4	[31:13]	0h - 1FFCh	8192	8808h	D0,D3hot	B
SDIO #0	D4	F0	[31:9]	0h - 1FCh	512	8809h	D0,D3hot	C

Table 1. PCI Devices and Functions (Sheet 2 of 2)

Vendor ID	8086h							
Function Name	**Device No**	**Function No**	**BAR**	**Address Range**	**Bytes**	**Device ID**	**Support Device Power States**	**INTx**
SDIO #1	D4	F1	[31:9]	0h - 1FCh	512	880Ah	D0,D3hot	C
SATA II	D6	F0	[31:10]	0h - 3FCh	1024	880Bh	D0,D3hot	D
USB Host #0 (OHCI0)	D8	F0	[31:8]	0h – FCh	256	880Ch	D0,D3hot	A
USB Host #0 (OHCI1)	D8	F1	[31:8]	0h – FCh	256	880Dh	D0,D3hot	A
USB Host #0 (OHCI2)	D8	F2	[31:8]	0h – FCh	256	880Eh	D0,D3hot	A
USB Host #0 (EHCI)	D8	F3	[31:8]	0h – FCh	256	880Fh	D0,D3hot	A
DMA	D10	F0	[31:8]	0h – FCh	256	8810h	D0,D3hot	B
UART #0	D10	F1	[31:4]	0h – Fh	16	8811h	D0,D3hot	B
UART #1	D10	F2	[31:4]	0h – Fh	16	8812h	D0,D3hot	B
UART #2	D10	F3	[31:4]	0h – Fh	16	8813h	D0,D3hot	B
UART #3	D10	F4	[31:4]	0h – Fh	16	8814h	D0,D3hot	B
DMA	D12	F0	[31:8]	0h – FCh	256	8815h	D0,D3hot	C
SPI	D12	F1	[31:5]	0h - 1Ch	32	8816h	D0,D3hot	C
I^2C	D12	F2	[31:8]	0h – FCh	256	8817h	D0,D3hot	C
CAN	D12	F3	[31:9]	0h - 1FCh	512	8818h	D0,D3hot	C
IEEE1588 block	D12	F4	[31:8]	0h – FCh	256	8819h	D0,D3hot	C

Figure 2. Intel® Platform Controller Hub EG20T Internal Topology Block Diagram



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2.0 PCI Express* Bridge

2.1 Overview

The PCI Express* Bridge is connected with the external PCI Express pins. The connection of the PCI Express Bridge with the Packet Hub requires an internal PCI-compatible bus.

This bridge implements the following features:

- From the upstream / Root Complex (RC) side, the peripheral looks like a PCI device or a PCI function, which is connected with PCI.
- The PCI Express maximum TLP payload size is 128 bytes.
- Supports the Power management operation (L1 and L3 mode)
- Supports the Electrical Idle operation (including L0s mode)

2.2 Additional Clarification

The Request ID of Request Packet (Memory Read Request, Memory Write Request) differs from the standard PCIe/PCI Bridge specification.

Specification:

- The request ID of the packet output by the PCIe bridge is:
  - — device number = 0
  - — function number = 0

The Intel® PCH EG20T PCIe bridge:

- Request-ID of the packet output by the PCIe bridge is:
  - — device number = requested device's device number
  - — function number = requested device's function number

2.3 Register Address Map

2.3.1 PCI Configuration Registers

Table 2 lists the PCI Configuration Registers.

Table 2. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h-01h	Vendor Identification Register	VID	RO	8086h
02h-03h	Device Identification Register	DID	RO	8800h
04h-05h	PCI Command Register	PCICMD	RO, RW	0000h
06h-07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h
09h-0Bh	Class Code Register	CC	RO	060400h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	01h

† These registers related to Prefetchable Memory Space should be used as the initial value.

Table 2. PCI Configuration Registers (Sheet 2 of 2)

Offset	Name	Symbol	Access	Initial Value
18h	Primary Bus Number	PBN	RW	00h
19h	Secondary Bus Number	SDBN	RW	00h
1Ah	Subordinate Bus Number	SBBN	RW	00h
1Bh	Secondary latency timer	SDLT	RO	00h
1Ch	I/O Base	IOBS	RW, RO	01h
1Dh	I/O Limit	IOLMT	RW, RO	01h
1Eh-1Fh	Secondary Status	SDSTS	RWC, RO	0000h
20h-21h	Memory Base	MBS	RW, RO	0000h
22h-23h	Memory Limit	MLMT	RW, RO	0000h
24h-25h	Prefetchable Memory Base†	PMBS	RW, RO	0001h
26h-27h	Prefetchable Memory Limit†	PMLMT	RW, RO	0001h
28h-2Bh	Prefetchable Base Upper 32-bit†	PMUBS	RW	00000000h
2Ch-2Fh	Prefetchable Limit Upper 32-bit†	PMULMT	RW	00000000h
30h-31h	I/O Base upper 16-bit	IOUBS	RW	0000h
32h-33h	I/O Limit upper 16-bit	IOULMT	RW	0000h
34h-34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	01h
3E-3Fh	Bridge Control Register	BRG_CTL	RW,RO	0000h
40h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
41h	Next Item Pointer #1 Register	NXT_PTR1	RO	70h
42h-43h	Power Management Capabilities Register	PM_CAP	RO	DA02h
44h-45h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW, RWC	0000h
70h	PCI Express Capability ID Register	PCIe_CAPID	RO	10h
71h	PCI Express Next Item Pointer Register	PCIe_NPR	RO	00h
72h-73h	PCI Express Capabilities Register	PCIe_CP	RO	0072h
74h-77h	PCI Express Device Capabilities	PCIe_DCP	RO	00008020h
78h-79h	PCI Express Device Control	PCIe_DCT	RO, RW, RWS	2010h
7Ah-7Bh	PCI Express Device Status	PCIe_DST	RO, RWC	0000h
7Ch-7Fh	PCI Express Link Capabilities	PCIe_LCP	RO	00033C11h
80h-81h	PCI Express Link Control	PCIe_LCT	RW, RO	0000h
82h-83h	PCI Express Link Status	PCIe_LST	RWC, RO	1011h
94h-97h	PCI Express Device Capabilities 2	PCIe_DCP2	RO	00000000h
98h-99h	PCI Express Device Control 2	PCIe_DCT2	RO	0000h
A0h-A1h	PCI Express Link Control 2	PCIe_LCT2	RW, RO	0000h
A2h-A3h	PCI Express Link Status 2	PCIe_LST2	RO	0000h

† These registers related to Prefetchable Memory Space should be used as the initial value.

2.4 PCI Configuration Registers

This section describes the PCI Configuration Registers.

2.4.1 VID— Vendor Identification Register

Table 3. 00h: VID- Vendor Identification Register

Size: 16-bit			**Default:** 8086h	**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 00h **Offset End:** 01h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :00	8086h	RO	VID	**Vendor ID (VID):** This is a 16-bit value assigned to Intel.

2.4.2 DID— Device Identification Register

Table 4. 02h: DID— Device Identification Register

Size: 16-bit			**Default:** 8800h	**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 02h **Offset End:** 03h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :00	8800h	RO	DID	**Device ID (DID):** This is a 16-bit value assigned to the PCIe-Bridge. PCIe-Bridge (D0:F0): 8800h

2.4.3 PCICMD— PCI Command Register

Table 5. 04h: PCICMD— PCI Command Register (Sheet 1 of 2)

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 04h **Offset End:** 05h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :11	00000b	RO		**Reserved**[1]
10	0b	RW	ITRPDS	**Interrupt Disable:** 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		**Reserved**[1]
08	0b	RW	SERR	**SERR# enable:** Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0b	RO		**Reserved**[1]
06	0b	RW	PER	**Parity Error Response:** This bit is hardwired to 0.
05 :03	000b	RO		**Reserved**[1]

Table 5. 04h: PCICMD— PCI Command Register (Sheet 2 of 2)

Size: 16-bit		**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 04h **Offset End:** 05h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
02	0b	RW	BME	**Bus Master Enable (BME):** This bit controls that a device serves as a bus master. 0 = Disable 1 = Enable
01	0b	RW	MSE	**Memory Space Enable (MSE):** This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the PCIe-Bridge memory-mapped registers. The Base Address register for PCIe-Bridge should be programmed before this bit is set.
00	0b	RW	IOSE	**I/O Space Enable (IOSE):** This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the PCIe-Bridge I/O registers. The Base Address register for PCIe-Bridge should be programmed before this bit is set.

Notes:
1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

2.4.4 PCISTS—PCI Status Register

Table 6. 06h: PCISTS—PCI Status Register (Sheet 1 of 2)

Size: 16-bit		**Default:** 0010h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 06h **Offset End:** 07h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15	0b	RWC	DPE	**Detected Parity Error**
14	0b	RWC	SSE	**Signaled System Error:** This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = Don't send error message 1 = Send error message
13	0b	RWC	RMA	**Received Master Abort:** Primary received Unsupported Request Completion Status. 0 = De-assert 1 = Assert
12	0b	RWC	RTA	**Received Target Abort**: Primary received Abort Completion Status 0 = De-assert 1 = Assert
11	0b	RWC	STA	**Signaled Target Abort:** Primary transmitted Abort Completion Status 0 = De-assert 1 = Assert
10 :09	00b	RO		Reserved[1]
08	0b	RWC	MDPE	**Master Data Parity Error**
07 :05	000b	RO		Reserved[1]
04	1b	RO	CPL	**Capabilities List**: This bit indicates the presence of a capabilities list.

Table 6. 06h: PCISTS—PCI Status Register (Sheet 2 of 2)

Size: 16-bit			**Default:** 0010h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 06h **Offset End:** 07h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
03	0b	RO	ITRPSTS	**Interrupt Status:** This bit reflects the status of the function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.	
02 :00	000b	RO		Reserved[1]	

Notes:
1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

2.4.5 RID— Revision Identification Register

Table 7. 08h: RID— Revision Identification Register

Size: 8-bit			**Default:** 01h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 08h **Offset End:** 08h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	01h	RO	RID	**Revision ID**: Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.	

2.4.6 CC— Class Code Register

Table 8. 09h: CC— Class Code Register

Size: 24-bit			**Default:** 060400h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 09h **Offset End:** 0Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
23 :16	06h	RO	BCC	**Base Class Code (BCC):** 06h = Bridge	
15 :08	04h	RO	SCC	**Sub Class Code (SCC):** 04h = PCI to PCI	
07 :00	00h	RO	PI	**Programming Interface (PI):** 00h = Not categorized	

2.4.7 MLT— Master Latency Timer Register

Table 9. 0Dh: MLT— Master Latency Timer Register

Size: 8-bit			Default: 00h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 0Dh Offset End: 0Dh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	00h	RO	MLT	**Master Latency Timer (MLT):** Hardwired to 00h. The PCIe-Bridge is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.	

2.4.8 HEADTYP— Header Type Register

Table 10. 0Eh: HEADTYP— Header Type Register

Size: 8-bit			Default: 01h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 0Eh Offset End: 0Eh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07	0b	RO	MFD	**Multi-Function Device:** 0 = Single-function device.	
06 :00	0000001b	RO	CONFIGLAYOUT	**Configuration Layout:** Hardwired to 01h, which indicates the standard PCI configuration layout.	

2.4.9 PBN— Primary Bus Number Register

Table 11. 18h: PBN— Primary Bus Number Register

Size: 8-bit			Default: 00h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 18h Offset End: 18h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	00h	RW[1]	PBN	**Primary Bus Number (PBN)**: This register is used to record the Bus Number of the logical PCI bus segment to which the primary interface of the bridge is connected.	

Notes:
1. "Primary Bus Number register" is written by "Configuration Write". The bytes written in is the "0" byte of Requester ID of the header.

2.4.10 SDBN— Secondary Bus Number Register

Table 12. 19h: SDBN— Secondary Bus Number Register

Size: 8-bit			**Default:** 00h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 19h **Offset End:** 19h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	00h	RW	SDBN	**Secondary Bus Number (SDBN)**: This register is used to record the Bus Number of the PCI bus segment to which the secondary interface of the bridge is connected.

2.4.11 SBBN— Subordinate Bus Number Register

Table 13. 1Ah: SBBN— Subordinate Bus Number Register

Size: 8-bit			**Default:** 00h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 1Ah **Offset End:** 1Ah
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	00h	RW	SBBN	**Subordinate Bus Number (SBBN):** This register is used to record the Bus Number of the highest numbered PCI bus segment, which is downstream of (or subordinate to) the bridge.

2.4.12 SDLT— Secondary Latency Timer Register

Table 14. 1Bh: SDLT— Secondary Latency Timer Register

Size: 8-bit			**Default:** 00h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 1Bh **Offset End:** 1Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	00h	RO	SDLT	**Secondary Latency Timer (SDLT):** This register adheres to the definition of the Latency Timer in PCI 3.0 but, applies only to the secondary interface of a bridge.

2.4.13 IOBS— I/O Base Register

Table 15. 1Ch: IOBS— I/O Base Register

Size: 8-bit			**Default:** 01h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 1Ch **Offset End:** 1Ch
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :04	0h	RW	IOBS	**I/O Base Register (IOBS):** PCI Express bridges support I/O Space for compatibility with legacy devices that require its use.
03 :00	1h	RO		**I/O Base Support type:** 0 = 16-bit addressing support 1 = 32-bit addressing support

2.4.14 IOLMT— I/O Limit Register

Table 16. 1Dh: IOLMT— I/O Limit Register

Size: 8-bit			**Default:** 01h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 1Dh **Offset End:** 1Dh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :04	0h	RW	IOLMT	**I/O Limit Register (IOLMT):** PCI Express bridges support I/O Space for compatibility with legacy devices that require its use.	
03 :00	1h	RO	IOLMTSUPPORT	**I/O Limit Support type:** 0 = 16-bit addressing support 1 = 32-bit addressing support	

2.4.15 SDSTS— Secondary Status Register

Table 17. 1Eh: SDSTS— Secondary Status Register (Sheet 1 of 2)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 1Eh **Offset End:** 1Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15	0b	RWC	DPE2	**Detected Parity Error**: This bit is set by the Secondary Side for a Type 1 Configuration Space header Function whenever it receives a Poisoned TLP, regardless of the state the Parity Error Response Enable bit in the Bridge Control register.	
14	0b	RWC	SSE2	**Received System Error:** This bit is set when the Secondary Side for a Type 1 Configuration Space header Function receives an ERR_FATAL or ERR_NONFATAL Message.	
13	0b	RWC	RMA2	**Received Master Abort:** Primary received Unsupported Request Completion Status. 0 = Not assert 1 = Assert	
12	0b	RWC	RTA2	**Received Target Abort:** Primary received Abort Completion Status 0 = Not assert 1 = Assert	
11	0b	RWC	STA2	**Signaled Target Abort:** Primary transmitted Abort Completion Status 0 = Not assert 1 = Assert	
10 :09	00b	RO	DEVSEL_TIME	**DEVSEL Timing:** This bit field encodes the timing of the secondary interface DEVSEL# as listed below. The encoding must indicate the slowest response time that the bridge uses to assert DEVSEL# on its secondary interface when it is responding as a target in conventional PCI mode to any transaction except a Configuration Read or Configuration Write. 00 = Fast DEVSEL# decoding 01 = Medium DEVSEL# decoding 10 = Slow DEVSEL# decoding 11 = Reserved	

Table 17. 1Eh: SDSTS— Secondary Status Register (Sheet 2 of 2)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 1Eh **Offset End:** 1Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
08	0b	RWC	MDPE2	**Master Data Parity Error:** This bit is used to report the detection of an uncorrectable data error by the bridge. 0 = No uncorrectable data error detected on the secondary interface. 1 = Uncorrectable data error detected on the secondary interface.	
07	0b	RO	BACK_TO_BACK_CAPABLE	**Fast Back-to-Back Transactions Capable:** This bit indicates whether or not the secondary interface of the bridge is capable of decoding fast back-to-back transactions when the transactions are from the same master but to different targets. 0 = The secondary interface is not capable of decoding fast back-to-back transactions to different targets. 1 = The secondary interface is capable of decoding fast back-to-back transaction to different targets.	
06	0b	RO		Reserved	
05	0b	RO	CAP66	**66 MHz Capable:** This bit indicates whether or not the secondary interface of the bridge is capable of operating at 66 MHz in conventional PCI mode. 0 = The secondary interface is not capable of 66 MHz operation. 1 = The secondary interface is capable of 66 MHz operation.	
04 :00	0h	RO		Reserved	

Note: Secondary Status Register shows the Secondary Bus status.

2.4.16 MBS— Memory Base Register

Table 18. 20h: MBS— Memory Base Register

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 20h **Offset End:** 21h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :04	000h	RW	MBS	**Memory Base Register (MBS):** These registers are required registers that define a (non-prefetchable) memory mapped I/O address range, which is used by the bridge to determine when to forward memory transactions from one interface to the other.	
03 :00	0h	RO		Reserved	

2.4.17 MLMT— Memory Limit Register

Table 19. 22h: MLMT— Memory Limit Register

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 22h **Offset End:** 23h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :04	000h	RW	MLMT	**Memory Limit Register (MLMT):** These registers are required registers that define a (non-prefetchable) memory mapped I/O address range, which is used by the bridge to determine when to forward memory transactions from one interface to the other.	
03 :00	0h	RO		Reserved	

2.4.18 PMBS— Prefetchable Memory Base Register

Table 20. 24h: PMBS— Prefetchable Memory Base Register

Size: 16-bit			**Default:** 0001h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 24h **Offset End:** 25h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :04	000h	RW	PMBS	**Prefetchable Memory Base Register (PMBS):** The Intel® PCH EG20T does not support Prefetchable Memory Device.	
03 :00	1h	RO		**Prefetchable Memory Base Support Addressing Mode** 0 = 32-bit 1 = 64-bit	

2.4.19 PMLMT— Prefetchable Memory Limit Register

Table 21. 26h: PMLMT— Prefetchable Memory Limit Register

Size: 16-bit			**Default:** 0001h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 26h **Offset End:** 27h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :04	000h	RW	PMLMT	**Prefetchable Memory Limit Register (MLMT):** The Intel® PCH EG20T does not support Prefetchable Memory Device.	
03 :00	1h	RO	PREFETCHADD SUPPORT	**Prefetchable Memory Limit Support Addressing Mode** 0 = 32bit 1 = 64bit	

2.4.20 PMUBS— Prefetchable Memory Base Upper 32-bit Register

Table 22. 28h: PMUBS— Prefetchable Memory Base Upper 32-bit Register

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 28h **Offset End:** 2Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RW	PMUBS	**Prefetchable Memory Base Upper 32-bit Register (PMUBS):** The Intel® PCH EG20T does not support Prefetchable Memory Device.

2.4.21 PMULMT— Prefetchable Memory Limit Upper 32-bit Register

Table 23. 2Ch: PMULMT— Prefetchable Memory Limit Upper 32-bit Register

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 2Ch **Offset End:** 2Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RW	PMULMT	**Prefetchable Memory Limit Upper 32-bit Register (PMULMT):** The Intel® PCH EG20T does not support Prefetchable Memory Device.

2.4.22 IOUBS— I/O Base Upper 16-bit Register

Table 24. 30h: IOUBS— I/O Base Upper 16-bit Register

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 30h **Offset End:** 31h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :00	0000h	RW	IOUBS	**I/O Base Upper 16-bit Register (IOUBS):** These registers are optional extensions to the I/O Base and I/O Limit registers.

2.4.23 IOULMT— I/O Limit Upper 16-bit Register

Table 25. 32h: IOULMT— I/O Limit Upper 16-bit Register

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 32h **Offset End:** 33h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :00	0000h	RW	IOULMT	**P I/O Limit Upper 16-bit Register (IOUBS):** These registers are optional extensions to the I/O Base and I/O Limit registers.

2.4.24 CAP_PTR— Capabilities Pointer Register

Table 26. 34h: CAP_PTR— Capabilities Pointer Register

Size: 8-bit			**Default:** 40h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 34h **Offset End:** 34h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	40h	RO	PTR	**Pointer (PTR):** This register points to the starting offset of the PCIe-Bridge capabilities ranges.	

2.4.25 INT_LN— Interrupt Line Register

Table 27. 3Ch: INT_LN— Interrupt Line Register

Size: 8-bit			**Default:** FFh		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 3Ch **Offset End:** 3Ch
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	FFh	RW	INT_LN	**Interrupt Line (INT_LN):** This data is not used by the Intel® PCH EG20T PCIe* bridge. This is a software-written value that indicates which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.	

2.4.26 INT_PN— Interrupt Pin Register

Table 28. 3Dh: INT_PN— Interrupt Pin Register

Size: 8-bit			**Default:** 01h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 3Dh **Offset End:** 3Dh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	01h	RO	INT_PN	**Interrupt Pin:** INTA	

2.4.27 BRG_CTL— Bridge Control Register

Table 29. 3Eh: BRG_CTL— Bridge Control Register (Sheet 1 of 2)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 3Eh **Offset End:** 3Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :12	0h	RO		Reserved	
11	0b	RO	DTSERR	**Discard Timer** SERR Enable Status Not applicable to PCI Express, hardwired to 0.	
10	0b	RO	DTS	**Discard Timer Status** Not applicable to PCI Express, hardwired to 0.	

Table 29. 3Eh: BRG_CTL— Bridge Control Register (Sheet 2 of 2)

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 3Eh **Offset End:** 3Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
09	0b	RO	SDT	**Secondary Discard Timer** Not applicable to PCI Express, hardwired to 0.
08	0b	RO	PDT	**Primary Discard Timer** Not applicable to PCI Express, hardwired to 0.
07	0b	RO	TRANSEN	**Fast Back-to-Back Transactions Enable** Not applicable to PCI Express, hardwired to 0.
06	0b	RW	SBRST	Secondary Bus Reset
05	0b	RO	MASTERABT	**Master Abort Mode** Not applicable to PCI Express, hardwired to 0.
04 :02	000b	RO		Reserved
01	0b	RW	SERREN	SERR Enable
00	0b	RW	PERREN	Parity Error Response Enable

Note: When writing in a register, write "0" in the Read Only bits.

2.4.28 PM_CAPID—PCI Power Management Capability ID Register

Table 30. 40h: PM_CAPID—PCI Power Management Capability ID Register

Size: 8-bit			**Default:** 01h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 40h **Offset End:** 40h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	01h	RO	PMC_ID	**Power Management Capability ID:** A value of 01h indicates that this is a PCI Power Management capabilities field.

2.4.29 NXT_PTR1—Next Item Pointer #1 Register

Table 31. 41h: NXT_PTR1—Next Item Pointer #1 Register

Size: 8-bit			**Default:** 70h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 41h **Offset End:** 41h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	70h	RO	NEXT_PV	**Next Item Pointer 1 Value:** Hardwired to 70h to indicate the power management registers capabilities list.

2.4.30 PM_CAP—Power Management Capabilities Register

Table 32. 42h: PM_CAP—Power Management Capabilities Register

Size: 16-bit			**Default:** DA02h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 42h **Offset End:** 43h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :11	11011b	R0	PME_SUP	**PME Support (PME_SUP):** This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the PCIe-Bridge is not capable of generating PME#. Software should never need to modify this field. PME notification is supported in the respective PME state (D0, D1, D3hot, D3cold).	
10	0b	RO	D2_SUP	D2 Support (D2_SUP). D2 State is not supported	
09	1b	RO	D1_SUP	D1 Support (D1_SUP). D1 State is supported	
08 :06	000b	R0	AUX_CUR	**Auxiliary Current (AUX_CUR):** This function does not support the D3cold state.	
05	0b	RO	DSI	**Device Specific Initialization (DSI):** The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.	
04	0b	RO		Reserved	
03	0b	RO	PME_CLK	**PME Clock (PME_CLK):** The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.	
02 :00	010b	RO	VER	**Version (VER):** The Intel® PCH EG20T reports 010b, indicating that it complies with the PCI Power Management Specification Revision 1.1	

2.4.31 PWR_CNTL_STS—Power Management Control/Status Register

Table 33. 44h: PWR_CNTL_STS—Power Management Control/Status Register (Sheet 1 of 2)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 44h **Offset End:** 45h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15	0b	RWC	STS	PME Status (STS): Indicates if a previously enabled PME event occurred or not.	
14 :13	00b	RO	DSCA	**Data Scale (DSCA):** Hardwired to 00b indicating it does not support the associated Data register.	
12 :09	0h	RO	DSEL	**Data Select (DSEL):** Hardwired to 0000b indicating it does not support the associated Data register.	
08	0b	RW	ENB	PME Enable: A value of 1 indicates that the device is enabled to generate PME.	
07 :02	000000b	RO		Reserved	

Table 33. 44h: PWR_CNTL_STS—Power Management Control/Status Register (Sheet 2 of 2)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 44h **Offset End:** 45h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
01 :00	00b	RW	POWERSTATE	**Power State**: This 2-bit field is used both to determine the current power state of PCIe-Bridge function and to set a new power state. The definition of the field values are: 00 = D0 state 01 = D1 state 11 = D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3hot state, the Intel® PCH EG20T must not accept accesses to the PCIe-Bridge memory range; but the configuration space must still be accessible. When software changes this value from the D3hot state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the Function.	

2.4.32 PCIe_CAPID—PCIe Capability ID Register

Table 34. 70h: PCIe_CAPID—PCIe Capability ID Register

Size: 8-bit			**Default:** 10h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 70h **Offset End:** 70h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	10h	RO	PMC_ID	**PCI express Capability ID**: A value of 10h indicates that the ID identifies the PCI express Capability register set.	

2.4.33 PCIe_NPR—PCIe Next Item Pointer Register

Table 35. 71h: PCIe_NPR—PCIe Next Item Pointer Register

Size: 8-bit			**Default:** 00h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 71h **Offset End:** 71h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	00h	RO	NEXT_P1V	**Next Item Pointer Value:** Hardwired to 00h to indicate that PCI express Capability is the last item in the capabilities list.	

2.4.34 PCIe_CP—PCIe Capabilities Register

Table 36. 72h: PCIe_CP—PCIe Capabilities Register

Size: 16-bit			**Default:** 0072h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 72h **Offset End:** 73h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :14	00b	RO	Reserved	Reserved	
13 :09	00h	RO	INT_MSG_NUM	**Interrupt Message Number**: This field indicates the MSI/MSI-X vector that is used for the interrupt message generated in association with any of the status bits of this Capability structure.	
08	0b	RO	SLOT	**Slot Implemented:** When set, this bit indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled). This field is valid for the following PCI Express Device/Port Types: • Root Port of PCI Express Root Complex • Downstream Port of PCI Express Switch	
07 :04	0111b	RO	DEV_PORT	Device Port Type: Indicates the specific type of this PCI Express Function. Note that different functions in a multi-function device can generally be of different types. Defined encodings are: 0000b PCI Express Endpoint 0001b Legacy PCI Express Endpoint 0100b Root Port of PCI Express Root Complex† 0101b Upstream Port of PCI Express Switch† 0110b Downstream Port of PCI Express Switch† 0111b PCI Express to PCI/PCI-X Bridge† 1000b PCI/PCI-X to PCI Express Bridge† 1001b Root Complex Integrated Endpoint 1010b Root Complex Event Collector †This value is only valid for Functions that are implemented	
03 :00	0010b	RO	CAP_VER	Capability Version: Indicates the version number of the PCI-SIG defined PCI Express Capability structure.	

2.4.35 PCIe_DCP—PCIe Device Capabilities Register

Table 37. 74h: PCIe_CP—PCIe Capabilities Register (Sheet 1 of 4)

Size: 32-bit			**Default:** 00008020h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 74h **Offset End:** 77h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :29	000b	RO		Reserved	
28	0b	RO	FUNCTIONRST	**Function Level Reset Capability:** A value of 1b indicates the Function supports the optional Function Level Reset mechanism. This field applies to Endpoints only. For all other Function types this bit must be hardwired to 0b	

Table 37. 74h: PCIe_CP—PCIe Capabilities Register (Sheet 2 of 4)

Size: 32-bit		**Default:** 00008020h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 74h **Offset End:** 77h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
27 :26	00b	RO	SLOTPOWER-SCALE	**Captured Slot Power Limit:** Scale (Upstream Ports only): Specifies the scale used for the Slot Power Limit Value. Range of Values: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x This value is set by the Set_Slot_Power_Limit Message or hardwired to 00b (see Section 6.9). The default value is 00b.
25 :18	00h	RO	SLOTPOWER-VALUE	**Captured Slot Power Limit Value (Up-stream Ports only):** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit Message or hardwired to 00h. The default value is 00h.
17 :16	00b	RO		Reserved
15	1b	RO	ROLE_ERR	**Role-Based Error Reporting**: When set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1., or subsequent PCI Express Base Specification revisions.
14 :12	000b	RO		The value read from this bit is undefined.
11 :09	000b	RO	L1LATENCY	**Endpoint L1 Acceptable Latency –** This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L1 Acceptable Latency number to compare against the L1 Exit Latencies reported (see below) by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L1 entry can be used with no loss of performance. Defined encodings are: 000b Maximum of 1 µs 001b Maximum of 2 µs 010b Maximum of 4 µs 011b Maximum of 8 µs 100b Maximum of 16 µs 101b Maximum of 32 µs 110b Maximum of 64 µs 111b No limit For Functions other than Endpoints, this field is Reserved and must be hardwired to 000b.

Table 37. 74h: PCIe_CP—PCIe Capabilities Register (Sheet 3 of 4)

Size: 32-bit		**Default:** 00008020h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 74h **Offset End:** 77h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
08 :06	000b	RO	L0LATENCY	**Endpoint L0s Acceptable Latency:** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L0s entry can be used with no loss of performance. Defined encodings are: 000b Maximum of 64 ns 001b Maximum of 128 ns 010b Maximum of 256 ns 011b Maximum of 512 ns 100b Maximum of 1 µs 101b Maximum of 2 µs 110b Maximum of 4 µs 111b No limit **For Functions other than Endpoints, this field is Reserved and must be hardwired to 000b**.
05	1b	RO	EXT_TAG	**Extended Tag Field Supported:** This bit indicates the maximum supported size of the Tag field as a Requester. Defined encodings are: 0b 5-bit Tag field supported 1b 8-bit Tag field supported ***Note:*** 8-bit Tag field generation must be enabled by the Extended Tag Field Enable bit in the Device Control register
04 :03	00b	RO	PFS	**Phantom Functions Supported:** This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions allowed by logically combining unclaimed Function Numbers (called Phantom Functions) with the Tag identifier. This field indicates the number of most significant bits of the Function Number portion of Requester ID that are logically combined with the Tag identifier. Defined encodings are: **00b** No Function Number bits are used for Phantom Functions. Multi-Function devices are permitted to implement up to 8 independent Functions. **01b** The most significant bit of the Function number in Requester ID is used for Phantom Functions; a multi-Function device is permitted to implement Functions 0-3. Functions 0, 1, 2, and 3 are permitted to use Function Numbers 4, 5, 6, and 7 respectively as Phantom Functions. **10b** The two most significant bits of Function Number in Requester ID are used for Phantom Functions; a multi-Function device is permitted to implement Functions 0-1. Function 0 is permitted to use Function Numbers 2, 4, and 6 for Phantom Functions. Function 1 is permitted to use Function Numbers 3, 5, and 7 as Phantom Functions. **11b** All 3 bits of Function Number in Requester ID used for Phantom Functions. The device must have a single Function 0 that is permitted to use all other Function Numbers as Phantom Functions. ***Note:*** Phantom Function support for the Function must be enabled by the Phantom Functions Enable field in the Device Control register before the Function is permitted to use the Function Number

Table 37. 74h: PCIe_CP—PCIe Capabilities Register (Sheet 4 of 4)

Size: 32-bit		**Default:** 00008020h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 74h **Offset End:** 77h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
02 :00	000b	RO	PAYLOADSIZE	**Max_Payload_Size Supported:** This field indicates the maximum payload size that the Function can support for TLPs. Defined encodings are: 000b 128 bytes max payload size 001b 256 bytes max payload size 010b 512 bytes max payload size 011b 1024 bytes max payload size 100b 2048 bytes max payload size 101b 4096 bytes max payload size 110b Reserved 111b Reserved The functions of a multi-function device are permitted to report different values for this field.

2.4.36 PCIe_DCT—PCIe Device Control Register

Table 38. 78h: PCIe_DCT—PCIe Drive Control Register (Sheet 1 of 3)

Size: 16-bit		**Default:** 2010h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 78h **Offset End:** 79h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15	0b	RW	CONFIG_RTY_EN	**Bridge Configuration Retry Enable:** When set, this bit enables PCI Express to PCI/PCI-X bridges to return Configuration Request Retry Status (CRS) in response to Configuration Requests that target devices below the bridge. Refer to the *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0* for further details. Default value of this bit is 0b.
14 :12	010b	RW	MRRS	**Max_Read_Request_Size:** This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. Defined encodings for this field are: 000b 128 bytes maximum Read Request size 001b 256 bytes maximum Read Request size 010b 512 bytes maximum Read Request size 011b 1024 bytes maximum Read Request size 100b 2048 bytes maximum Read Request size 101b 4096 bytes maximum Read Request size 110b Reserved 111b Reserved Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b. Default value of this field is 010b.

Table 38. 78h: PCIe_DCT—PCIe Drive Control Register (Sheet 2 of 3)

Size: 16-bit		**Default:** 2010h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 78h **Offset End:** 79h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
11	0b	RO	SNOOP	**Enable No Snoop:** If this bit is set, the Function is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Note that setting this bit to 1b should not cause a Function to set the No Snoop attribute on all transactions that it initiates. Even when this bit is set, a Function is only permitted to set the No Snoop attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system. This bit is permitted to be hardwired to 0b if a Function would never set the No Snoop attribute in transactions it initiates. Default value of this bit is 0b.
10	0b	RWS (Sticky Read-Write)	PM_ENB	**Auxiliary (AUX) Power PM Enable:** Setting this bit enables a Function to draw AUX power independent of PME AUX power. Functions that require AUX power on legacy operating systems should continue to indicate PME AUX power requirements. AUX power is allocated as requested in the AUX_Current field of the Power Management Capabilities register (PMC), independent of the PME_En bit in the Power Management Control/Status register. For multi-Function devices, a component is allowed to draw AUX power if at least one of the Functions has this bit set. ***Note:*** Functions that consume AUX power must preserve the value of this sticky register when AUX power is available. In such Functions, this register value is not modified by Conventional Reset. Functions that do not implement this capability hardwire this bit to 0b.
09	0b	RW	PHANTOM_EN	**Phantom Functions Enable**: When set, this bit enables a Function to use unclaimed Functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is Clear, the Function is not allowed to use Phantom Functions. Functions that do not implement this capability hardwire this bit to 0b. Default value of this bit is 0b.
08	0b	RW	EXT_TAG_FIELD	**Extended Tag Field Enable:** When set, this bit enables a Function to use an 8-bit Tag field as a Requester. If the bit is Clear, the Function is restricted to a 5-bit Tag field. Functions that do not implement this capability hardwire this bit to 0b. Default value of this bit is 0b.
07 :05	000b	RW	PAYLOD_SIZE	**Max_Payload_Size:** This field sets maximum TLP payload size for the Function. As a Receiver, the Function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Defined encodings for this field are: 000b 128 bytes max payload size 001b 256 bytes max payload size 010b 512 bytes max payload size 011b 1024 bytes max payload size 100b 2048 bytes max payload size 101b 4096 bytes max payload size 110b Reserved 111b Reserved Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b. System software is not required to program the same value for this field for all the Functions of a multi-Function device. Default value of this field is 000b.

Table 38. 78h: PCIe_DCT—PCIe Drive Control Register (Sheet 3 of 3)

Size: 16-bit		**Default:** 2010h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 78h **Offset End:** 79h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
04	1b	RW	ERO	**Enable Relaxed Ordering:** If this bit is set, the Function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. Default value of this bit is 1b.
03	0b	RW	URREN	**Unsupported Request Reporting Enable:** This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending Error Messages. For a multi-Function device, this bit controls error reporting for each Function. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.
02	0b	RW	FEREN	**Fatal Error Reporting Enable:** This bit in conjunction with other bits, controls sending ERR_FATAL Messages. For a multi-Function device, this bit controls error reporting for each Function from the point-of-view of the respective Function. For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL Message is generated. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.
01	0b	RW	NFEREN	**Non-Fatal Error Reporting Enable:** This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages. For a multi-Function device, this bit controls error reporting for each Function from point-of-view of the respective Function. For a Root Port, the reporting of Non-fatal errors is internal to the root. No external ERR_NONFATAL Message is generated. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.
00	0b	RW	CEREN	**Correctable Error Reporting Enable:** This bit, in conjunction with other bits, controls sending ERR_COR Messages. For a multi-Function device, this bit controls error reporting for each Function from the point-of-view of the respective Function. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR Message is generated. A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b. Default value of this bit is 0b.

2.4.37 PCIe_DST—PCIe Device Status Register

Table 39. 7Ah: PCIe_DST—PCIe Device Status Register (Sheet 1 of 2)

Size: 16-bit		**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 7Ah **Offset End:** 7Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :06	000h	RO		Reserved

Table 39. 7Ah: PCIe_DST—PCIe Device Status Register (Sheet 2 of 2)

Size: 16-bit			Default: 0000h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 7Ah Offset End: 7Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
05	0b	RO	TRANSPENDING	**Transactions Pending:** When set, this bit indicates that a Port has issued Non-Posted Requests on its own behalf (using the Requester ID of the Port), which have not been completed. The Port reports this bit cleared only when all such outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. Note that Root and Switch Ports implementing only the functionality required by this document do not issue Non-Posted Requests on their own behalf, and therefore are not subject to this case. Root and Switch Ports that do not issue Non-Posted Requests on their own behalf hardwire this bit to 0b.	
04	0b	RO	APD	**AUX Power Detected:** Functions that require AUX power report this bit as set if AUX power is detected by the Function.	
03	0b	RWC	URD	**Unsupported Request Detected:** This bit indicates that the Function received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. Default value of this bit is 0b.	
02	0b	RWC	FED	**Fatal Error Detected:** This bit indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register. Default value of this bit is 0b.	
01	0b	RWC	NFED	**Non-Fatal Error Detected:** This bit indicates status of Nonfatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Uncorrectable Error Mask register. Default value of this bit is 0b.	
00	0b	RWC	CRD	**Correctable Error Detected:** This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. For a multi-Function device, each Function indicates status of errors as perceived by the respective Function. For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the Correctable Error Mask register. Default value of this bit is 0b.	

2.4.38 PCIe_LCP—PCIe Link Capabilities Register

Table 40. 7Ch: PCIe_LCP—PCIe Link Capabilities Register (Sheet 1 of 3)

Size: 32-bit			Default: 00033C11h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 7Ch Offset End: 7Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :24	00h	RO	PN	**Port Number:** This field indicates the PCI Express Port number for the given PCI Express Link.	
23 :22	00b	RO		Reserved	

Table 40. 7Ch: PCIe_LCP—PCIe Link Capabilities Register (Sheet 2 of 3)

Size: 32-bit		**Default:** 00033C11h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 7Ch **Offset End:** 7Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
21	0b	RO	LBNC	**Link Bandwidth Notification Capability:** This field is not applicable and is reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b.
20	0b	RO	DLL_ACT	**Data Link Layer Link Active Reporting Capable:** For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
19	0b	RO	DOWNERR_CAP	**Surprise Down Error Reporting Capable:** For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
18	0b	RO	CPM	**Clock Power Management:** For Upstream Ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these Link states. This Capability is applicable only in form factors that support "clock request" (CLKREQ#) capability.
17 :15	110b	RO	L1_LATENCY	**L1 Exit Latency:** This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L1 to L0. Defined encodings are: 000b Less than 1µs 001b 1 µs to less than 2 µs 010b 2 µs to less than 4 µs 011b 4 µs to less than 8 µs 100b 8 µs to less than 16 µs 101b 16 µs to less than 32 µs 110b 32 µs-64 µs 111b More than 64 µs ***Note:*** Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock.
14 :12	011b	RO	L0_LATENCY	**L0s Exit Latency:** This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. Defined encodings are: 000b Less than 64 µs 001b 64 µs to less than 128 µs 010b 128 µs to less than 256 µs 011b 256 µs to less than 512 µs 100b 512 µs to less than 1 µs 101b 1 µs to less than 2 µs 110b 2 µs-4 µs 111b More than 4 µs ***Note:*** Exit latencies may be influenced by PCI Express reference clock configuration depending upon whether a component uses a common or separate reference clock.

Table 40. 7Ch: PCIe_LCP—PCIe Link Capabilities Register (Sheet 3 of 3)

Size: 32-bit			Default: 00033C11h	Power Well: Core
Access	PCI Configuration		B:D:F D0:F0	Offset Start: 7Ch Offset End: 7Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
11 :10	11b	RO	ASPM	**Active State Power Management (ASPM) Support:** This field indicates the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b Reserved 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported Multi-Function devices must report the same value in this field for all Functions.
09 :04	01h	RO	MLW	**Maximum Link Width:** This field indicates the maximum Link width (xN – corresponding to N Lanes) implemented by the component. This value is permitted to exceed the number of Lanes routed to the slot (Downstream Port), adapter connector (Upstream Port), or in the case of component-to-component connections, the actual wired connection width. Defined encodings are: 000000b Reserved 000001b x1 000010b x2 000100b x4 001000b x8 001100b x12 010000b x16 100000b x32 Multi-Function devices must report the same value in this field for all Functions.
03 :00	1h	RO	LINKSPEED	**Supported Link Speeds:** This field indicates the supported Link speed(s) of the associated Port. Defined encodings are: 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5 GT/s Link speeds supported All other encodings are reserved. Multi-Function devices must report the same value in this field for all Functions.

2.4.39 PCIe_LCT—PCIe Link Control Register

Table 41. 81h: PCIe_LCT—PCIe Link Control Register (Sheet 1 of 3)

Size: 16-bit			Default: 0000h	Power Well: Core
Access	PCI Configuration		B:D:F D0:F0	Offset Start: 80h Offset End: 81h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :12	0h	RO	PN	**Reserved.**
11	0b	RO	LABIE	**Link Autonomous Bandwidth Interrupt Enable** – When set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches.

Table 41. 81h: PCIe_LCT—PCIe Link Control Register (Sheet 2 of 3)

Size: 16-bit		**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 80h **Offset End:** 81h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
10	0b	RO	LBMIE	**Link Bandwidth Management Interrupt Enable:** When set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches.
09	0b	RO	HDWDIS	**Hardware Autonomous Width Disable:** When set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Not Supported, Hardwired to 0
08	0b	RW	ENBPM	**Enable Clock Power Management:** Applicable only for Upstream Ports and with form factors that support a "Clock Request" (CLKREQ#) mechanism, this bit operates as follows: **0b** Clock power management is disabled and device must hold CLKREQ# signal low. **1b** When this bit is set, the device is permitted to useCLKREQ# signal to power manage Link clock according to protocol defined in appropriate form factor specification.
07	0b	RW	EXTS	**Extended Synch:** When set, this bit forces the transmission of additional Ordered Sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (for example, logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. Default value for this bit is 0b.
06	0b	RW	CCCNF	**Common Clock Configuration:** When set, this bit indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. A value of 0b indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies. After changing the value in this bit in both components on a Link, software must trigger the Link to retrain by writing a 1b to the Retrain Link bit of the Downstream Port. Default value of this bit is 0b.
05	0b	RW	LRET	**Retrain Link:** A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. If the LTSSM is already in Recovery or Configuration, re-entering Recovery is permitted but not required. Reads of this bit always return 0b. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that is already in progress. This bit is not applicable and is reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. This bit always returns 0b when read.
04	0b	RW	LDIS	**Link Disable:** This bit disables the Link by directing the LTSSM to the Disabled state, when set; this bit is reserved on Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. Default value of this bit is 0b.

Table 41. 81h: PCIe_LCT—PCIe Link Control Register (Sheet 3 of 3)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 80h **Offset End:** 81h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
03	0b	RO	RCB	Read Completion Boundary (RCB): Not applicable – must hardwire the bit to 0b	
02	0b	RO		Reserved	
01 :00	00b	RW	ASPMC	**Active State Power Management (ASPM) Control:** This field controls the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b Disabled 01b L0s Entry Enabled 10b L1 Entry Enabled 11b L0s and L1 Entry Enabled	

2.4.40 PCIe_LST—PCIe Link Status Register

Table 42. 82h: PCIe_LST—PCIe Link Status Register (Sheet 1 of 2)

Size: 16-bit			**Default:** 1011h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 82h **Offset End:** 83h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15	0b	RWC	LABS	**Link Autonomous Bandwidth Status:** This bit is set by hardware to indicate that the hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches.	
14	0b	RWC	LBMS	**Link Bandwidth Management Status** – This bit is set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches.	
13	0b	RO	DL_ACTIVE	**Data Link Layer Link Active:** This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the corresponding Data Link Layer Link Active Reporting capability bit is implemented. Otherwise, this bit must be hardwired to 0b.	
12	1b	RO	SLOTCLK_CONFIG	**Slot Clock Configuration:** This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared.	
11	0b	RO	LT	**Link Training:** This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but, Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state. This bit is not applicable and reserved for Endpoints, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches,	

Table 42. 82h: PCIe_LST—PCIe Link Status Register (Sheet 2 of 2)

Size: 16-bit			**Default:** 1011h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 82h **Offset End:** 83h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
10	0b	RO	UNDEF	**Undefined:** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.
09 :04	01h	RO	NLW	**Negotiated Link Width:** This field indicates the negotiated width of the given PCI Express Link. Defined encodings are: 00 0001b x1 00 0010b x2 00 0100b x4 00 1000b x8 00 1100b x12 01 0000b x16 10 0000b x32
03 :00	1h	RO	CLS	**Current Link Speed:** This field indicates the negotiated Link speed of the given PCI Express Link. Defined encodings are: 0001b 2.5 GT/s PCI Express Link 0010b 5.0 GT/s PCI Express Link

2.4.41 PCIe_DCP2—PCIe Device Capabilities 2 Register

Table 43. 94h: PCIe_LST—PCIe Link Status Register (Sheet 1 of 2)

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 94h **Offset End:** 97h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :05	000000 0h	RO		Reserved
04	0b	RO	CTDS	**Completion Timeout Disable Supported** – A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports.

Table 43. 94h: PCIe_LST—PCIe Link Status Register (Sheet 2 of 2)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 94h **Offset End:** 97h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
03 :00	0h	RO	CTRS	**Completion Timeout Ranges Supported:** This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50 µs to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s Bits are set according to the information given below to show timeout value ranges supported. 0000b Completion Timeout programming not supported – the Function must implement a timeout value in the range 50 s to 50 ms. 0001b Range A 0010b Range B 0011b Ranges A and B 0110b Ranges B and C 0111b Ranges A, B, and C 1110b Ranges B, C and D 1111b Ranges A, B, C, and D All other values are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms.

2.4.42 PCIe_DCT2—PCIe Device Control 2 Register

Table 44. 98h: PCIe_DCT2—PCIe Device Control 2 Register (Sheet 1 of 2)

Size: 16-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 98h **Offset End:** 99h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :05	0000000h	RO		Reserved
04	0b	RO	CTDS	**Completion Timeout Disable Supported** – A value of 1b indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue Requests on their own behalf and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. This mechanism is optional for Root Ports.

Table 44. 98h: PCIe_DCT2—PCIe Device Control 2 Register (Sheet 2 of 2)

Size: 16-bit			**Default:** 00000000h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 98h **Offset End:** 99h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
03 :00	0h	RO	CTRS	**Completion Timeout Ranges Supported:** This field indicates device Function support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue Requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of Requests issued on PCI Express. For all other Functions this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50 s to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4 s Range D: 4 s to 64 s Bits are set according to the information given below to show timeout value ranges supported. 0000b Completion Timeout programming not supported – the Function must implement a timeout value in the range 50 s to 50 ms. 0001b Range A 0010b Range B 0011b Ranges A and B 0110b Ranges B and C 0111b Ranges A, B, and C 1110b Ranges B, C and D 1111b Ranges A, B, C, and D All other values are reserved. It is strongly recommended that the Completion Timeout mechanism not expire in less than 10 ms.	

2.4.43 PCIe_LCT2—PCIe Link Control 2 Register

Table 45. A0h: PCIe_LCT2—PCIe Link Control 2 Register (Sheet 1 of 3)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** A0h **Offset End:** A1h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :13	000b	RO		Reserved	
12	0b	RW	CDEMP	**Compliance De-emphasis:** This bit sets the de-emphasis level in Polling. Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this bit to 0b.	

Table 45. A0h: PCIe_LCT2—PCIe Link Control 2 Register (Sheet 2 of 3)

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** A0h **Offset End:** A1h

Bit Range	Default	Access	Acronym	Description
11	0b	RW	CSOS	**Compliance SOS:** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0b.
10	0b	RW	EMC	**Enter Modified Compliance:** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling. Compliance substate. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b.
09 :07	000b	RW	TM	**Transmit Margin:** This field controls the value of the nonde-emphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling. Configuration substate. Encodings: **000b** Normal operating range **001b** 800-1200 mV for full swing and 400-700 mV for half-swing **010b - (n-1)** Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing **n - 111b** reserved Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b.

Table 45. A0h: PCIe_LCT2—PCIe Link Control 2 Register (Sheet 3 of 3)

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** A0h **Offset End:** A1h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
06	0b	RO	SDEMC	**Selectable De-emphasis:** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
05	0b	RO	HASD	**Hardware Autonomous Speed Disable:** When set, this bit disables hardware from changing the Link speed for device specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. Initial transition to the highest supported common link speed is not blocked by this bit. Functions that do not implement the associated mechanism are permitted to hardwire this bit to 0b.
04	0b	RW	EC	**Enter Compliance:** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 0b.
03 :00	0h	RW	TLS	**Target Link Speed:** For Downstream Ports, this field sets an upper limit on Link operational speed by restricting the values advertised by the Upstream component in its training sequences. Defined encodings are: 0001b 2.5 GT/s Target Link Speed 0010b 5.0 GT/s Target Link Speed All other encodings are reserved. Components that support only the 2.5 GT/s speed are permitted to hardwire this field to 0000b.

2.4.44 PCIe_LST2—PCIe Link Status 2 Register

Table 46. A2h: PCIe_LST2—PCIe Link Status 2 Register (Sheet 1 of 2)

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** A2h **Offset End:** A3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :01	0000h	RO		Reserved

Table 46. A2h: PCIe_LST2—PCIe Link Status 2 Register (Sheet 2 of 2)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** A2h **Offset End:** A3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
00	0b	RO	CDEMS	**Compliance De-emphasis:** This bit sets the de-emphasis level in Polling. Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this bit to 0b.	

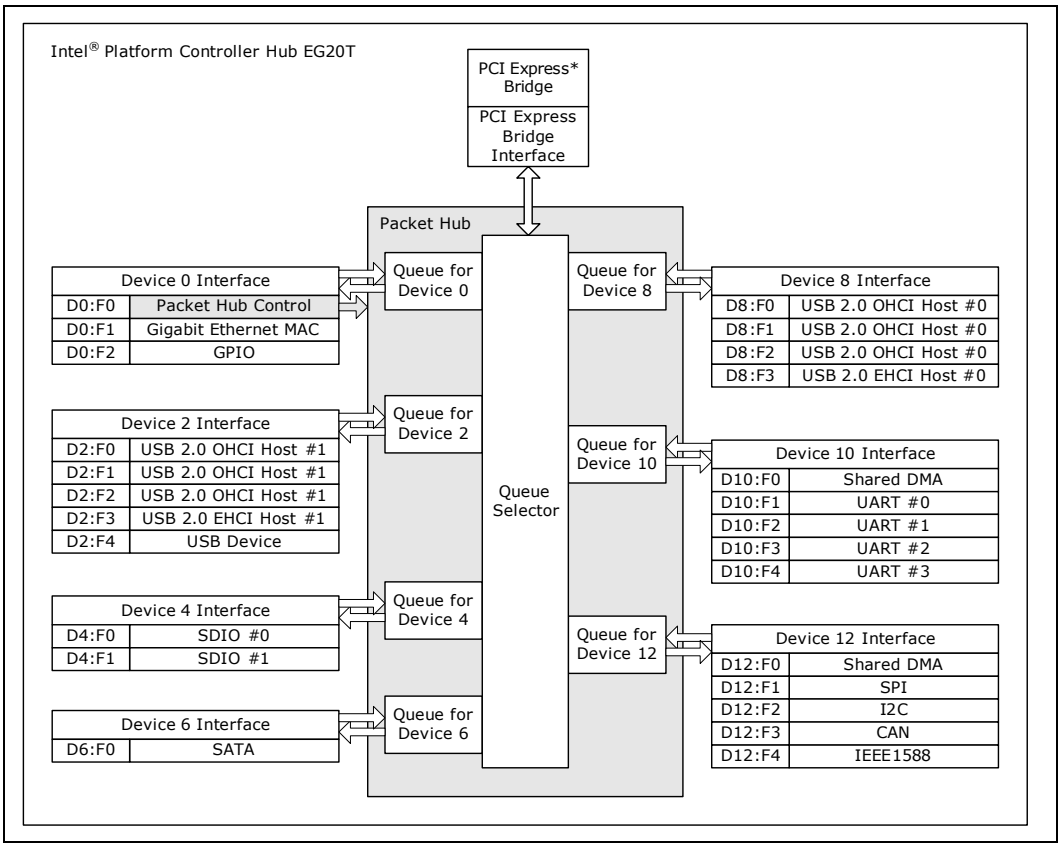
§ §

3.0 Packet Hub

3.1 Overview

PCI functions in the Intel® Platform Controller Hub EG20T are tied to an external PCI Express* link through an internal PCI compatible bus which performs parallel operation. The Packet Hub's connection to the PCI functions is also through the PCI compatible bus.

Figure 3. Packet Hub Configuration



Packet Hub is provided to realize QoS of upstream PCI Express Transaction Layer Packets (TLP) from the Intel® PCH EG20T's PCI functions. It also provides flexibility of issuing interrupts from various internal functions on the PCI Express link with programmable delay intervals to optimize CPU power saving by reducing the frequency of CPU waking up from ACPI C-states.

Packet Hub is functional with default settings. To achieve the benefits of having flexible QoS and interrupt reduction mechanism, system specific programming onto Packet Hub registers is required through software.

3.2 Register Address Map

3.2.1 PCI Configuration Registers

Table 47. PCI Configuration Registers

Offset	Name	Symbol	Access	Initial Value
00h - 01h	Vendor Identification Register	VID	RO	8086h
02h - 03h	Device Identification Register	DID	RO	8801h
04h - 05h	PCI Command Register	PCICMD	RO, RW	0000h
06h - 07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h
09h - 0Bh	Class Code Register	CC	RO	FF0000h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	80h
14h - 17h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch - 2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh - 2Fh	Subsystem ID Register	SSID	RWO	0000h
30h - 33h	Extended ROM Base Address Register	ROM_BASE	RW, RO	00000000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	00h
40h	MSI Capability ID Register	MSI_CAP	RO	05h
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h - 43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h - 47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h - 49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	00h
52h - 53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h - 55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW	0000h

3.2.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

These registers are defined in the MMIO space of Device-0 Function-0.

Queue Control Register and Device Control Register values are mapped by Base address1 (as Memory Space).

Only DWord accesses to these registers are permitted.

3.2.2.1 Queue Control Register

Table 48. Queue Control Registers

Offset	Name	Symbol	Access	Size (bits)	Initial Value
000h	Packet Hub ID Register	PHUB_ID	RO	32	Fixed
004h	Queue Priority Value Register	QP_VAL	RW	32	00000000h
008h	Upstream Queue Max Size Register	UPQ_MXSZ	RW	32	00000000h
00Ch	Downstream Queue Max Size Register	DWQ_MXSZ	RW	32	00000000h

Note:
1. Packet Hub ID Register has a fixed value
2. Only DWord accesses to these registers are permitted.

3.2.2.2 Device Control Registers

Table 49. Device Control Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Size (bits)	Initial value
010h	Completion Response Time Out Register	CR_TO	RW	32	02222222h
014h	Device Control Register	DEV_CTL	RW	32	00000000h
018h	Dead Lock Avoid type selector Register	DLK_AS	RW	32	00000000h
020h	Interrupt Pin register Write Permit Register0 (D0 and D2, and F0 - F7)	INT_WP0	RW	32	00000000h
024h	Interrupt Pin register Write Permit Register 1 (D4 and D6, and F0-F7)	INT_WP1	RW	32	00000000h
028h	Interrupt Pin register Write Permit Register 2 (D8 and D10, and F0 – F7)	INT_WP2	RW	32	00000000h
02Ch	Interrupt Pin register Write Permit Register 3 (D12, and F0 – F7)	INT_WP3	RW	32	00000000h
040h	Interrupt Reduction Value Dev0 Func0	INTRD_D0F0	RW	32	00020000h
044h	Interrupt Reduction Value Dev0 Func1	INTRD_D0F1	RW	32	00020000h
048h	Interrupt Reduction Value Dev0 Func2	INTRD_D0F2	RW	32	00020000h
04Ch - 07Ch	Reserved		RO	32	00000000h
080h	Interrupt Reduction Value Dev2 Func0	INTRD_D2F0	RW	32	00020000h
084h	Interrupt Reduction Value Dev2 Func1	INTRD_D2F1	RW	32	00020000h
088h	Interrupt Reduction Value Dev2 Func2	INTRD_D2F2	RW	32	00020000h
08Ch	Interrupt Reduction Value Dev2 Func3	INTRD_D2F3	RW	32	00020000h
090h	Interrupt Reduction Value Dev2 Func4	INTRD_D2F4	RW	32	00020000h

Table 49. Device Control Registers (Sheet 2 of 2)

094h - 0BCh	Reserved		RO	32	00000000h
0C0h	Interrupt Reduction Value Dev4 Func0	INTRD_D4F0	RW	32	00020000h
0C4h	Interrupt Reduction Value Dev4 Func1	INTRD_D4F1	RW	32	00020000h
0C8h - 0FCh	Reserved		RO	32	00000000h
100h	Interrupt Reduction Value Dev6 Func0	INTRD_D6F0	RW	32	00020000h
104h - 13Ch	Reserved		RO	32	00000000h
140h	Interrupt Reduction Value Dev8 Func0	INTRD_D8F0	RW	32	00020000h
144h	Interrupt Reduction Value Dev8 Func1	INTRD_D8F1	RW	32	00020000h
148h	Interrupt Reduction Value Dev8 Func2	INTRD_D8F2	RW	32	00020000h
14Ch	Interrupt Reduction Value Dev8 Func3	INTRD_D8F3	RW	32	00020000h
150h - 17Ch	Reserved		RO	32	00000000h
180h	Interrupt Reduction Value Dev10 Func0	INTRD_D10F0	RW	32	00020000h
184h	Interrupt Reduction Value Dev10 Func1	INTRD_D10F1	RW	32	00020000h
188h	Interrupt Reduction Value Dev10 Func2	INTRD_D10F2	RW	32	00020000h
18Ch	Interrupt Reduction Value Dev10 Func3	INTRD_D10F3	RW	32	00020000h
190h	Interrupt Reduction Value Dev10 Func4	INTRD_D10F4	RW	32	00020000h
194h - 1BCh	Reserved		RO	32	00000000h
1C0h	Interrupt Reduction Value Dev12 Func0	INTRD_D12F0	RW	32	00020000h
1C4h	Interrupt Reduction Value Dev12 Func1	INTRD_D12F1	RW	32	00020000h
1C8h	Interrupt Reduction Value Dev12 Func2	INTRD_D12F2	RW	32	00020000h
1CCh	Interrupt Reduction Value Dev12 Func3	INTRD_D12F3	RW	32	00020000h
1D0h	Interrupt Reduction Value Dev12 Func4	INTRD_D12F4	RW	32	00020000h
1D4h - 23Ch	Reserved		RO	32	00000000h

Notes:
1. Registers are mounted only when there is a corresponding function.
2. Only DWord accesses to these registers are permitted.

3.3 Registers

3.3.1 PCI Configuration Registers

3.3.1.1 VID— Vendor Identification Register

Table 50. 00h: VID- Vendor Identification Register

Size: 16-bit			**Default:** 8086h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 00h **Offset End:** 01h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :00	8086h	RO	VID	**Vendor ID (VID):** This is a 16-bit value assigned to Intel.

3.3.1.2 DID— Device Identification Register

Table 51. 02h: DID- Device Identification Register

Size: 16-bit			**Default:** 8801h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 02h **Offset End:** 03h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :00	8801h	RO	DID	**Device ID (DID):** This is a 16-bit value assigned to the Packet Hub. Packet Hub (D0:F0): 8801h

3.3.1.3 PCICMD— PCI Command Register

Table 52. 04h: PCICMD- PCI Command Register (Sheet 1 of 2)

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 04h **Offset End:** 05h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 : 11	00h	RO		Reserved[1]
10	0b	RW	ITRPDS	**Interrupt Disable:** 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. PCISTS.IS is not affected by the interrupt enable.
09	0b	RO		Reserved[1]
08	0b	RW	SERR	**SERR# Enable:** Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07 : 03	00000b	RO		Reserved[1]

Table 52. 04h: PCICMD- PCI Command Register (Sheet 2 of 2)

Size: 16-bit			Default: 0000h		Power Well: Core
Access	PCI Configuration		B:D:F D0:F0		Offset Start: 04h Offset End: 05h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
02	0b	RW	BME	**Bus Master Enable (BME):** This bit controls that a device serves as a bus master. 0 = Disable 1 = Enable	
01	0b	RW	MSE	**Memory Space Enable (MSE):** This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the Packet Hub memory-mapped registers. The Base Address register for Packet Hub should be programmed before this bit is set.	
00	0b	RW		Reserved For future compatibility, it is recommended writing 0 to this bit.	

Notes:
1. Reserved: This bit is reserved for future expansion. Only "0" will be accepted as the write data to the reserved bit. When "1" is written the operation is not guaranteed.

3.3.1.4 PCISTS—PCI Status Register

Table 53. 06h: PCISTS- PCI Status Register (Sheet 1 of 2)

Size: 16-bit			Default: 0010h		Power Well: Core
Access	PCI Configuration		B:D:F D0:F0		Offset Start: 06h Offset End: 07h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15	0b	RO		**Reserved**[1]	
14	0b	RWC	SSE	**Signaled System Error:** This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message	
13	0b	RWC	RMA	**Received Master Abort:** Primary received Unsupported Request Completion Status.	
12	0b	RWC	RTA	**Received Target Abort:** Primary received Abort Completion Status	
11	0b	RWC	STA	**Signaled Target Abort:** Primary transmitted Abort Completion Status	
10 : 05	00h	RO		Reserved[1]	
04	1b	RO	CPL	**Capabilities List:** This bit indicates the presence of a capabilities list.	
03	0b	RO	ITRPSTS	**Interrupt Status:** This bit reflects the status of this function's interrupt at the input of the enable/disable logic. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.	

Table 53. 06h: PCISTS- PCI Status Register (Sheet 2 of 2)

Size: 16-bit			**Default:** 0010h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 06h **Offset End:** 07h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
02 : 00	000b	RO		Reserved[1]	

Notes:
1. Reserved: This bit is reserved for future expansion. Only "0" will be accepted as the write data to the reserved bit. When "1" is written the operation is not guaranteed.

3.3.1.5 RID— Revision Identification Register

Table 54. 08h: RID- Revision Identification Register

Size: 8-bit			**Default:** 01h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 08h **Offset End:** 08h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 : 00	01h	RO		**Revision ID:** Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.	

3.3.1.6 CC— Class Code Register

Table 55. 09h: CC - Class Code Register

Size: 24-bit			**Default:** FF0000h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 09h **Offset End:** 0Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
23 : 16	FFh	RO	BCC	**Base Class Code (BCC):** FFh = No categorized.	
15 : 08	00h	RO	SCC	**Sub Class Code (SCC):** 00h = No categorized	
07 : 00	00h	RO	PI	**Programming Interface (PI):** 00h = No categorized	

3.3.1.7 MLT— Master Latency Timer Register

Table 56. 0Dh: MLT - Master Latency Timer Register

Size: 8-bit			**Default:** 00h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 0Dh **Offset End:** 0Dh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 : 00	00h	RO	MLT	**Master Latency Timer (MLT):** Hardwired to 00h. The Packet Hub is implemented internal to the Intel® PCH EG20T and not arbitrated as a PCI device.	

3.3.1.8 HEADTYP— Header Type Register

Table 57. 0Eh: HEADTYP - Header Type Register

Size: 8-bit			**Default:** 80h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 0Eh **Offset End:** 0Eh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07	1b	RO	MFD	**Multi-Function Device:** 1 = Multi-function device.
06 : 00	00h	RO	CONFIGLAYOUT	**Configuration Layout:** Hardwired to 00h, which indicates the standard PCI configuration layout.

3.3.1.9 MEM_BASE— MEM Base Address Register

Table 58. 14h: MEM_BASE - MEM Base Address Register

Size: 32-bit			**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 14h **Offset End:** 17h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 : 11	000000h	RW	BA	**Base Address:** Bits 31:11 claim a 2048 byte address space	
10 : 04	00h	RO		Reserved	
03	0b	RO	PREFETCHABLE	**Prefetchable:** Hardwired to 0 indicating that this range should not be prefetched.	
02 : 01	000b	RO	TYPE	**Type:** Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.	
00	0b	RO	RTE	**Resource Type Indicator (RTE):** Hardwired to 0 indicating that the base address field in this register maps to memory space.	

3.3.1.10 ROM_BASE— Extended ROM Base Address Register

Table 59. 30h: ROM_BASE - Extended ROM Base Address Register

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 30h **Offset End:** 33h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 : 17	0000h	RW	BA	**Base Address:** Bits 31: 17 claim a 128K byte address space
16 : 01	0000h	RO		Reserved
00	0b	RW	ADE	**Address Decode Enable (ADE):** If set to 1 by software, Extended ROM maps to Memory space.

3.3.1.11 SSVID— Subsystem Vendor ID Register

Table 60. 2Ch: SSVID - Subsystem Vendor ID Register

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 2Ch **Offset End:** 2Dh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 : 00	0000h	RWO	SSVID	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value

3.3.1.12 SSID— Subsystem ID Register

Table 61. 2Eh: SID - Subsystem ID Register

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 2Eh **Offset End:** 2Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 : 00	0000h	RWO	SSID	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value

3.3.1.13 CAP_PTR— Capabilities Pointer Register

Table 62. 34h: CAP_PTR - Capabilities Pointer Register

Size: 8-bit			**Default:** 40h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 34h **Offset End:** 34h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 : 00	40h	RO	PTR	**Pointer (PTR):** This register points to the starting offset of the Packet Hub capabilities ranges.	

3.3.1.14 INT_LN— Interrupt Line Register

Table 63. 3Ch: INT_LN - Interrupt Line Register

Size: 8-bit			**Default:** FFh		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 3Ch **Offset End:** 3Ch
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 : 00	FFh	RW	INT_LN	**Interrupt Line (INT_LN):** This data is not used by the Intel® PCH EG20T. It is to communicate to software the interrupt line that the interrupt pin is connected to.	

3.3.1.15 INT_PN— Interrupt Pin Register

Table 64. 3Dh: INT_PN - Interrupt Pin Register

Size: 8-bit			**Default:** 00h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 3Dh **Offset End:** 3Dh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 : 00	00h	RO	INT_PN	**Interrupt Pin:** Hardwired to 00h indicating that this function does not generate interrupt.	

3.3.1.16 MSI_CAPID—MSI Capability ID Register

Since there is no interrupt source in the Packet Hub, the MSI message is not sent upstream from the Packet Hub to the PCI Express bus. The value of the MSI registers in the Packet Hub does not affect MSI operation of the Intel® PCH EG20T.

Table 65. 40h: MSI_CAPID - MSI Capability ID Register

Size: 8-bit			**Default:** 05h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 40h **Offset End:** 40h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 : 00	05h	RO	MSI_CAPID	**MSI Capability ID:** A value of 05h indicates that this identifies the MSI register set.

3.3.1.17 MSI_NPR—MSI Next Item Pointer Register

Table 66. 41h: MSI_NPR - MSI Next Item Pointer Register

Size: 8-bit			**Default:** 50h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 41h **Offset End:** 41h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 : 00	50h	RO	NEXT_PV	**Next Item Pointer Value:** Value of 50h indicates that power management registers capabilities list.

3.3.1.18 MSI_MCR—MSI Message Control Register

Since there is no interrupt source in the Packet Hub, the MSI message is not sent upstream from the Packet Hub to the PCI Express bus. The value of the MSI registers in the Packet Hub does not affect MSI operation of the Intel® PCH EG20T.

Table 67. 42h: MSI_MCR - MSI Message Control Register

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 42h **Offset End:** 43h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 : 08	00h	RO		Reserved
07	0b	RO	C64	**64 Bit Address Capable:** 0 = 32bit capable only
06 : 04	000b	RW	MME	**Multiple Message Enable (MME):** Indicates actual number of messages allocated to the device
03 : 01	000b	RO	MMC	**Multiple Message Capable (MMC):** Indicates that the Packet Hub supports 1 interrupt message
00	0b	RW	MSIE	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts

3.3.1.19 MSI_MAR—MSI Message Address Register

Since there is no interrupt source in the Packet Hub, the MSI message is not sent upstream from the Packet Hub to the PCI Express bus. The value of the MSI registers in the Packet Hub does not affect MSI operation of the Intel® PCH EG20T.

Table 68. 44h: MSI_MAR - MSI Message Address Register

Size: 32-bit			**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 44h **Offset End:** 47h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 : 02	00000000h	RW	ADDR	**Address (ADDR):** Lower 32 bits of the system specified message address, always DWord aligned	
01 : 00	00b	RO		Reserved	

3.3.1.20 MSI_MD—MSI Message Data Register

Since there is no interrupt source in the Packet Hub, the MSI message is not sent upstream from the Packet Hub to the PCI Express bus. The value of the MSI registers in the Packet Hub does not affect MSI operation of the Intel® PCH EG20T.

Table 69. 48h: MSI_MD - MSI Message Data Register

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 48h **Offset End:** 49h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 : 00	0000h	RW	DATA	**Data (DATA):** When MSI is enabled, this 16-bit field is programmed by system software.	

3.3.1.21 PM_CAPID—PCI Power Management Capability ID Register

Table 70. 50h: PM_CAPID - PCI Power Management Capability ID Register

Size: 8-bit			**Default:** 01h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 50h **Offset End:** 50h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 : 00	01h	RO	PMC_ID	**Power Management Capability ID:** A value of 01h indicates that this is a PCI Power Management capabilities field.	

3.3.1.22 PM_NPR—PM Next Item Pointer Register

Table 71. 51h: PM_NPR - PM Next Item Pointer Register

Size: 8-bit			**Default:** 00h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 51h **Offset End:** 51h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 : 00	00h	RO	NEXT_P1V	**Next Item Pointer:** Hardwired to 00h to indicate that power management is the last item in the capabilities list.	

3.3.1.23 PM_CAP—Power Management Capabilities Register

Table 72. 52h: PM_CAP - Power Management Capabilities Register

Size: 16-bit			**Default:** 0002h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 52h **Offset End:** 53h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 : 11	00000b	RO	PME_SUP	**PME Support (PME_SUP):** This 5-bit field indicates the power states in which the Function may assert PME#. The Packet Hub does not support the D1 or D2 states. For all other states, the Packet Hub is capable of generating PME#. Software should never need to modify this field.	
10	0b	RO	D2_SUP	**D2 Support (D2_SUP):** 0 = D2 State is not supported	
09	0b	RO	D1_SUP	**D1 Support (D1_SUP):** 0 = D1 State is not supported	
08 : 06	000b	RO	AUX_CUR	**Auxiliary Current (AUX_CUR):** This function does not support the D3cold state.	
05	0b	RO	DSI	**Device Specific Initialization (DSI):** The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.	
04	0b	RO		Reserved	
03	0b	RO	PME_CLK	**PME Clock (PME_CLK):** The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.	
02 : 00	010b	RO	VER	**Version (VER):** The Intel® PCH EG20T reports 010b indicating that it complies with the PCI Power Management Specification Revision 1.1.	

3.3.1.24 PWR_CNTL_STS—Power Management Control/Status Register

Table 73. 54h: PWR_CNTL_STS - Power Management Control/Status Register

Size: 16-bit			Default: 0000h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 54h Offset End: 55h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15	0b	RO	STS	**PME Status (STS):** The Packet Hub does not generate PME#.	
14 : 13	00b	RO	DSCA	**Data Scale (DSCA):** Hardwired to 00b indicating it does not support the associated Data register.	
12 : 09	0h	RO	DSEL	**Data Select (DSEL):** Hardwired to 0000b indicating it does not support the associated Data register.	
08 : 02	00h	RO		Reserved	
01 : 00	00b	RW	POWERSTATE	**Power State:** This 2-bit field is used both to determine the current power state of Packet Hub function and to set a new power state. The definition of the field values are: 00b = D0 state 11b = D3hot state If software attempts to write a value of 10b or 01b into this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3hot state, the Intel® PCH EG20T must not accept accesses to the Packet Hub memory range; but the configuration space must still be accessible. When software changes this value from the D3hot state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the Function.	

3.3.2 Memory-Mapped I/O Registers (BAR: MEM_BASE)

3.3.2.1 Packet Hub ID Register

Table 74. 000h: Packet Hub ID Register

Size: 32-bit			Default: Fixed*		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 000h Offset End: 003h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 : 00	Fixed*	RO	PHID	**Packet Hub ID:** This value indicate Chip production ID	

Notes:
1. Packet Hub ID Register is fixed value by hardware.
2. Only DWord accesses to these registers are permitted.

3.3.2.2 Queue Priority Value Register

Table 75. 004h: Queue Priority Value Register

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 004h **Offset End:** 007h

Bit Range	Default	Access	Acronym	Description
31 : 27	00h	RO		Reserved
26 : 24	000b	RW	D12PRIORITY	Device 12 Priority
23	0b	RO		Reserved
22 : 20	000b	RW	D10PRIORITY	Device 10 Priority
19	0b	RO		Reserved
18 : 16	000b	RW	D8PRIORITY	Device 8 Priority
15	0b	RO		Reserved
14 : 12	000b	RW	D6PRIORITY	Device 6 Priority
11	0b	RO		Reserved
10 : 08	000b	RW	D4PRIORITY	Device 4 Priority
07	0b	RO		Reserved
06 : 04	000b	RW	D2PRIORITY	Device 2 Priority
03	0b	RO		Reserved
02 : 00	000b	RW	D0PRIORITY	Device 0 Priority

Notes:
1. This register determines the priority of Packet transmission. A priority can be specified independently for every Device. High priority Device is granted for transaction, in the meantime transactions from lower priority Devices are pending. For Devices with same priority, transactions are granted based on Round-Robin sequence. Priority value 000b: Highest priority, 111b Lowest priority.
2. Only DWord accesses to these registers are permitted.

3.3.2.3 Upstream Queue Max Size Register

Table 76. 008h: Upstream Queue Max Size Register (Sheet 1 of 2)

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 008h **Offset End:** 00Bh

Bit Range	Default	Access	Acronym	Description
31 : 26	00h	RO		Reserved
25 : 24	00b	RW	FD12MCODE	from Device 12 Queue Max Size-code
23 : 22	00b	RO		Reserved
21 : 20	00b	RW	FD10MCODE	from Device 10 Queue Max Size-code
19 : 18	00b	RO		Reserved
17 : 16	00b	RW	FD8MCODE	from Device 8 Queue Max Size-code

Table 76. 008h: Upstream Queue Max Size Register (Sheet 2 of 2)

Size: 32-bit			Default: 00000000h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 008h Offset End: 00Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 : 14	00b	RO		Reserved	
13 : 12	00b	RW	FD6MCODE	from Device 6 Queue Max Size-code	
11 : 10	00b	RO		Reserved	
09 : 08	00b	RW	FD4MCODE	from Device 4 Queue Max Size-code	
07 : 06	00b	RO		Reserved	
05 : 04	00b	RW	FD2MCODE	from Device 2 Queue Max Size-code	
03 : 02	00b	RO		Reserved	
01 : 00	00b	RW	FD0MCODE	from Device 0 Queue Max Size-code	

Notes:
1. The meaning of the code 00b: No-limit, 01b: 4-packet, 10b: 8-packet, 11b: 16-packet.
2. Only DWord accesses to these registers are permitted.

3.3.2.4 Downstream Queue Max Size Register

Table 77. 00Ch: Downstream Queue Max Size Register

Size: 32-bit			Default: 00000000h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 00Ch Offset End: 00Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 : 26	00b	RO		Reserved	
25 : 24	00b	RW	TD12MCODE	to Device 12 Queue Max Size-code	
23 : 22	00b	RO		Reserved	
21 : 20	00b	RW	TD10MCODE	to Device 10 Queue Max Size-code	
19 : 18	00b	RO		Reserved	
17 : 16	00b	RW	TD8MCODE	to Device 8 Queue Max Size-code	
15 : 14	00b	RO		Reserved	
13 : 12	00b	RW	TD6MCODE	to Device 6 Queue Max Size-code	
11 : 10	00b	RO		Reserved	
09 : 08	00b	RW	TD4MCODE	to Device 4 Queue Max Size-code	
07 : 06	00b	RO		Reserved	
05 : 04	00b	RW	TD2MCODE	to Device 2 Queue Max Size-code	
03 : 02	00b	RO		Reserved	
01 : 00	00b	RW	TD0MCODE	to Device 0 Queue Max Size-code	

Notes:
1. The meaning of the code 00b: No-limit, 01b: 4-packet, 10b: 8-packet, 11b: 16-packet.
2. Only DWord accesses to these registers are permitted.

3.3.2.5 Completion Response Time-out Register

Table 78. 010h: Completion Response Time-out Register

Size: 32-bit			**Default:** 02222222h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 010h **Offset End:** 013h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 : 26	00b	RO		Reserved	
25 : 24	10b	RW	D12CST	Device 12 Completion response time out Code	
23 : 22	00b	RO		Reserved	
21 : 20	10b	RW	D10CST	Device 10 Completion response time out Code	
19 : 18	00b	RO		Reserved	
17 : 16	10b	RW	D8CST	Device 8 Completion response time out Code	
15 : 14	00b	RO		Reserved	
13 : 12	10b	RW	D6CST	Device 6 Completion response time out Code	
11 : 10	00b	RO		Reserved	
09 : 08	10b	RW	D4CST	Device 4 Completion response time out Code	
07 : 06	00b	RO		Reserved	
05 : 04	10b	RW	D2CST	Device 2 Completion response time out Code	
03 : 02	00b	RO		Reserved	
01 : 00	10b	RW	D0CST	Device 0 Completion response time out Code	

Notes:
1. The meaning of this code 00b: [Infinite], 01b:[50us], 10b: [10ms], 11b: [50ms].
2. Only DWord accesses to these registers are permitted.

3.3.2.6 Device Read Pre-Fetch Control Register

Table 79. 014h: Device Read Pre-Fetch Control Register (Sheet 1 of 2)

Size: 32-bit			**Default:** 00000000h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 014h **Offset End:** 017h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 : 28	00b	RW		Reserved	
27 : 26	00b	RW	D12EXTV	Device 12 extension time Value Code	
25 : 24	00b	RW	D12PMRW	Device 12 Pre-Memory Read DWord Size Value Code	
23 : 22	00b	RW	D10EXTV	Device 10 slave extension time Value Code	
21 : 20	00b	RW	D10PMRW	Device 10 Pre-Memory Read DWord Size Value Code	
19 : 18	00b	RW	D8EXTV	Device 8 slave extension time Value Code	

Table 79. 014h: Device Read Pre-Fetch Control Register (Sheet 2 of 2)

Size: 32-bit			Default: 00000000h	Power Well: Core
Access	PCI Configuration		B:D:F D0:F0	Offset Start: 014h Offset End: 017h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
17 : 16	00b	RW	D8PMRW	Device 8 Pre-Memory Read DWord Size Value Code
15 : 14	00b	RW	D6EXTV	Device 6 slave extension time Value Code
13 : 12	00b	RW	D6PMRW	Device 6 Pre-Memory Read DWord Size Value Code
11 : 10	00b	RW	D4EXTV	Device 4 slave extension time Value Code
09 : 08	00b	RW	D4PMRW	Device 4 Pre-Memory Read DWord Size Value Code
07 : 06	00b	RW	D2EXTV	Device 2 slave extension time Value Code
05 : 04	00b	RW	D2PMRW	Device 2 Pre-Memory Read DWord Size Value Code
03 : 02	00b	RW	D0EXTV	Device 0 slave extension time Value Code
01 : 00	00b	RW	D0PMRW	Device 0 Pre-Memory Read DWord Size Value Code

Notes:
1. The meaning of Pre-Memory Read DWord Size Value Code 00b: [No-Pre Read], 01b: [32 DWords], 10b: [64 DWords], 11b: [128 DWords].
2. The meaning of slave extension time Value Code 00b: [8 clock cycles wait], 01b: [16 clock cycles wait], 10b: [32 clock cycles wait], 11b: [64 clock cycles wait]
3. This register controls speculative DMA transfers of Device.
4. When internal PCI compatible bus performs Read access by 16 bursts (1 burst = 16 DWords), the size of pre-fetch is specified by "Memory Read DWord Size Value Code"
5. The time specified by "slave extension time Value Code" delays change of a bus master.
6. Only DWord accesses to these registers are permitted.

3.3.2.7 Dead Lock Avoid Type Selector Register

Table 80. 018h: Dead Lock Avoid Type Selector Register

Size: 32-bit			Default: 00000000h	Power Well: Core
Access	PCI Configuration		B:D:F D0:F0	Offset Start: 018h Offset End: 01Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 : 01	00000000h	RO		Reserved
00	0b	RW	DLAT	Dead Lock Avoid type select 0 = Dead Lock Avoid System 1st Stop Upstream 1 = Dead Lock Avoid System 1st Stop Downstream

Note: Only DWord accesses to these registers are permitted.

3.3.2.8 Interrupt Pin Register Write Permit Register 0

Table 81. 020h: Interrupt Pin Register Write Permit Register 0

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 020h **Offset End:** 023h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 : 21	0h	RO		Reserved
20	0b	RW	D2F4IPR	Device 2 Function 4 Interrupt Pin register Write Permit
19	0b	RW	D2F3IPR	Device 2 Function 3 Interrupt Pin register Write Permit
18	0b	RW	D2F2IPR	Device 2 Function 2 Interrupt Pin register Write Permit
17	0b	RW	D2F1IPR	Device 2 Function 1 Interrupt Pin register Write Permit
16	0b	RW	D2F0IPR	Device 2 Function 0 Interrupt Pin register Write Permit
15 : 03	0h	RO		Reserved
02	0b	RW	D0F2IPR	Device 0 Function 2 Interrupt Pin register Write Permit
01	0b	RW	D0F1IPR	Device 0 Function 1 Interrupt Pin register Write Permit
00	0b	RW	D0F0IPR	Device 0 Function 0 Interrupt Pin register Write Permit

Notes:
1. If Interrupt Pin register Write Permit is "1", write access to Interrupt Pin register is permitted.
2. Only DWord accesses to these registers are permitted.

3.3.2.9 Interrupt Pin Register Write Permit Register 1

Table 82. 024h: Interrupt Pin Register Write Permit Register 1

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0	**Offset Start:** 024h **Offset End:** 027h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 : 17	0h	RO		Reserved
16	0b	RW	D6F0IPR	Device 6 Function 0 Interrupt Pin register Write Permit
15 : 02	0h	RO		Reserved
01	0b	RW	D4F1IPR	Device 4 Function 1 Interrupt Pin register Write Permit
00	0b	RW	D4F0IPR	Device 4 Function 0 Interrupt Pin register Write Permit

Notes:
1. If Interrupt Pin register Write Permit is "1", write access to Interrupt Pin register is permitted.
2. Only DWord accesses to these registers are permitted.

3.3.2.10 Interrupt Pin Register Write Permit Register 2

Table 83. 028h: Interrupt Pin Register Write Permit Register 2

Size: 32-bit			Default: 00000000h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 028h Offset End: 02Bh
Bit Range	Default	Access	Acronym	Description	
31 : 21	0h	RO		Reserved	
20	0b	RW	D10F4IPR	Device 10 Function 4 Interrupt Pin register Write Permit	
19	0b	RW	D10F3IPR	Device 10 Function 3 Interrupt Pin register Write Permit	
18	0b	RW	D10F2IPR	Device 10 Function 2 Interrupt Pin register Write Permit	
17	0b	RW	D10F1IPR	Device 10 Function 1 Interrupt Pin register Write Permit	
16	0b	RW	D10F0IPR	Device 10 Function 0 Interrupt Pin register Write Permit	
15: 04	0h	RO		Reserved	
03	0b	RW	D8F3IPR	Device 8 Function 3 Interrupt Pin register Write Permit	
02	0b	RW	D8F2IPR	Device 8 Function 2 Interrupt Pin register Write Permit	
01	0b	RW	D8F1IPR	Device 8 Function 1 Interrupt Pin register Write Permit	
00	0b	RW	D8F0IPR	Device 8 Function 0 Interrupt Pin register Write Permit	

Notes:
1. If Interrupt Pin register Write Permit is "1", write access to Interrupt Pin register is permitted.
2. Only DWord accesses to these registers are permitted.

3.3.2.11 Interrupt Pin Register Write Permit Register 3

Table 84. 02Ch: Interrupt Pin Register Write Permit Register 3

Size: 32-bit			Default: 00000000h		Power Well: Core
Access		PCI Configuration	B:D:F D0:F0		Offset Start: 02Ch Offset End: 02Fh
Bit Range	Default	Access	Acronym	Description	
31 : 05	0h	RO		Reserved	
04	0b	RW	D12F4IPR	Device 12 Function 4 Interrupt Pin register Write Permit	
03	0b	RW	D12F3IPR	Device 12 Function 3 Interrupt Pin register Write Permit	
02	0b	RW	D12F2IPR	Device 12 Function 2 Interrupt Pin register Write Permit	
01	0b	RW	D12F1IPR	Device 12 Function 1 Interrupt Pin register Write Permit	
00	0b	RW	D12F0IPR	Device 12 Function 0 Interrupt Pin register Write Permit	

Notes:
1. If Interrupt Pin register Write Permit is "1", write access to Interrupt Pin register is permitted.
2. Only DWord accesses to these registers are permitted.

3.3.2.12 Interrupt Reduction Control Register

Interrupt Reduction Control register exists for each PCI Function (except for D0:F0 Packet Hub Control) as shown in Section 3.4.2.1, "Related Registers" on page 111 and the addresses for them are listed in Section 3.2.2.2, "Device Control Registers" on page 89.

Table 85. 040h: Interrupt Reduction Control Register

Size: 32-bit			**Default:** 00020000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 040h-23C **Offset End:** 043h-23Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 : 24	00h	RO		Reserved	
23 : 16	002h	RW		Reserved	
15 : 10	00h	RO		Reserved	
09 : 00	000h	RW	IWV	Interrupt Wait value	

Notes:
1. The time period of this value is 5 microseconds.
2. "Interrupt Wait value" sets up delay time, after an interrupt occurs until it sends a packet.
3. Only DWord accesses to these registers are permitted.

3.4 Functional Description

3.4.1 QoS

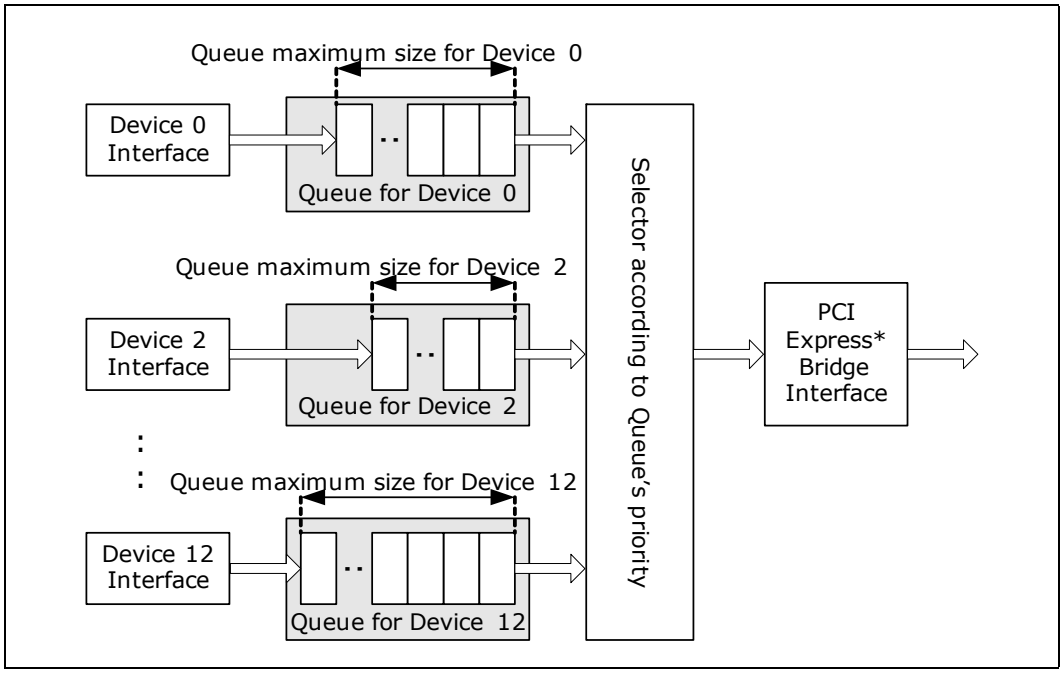
QoS is controlled at the Device level.

The parameters of QoS are the Queue max size and level of priority for each Device.

Queue max size restricts the quantity of packets from the Device to the Queue. In other words, packets from the Device beyond this value do not go into the Queue.

Priority determines the priority of packet transmission. A priority can be specified independently for every Device. High priority Device is granted for transaction, in the meantime transactions from lower priority Devices are pending. For Devices with same priority, transactions are granted based on Round-Robin sequence. There are eight priority levels.

Figure 4. QoS Mechanism



Example 1: When having the priority of CAN the highest value 000b is set to the "BASE(Dev0, Func0 BAR1 register value)+004h [bit 26: 24]". Even when the speed of PCI Express Bridge falls off, upstream-data of CAN is transmitted without failure.

3.4.1.1 Related Registers

Priority register determines the priority of packet transmission. A priority can be specified independently for every Device. High priority Device is granted for transaction, in the meantime transactions from lower priority Devices are pending. For Devices with same priority, transactions are granted based on Round-Robin sequence.

Priority value 000b means highest priority, and 111b means lowest priority

The meaning of the size codes:

- 00b: No-limit
- 01b: 4-packet is maximum
- 10b: 8-packet is maximum
- 11b: 16-packet is maximum

Table 86. List of QoS Control Registers (Sheet 1 of 2)

Device Number	Parameter= Register [bit position]	Function Number	Internal Function
0	priority = QP_VAL [2: 0] size = UPQ_MXSZ [1: 0]	0	Packet Hub
		1	Gigabit Ethernet MAC
		2	GPIO

Table 86. List of QoS Control Registers (Sheet 2 of 2)

Device Number	Parameter= Register [bit position]	Function Number	Internal Function
2	priority= QP_VAL [6: 4] size= UPQ_MXSZ [5: 4]	0	USB OHCI
		1	USB OHCI
		2	USB OHCI
		3	USB EHCI
		4	USB Device
4	priority= QP_VAL [10: 8] size= UPQ_MXSZ [9: 8]	0	SD Host
		1	SD Host
6	priority= QP_VAL [14: 12] size= UPQ_MXSZ [13: 12]	0	SATA
8	priority= QP_VAL [18: 16] size= UPQ_MXSZ [17: 16]	0	USB OHCI
		1	USB OHCI
		2	USB OHCI
		3	USB EHCI
10	priority= QP_VAL [22: 20] size= UPQ_MXSZ [21: 20]	0	Shared DMA
		1	UART #0
		2	UART #1
		3	UART #2
		4	UART #3
12	priority= QP_VAL [26: 24] size= UPQ_MXSZ [25: 24]	0	Shared DMA
		1	SPI
		2	I^2C
		3	CAN
		4	IEE1588

3.4.2 Interrupt Reduction Mechanism

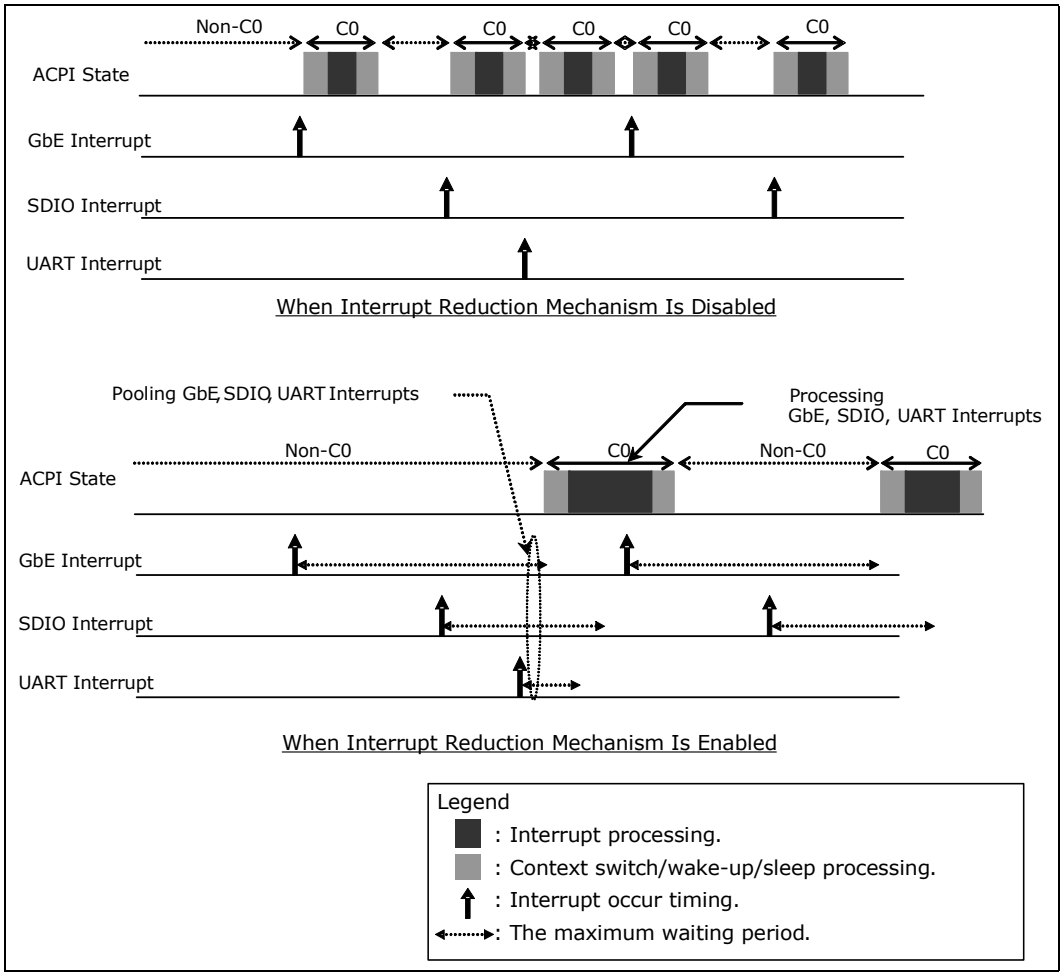
When an interrupt occurs the interrupt circuit notifies this mechanism. This mechanism pools the interrupt. Simultaneously down counting is started. The initial value of down count (for every interrupt) can be changed by software.

All of the interrupts that have been pooled are sent to the CPU when the down count value becomes 0.

According to this mechanism, the CPU can process two or more interrupts simultaneously.

Figure 5 illustrates that this mechanism allows the CPU to remain in low-power C-states longer.

Figure 5. Effect of Interrupt Reduction Mechanism



3.4.2.1 Related Registers

Table 87. List of Interrupt Reduction Control Registers

Device Number	Function Number	Internal Function	Register
0	0	Packet Hub	---
	1	Gigabit Ethernet MAC	INTRD_D0F1
	2	GPIO	INTRD_D0F2
2	0	USB OHCI	INTRD_D2F0
	1	USB OHCI	INTRD_D2F1
	2	USB OHCI	INTRD_D2F2
	3	USB EHCI	INTRD_D2F3
	4	USB Device	INTRD_D2F4
4	0	SD Host	INTRD_D4F0
	1	SD Host	INTRD_D4F1
6	0	SATA	INTRD_D6F0
8	0	USB OHCI	INTRD_D8F0
	1	USB OHCI	INTRD_D8F1
	2	USB OHCI	INTRD_D8F2
	3	USB EHCI	INTRD_D8F3
10	0	Shared DMA	INTRD_D10F0
	1	UART #0	INTRD_D10F1
	2	UART #1	INTRD_D10F2
	3	UART #2	INTRD_D10F3
	4	UART #3	INTRD_D10F4
12	0	Shared DMA	INTRD_D12F0
	1	SPI	INTRD_D12F1
	2	I^2C	INTRD_D12F2
	3	CAN	INTRD_D12F3
	4	IEE1588	INTRD_D12F4

Note: Refer to Section 3.3.2.12. for details

Table 88 shows the relationship between PCI Function and INT*x*. One MSI is available to each PCI Function.

Table 88. List of INT*x* and MSI

Device Number	Function Number	Internal Function	IntPin	Device Level	Chip Level	Number of MSI
0	0	Packet Hub	0	-	-	-
	1	Gigabit Ethernet MAC	1	INTA	INTA	1
	2	GPIO	1	INTA	INTA	1
2	0	USB OHCI	2	INTB	INTD	1
	1	USB OHCI	2	INTB	INTD	1
	2	USB OHCI	2	INTB	INTD	1
	3	USB EHCI	2	INTB	INTD	1
	4	USB Device	2	INTB	INTD	1
4	0	SD Host	3	INTC	INTC	1
	1	SD Host	3	INTC	INTC	1
6	0	SATA	4	INTD	INTB	1
8	0	USB OHCI	1	INTA	INTA	1
	1	USB OHCI	1	INTA	INTA	1
	2	USB OHCI	1	INTA	INTA	1
	3	USB EHCI	1	INTA	INTA	1
10	0	Shared DMA	2	INTB	INTD	1
	1	UART #0	2	INTB	INTD	1
	2	UART #1	2	INTB	INTD	1
	3	UART #2	2	INTB	INTD	1
	4	UART #3	2	INTB	INTD	1
12	0	Shared DMA	3	INTC	INTC	1
	1	SPI	3	INTC	INTC	1
	2	I^2C	3	INTC	INTC	1
	3	CAN	3	INTC	INTC	1
	4	IEEE1588	3	INTC	INTC	1

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4.0 Serial ROM Interface

4.1 Overview

The Serial ROM interface controls the Serial ROM (SROM) interconnect using the SPI protocol. This interface performs following roles:

- Initialization of hardware for Ethernet function and of PCI configuration. The SPI-ROM operates using packet mode, which performs 4 bytes of Read or Write at a time (56 SPI-cycle/operation).
  - — Initialization of MAC-address of Gigabit Ethernet
  - — Initialization of "Subsystem ID" or "Subsystem Vendor ID" of each PCI device in the Intel® Platform Controller Hub EG20T
- Access to option ROM space for AHCI SATA function (ROM mode).

4.1.1 Terminal Connection When Not Connecting Serial ROM

The terminal connection for the case when the Serial ROM is not connected is listed as follows. The operation of the Intel® PCH EG20T is not guaranteed if this guideline is not followed.

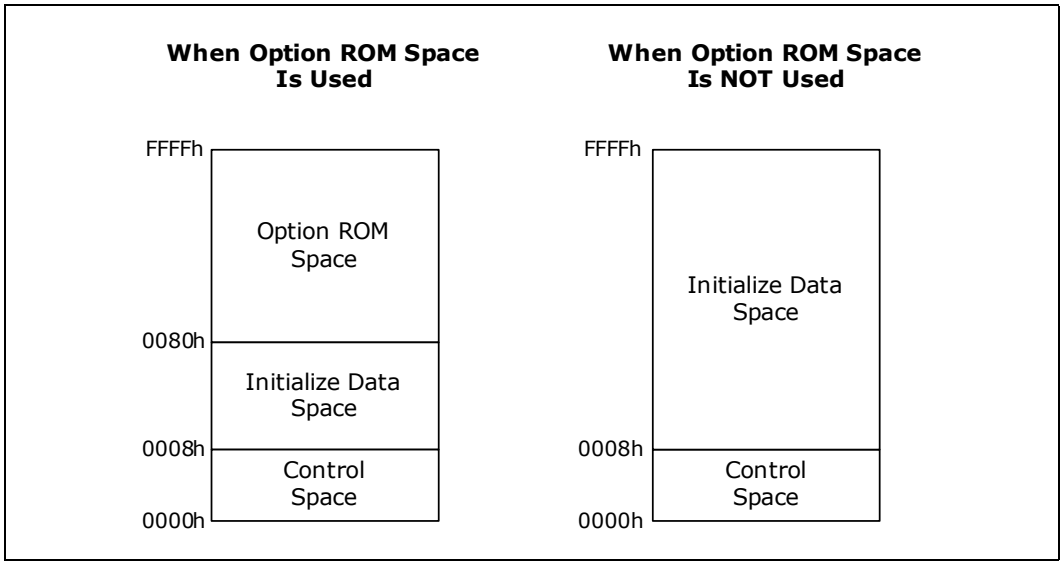
- sromif_cs - Open
- sromif_clk - Open
- sromif_dout - Open
- sromif_din - Pull-down 10 kΩ resistor

4.1.2 Serial ROM Address Map Structure

The Serial ROM is SPI EEPROM (from 1 kB to 64 kB) supporting 8-bit transactions. The Serial ROM connects directly to the Serial ROM interconnect. Serial ROM address MAP is shown as follows.

Note: Intel® Platform Controller Hub EG20T reverses Byte alignment in DWord boundary through Expansion ROM Space. Please refer to Section 4.2.3, "Example of Serial ROM Data" on page 120 for an example.

Figure 6. Address Map of Each Use Case



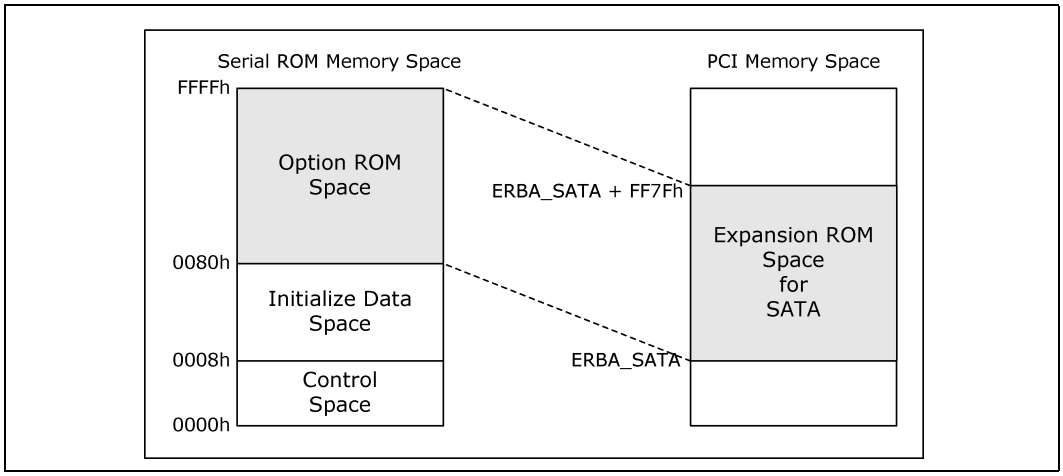
4.1.2.1 Option ROM Space

This space is the Expansion ROM space for the SATA interface (Device No= 6, Function No= 0). The relationship between Serial ROM address and Expansion ROM Space Address is expressed by the following formulas.

Serial ROM address = PCI address - **ERBA_SATA** + 0080h

Note: **ERBA_SATA** is the Expansion ROM Base Address Value of SATA.

Figure 7. Relationship Between Option ROM Space in Serial ROM and Expansion ROM Space of SATA



4.1.2.2 Initialize Data Space

The Initialize data is contained in this space. Initialize data is used for two purposes:

- Initialization of MAC-address of Gigabit Ethernet

- Initialization of Subsystem ID or Subsystem Vendor ID of each PCI device in the Intel® PCH EG20T

4.1.2.2.1 Structure of Initialization of MAC Address of Gigabit Ethernet

DWord Addr	Byte Addr [+3]								Byte Addr [+2]								Byte Addr [+1]								Byte Addr [+0]							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0
1	All"0"								All"0"								All"0"								80h							
2	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0
3	MAC[47:40]								MAC [39:32]								MAC [31:24]								MAC [23:16]							
4	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1
5	MAC [15:8]								MAC [7:0]								All"0"								All"0"							
6	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	1	0
7	01h								All"0"								All"0"								All"0"							

Note: Data size is 24 bytes.

4.1.2.2.2 Structure of Initialization of Subsystem ID or Subsystem Vendor ID

Device No and **Func No** are the Device numbers and Function numbers of the device.

- When setting up only Subsystem ID, a Subsystem Vendor ID value is set to 0.
- When setting up only Subsystem Vendor ID, a Subsystem ID value is set to 0.
- When not using "Expansion ROM Space for SATA," it can be repeated for each device in the Intel® PCH EG20T. The number of repetitions is restricted to 14. When writing in the same address, the data written later is effective.

DWord Addr	Byte Addr [+3]								Byte Addr [+2]								Byte Addr [+1]								ByteAddr [+0]							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	**Device No**								**Func No**							
1	Subsystem Vendor ID [7:0]								Subsystem Vendor ID [15:8]								Subsystem ID [7:0]								Subsystem ID [15:8]							

Note: Data size is 8 bytes.

Table 89 shows the relationship between a device (built into the Intel® PCH EG20T) and Device No. and Func No.

Table 89. List of PCI Device and Function Number in the Intel® Platform Controller Hub EG20T (Sheet 1 of 2)

Device Name	Device No	Func No	Device Name	Device No	Func No
Packet Hub	0	0	Local DMA	10	0
Gigabit Ethernet MAC	0	1	UART FIFO256	10	1
GPIO	0	2	UART FIFO64 #0	10	2

Table 89. List of PCI Device and Function Number in the Intel® Platform Controller Hub EG20T (Sheet 2 of 2)

USB OHCI #0	2	0	UART FIFO64 #1	10	3
USB OHCI #1	2	1	UART FIFO64 #2	10	4
USB OHCI #2	2	2	Local DMA	12	0
USB EHCI	2	3	SPI	12	1
USB device	2	4	I^2C	12	2
SD Host #0	4	0	CAN	12	3
SD Host #1	4	1	IEEE1588	12	4
SATA	6	0			
USB OHCI #3	8	0			
USB OHCI #4	8	1			
USB OHCI #5	8	2			
USB EHCI	8	3			

Initialize data space is constituted from:

- Not more than one initialization of MAC-address of Gigabit Ethernet data
- Zero or more Initialization of Subsystem ID or Subsystem Vendor ID data
- Last 8 bytes all 0 data (indicate the end of Initialize Data Space)

4.1.2.3 Control Space

Control Space is used for state observation and write control of SROM via registers. The registers are explained in Section 4.2.2.2, “Special Address” on page 119.

4.2 Functional Description

4.2.1 Operation Mode

The two operation modes are as follows:

1. Packet Write mode
   - At Intel® PCH EG20T start-up, the Serial ROM interface operates in Packet Write mode (initialization by hardware for Functions)
   - It starts to download the MAC address of Gigabit Ethernet automatically from the external ROM
   - When Serial ROM is not connected, Packet Write mode is immediately completed by pull-down of sromif_din pin.
   - After the processing ends, it shifts to ROM mode.
2. ROM mode (accessing ROM space for Function)
   - Serial ROM interface responds to all the bus requests after power supply; it is necessary to manage requests with software so as not to request Serial ROM interface at the same time.
   - When simultaneous accesses are carried out, an operation is guaranteed, but a waiting time becomes long.
   - In order to write in Serial ROM, it is necessary to set the bit-0 of Serial ROM Interface Control Register to "1."

4.2.2 ROM Mode

Serial ROM is seen as EEPROM of the width of DWord connected with the internal bus in ROM mode. Therefore, Read/Write of each DWord is possible.

The program must perform 1 DWord of Serial ROM write accesses at a time. (Read access supports Byte, Word and DWord). When 1 DW write operation (32 bits = 1 DW) is completed, a waiting time of 5 ms is generated following completion.

The sequence "1 DW writing -> 5ms wait" must be repeated for subsequent operations.

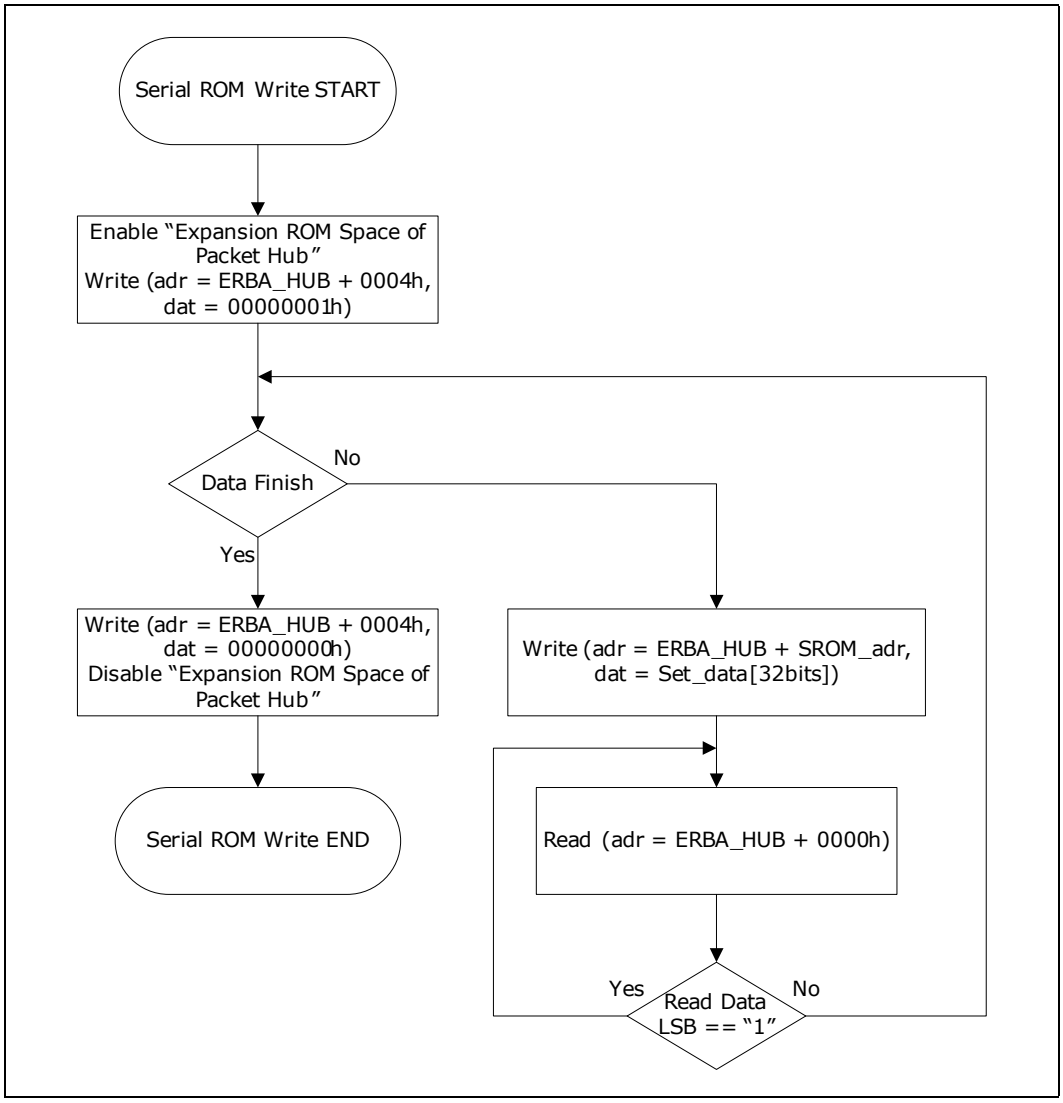
However, high-speed writing is possible by the observation of the Status Register in Serial ROM.

4.2.2.1 The Serial ROM Writing Method

Data can be written in Serial ROM using the Serial ROM Interface.

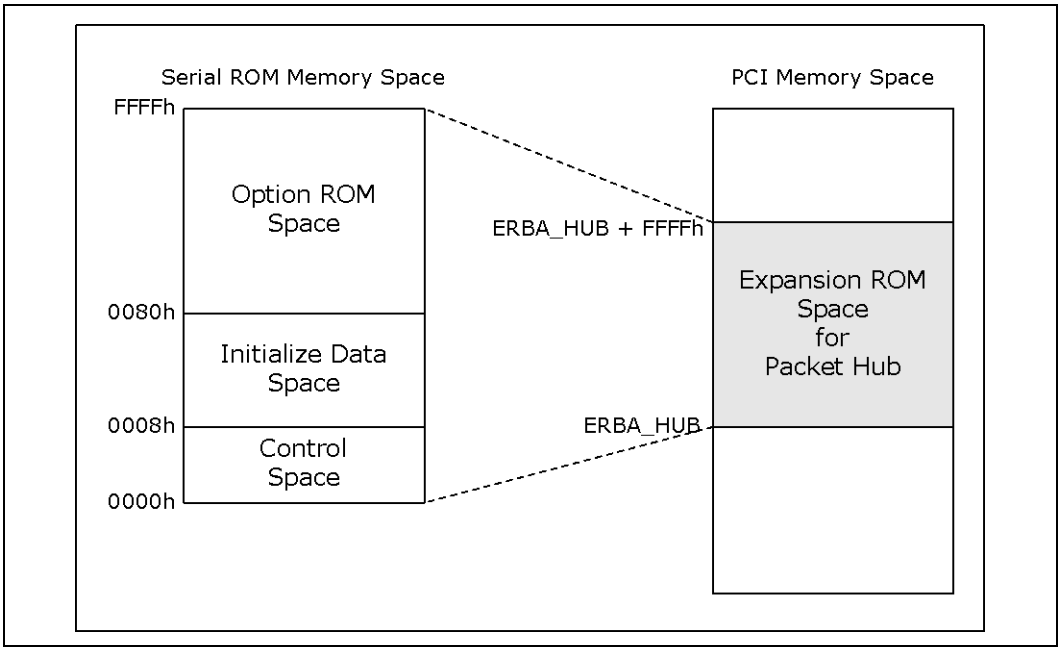
Data is written in Serial ROM using the Expansion ROM space of Packet Hub (Device No=0, Func No=0). Be sure to write in by 32-bit width. Writing flow is shown in Figure 8.

Figure 8. Serial ROM Write Flowchart



Note: ERBA_HUB defined as Table 59, "30h: ROM_BASE - Extended ROM Base Address Register" on page 95.

Figure 9. Relationship Between 'Serial ROM Space' and 'Expansion ROM Space of Packet Hub



4.2.2.2 Special Address

Serial ROM Address = 0000h

It is reserved as Status Register.

Therefore, Read/Write to Serial ROM address 0000h = Read/Write to Status Register.

4.2.2.2.1 Status Register

Table 90. 00h: Status Register (Sheet 1 of 2)

Size: 32-bit		**Default:** 00h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 00h **Offset End:** 03h
	Memory Mapped IO	**BAR** ERBA_HUB		**Offset:** 00h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :04	0h	RO	RSVD	**Reserved**
03 :02	0	RW	BP	**Serial ROM Array Addresses Protected Control** "00" Non Array Addresses Protected "01" Higher 1/4 Array Addresses Protected "10" Higher 1/2 Array Addresses Protected "11" All Array Addresses Protected
01	0	RO	WEL	**Serial ROM Write Enable Latch** 0 = Indicates that the device is not write enabled 1 = Indicates that the device is write enabled

Table 90. 00h: Status Register (Sheet 2 of 2)

Size: 32-bit		Default: 00h		Power Well: Core
Access	PCI Configuration	B:D:F D0:F0		Offset Start: 00h Offset End: 03h
	Memory Mapped IO	BAR ERBA_HUB		Offset: 00h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
00	0b	RO	WIP	**Serial ROM Write In Process** 0 = Indicates that the device is ready 1 = Indicates that the write cycle is in progress

4.2.2.2.2 Serial ROM Interface Control Register

Table 91. 04h: Serial ROM Interface Control Register

Size: 32-bit		Default: 00h		Power Well: Core
Access	PCI Configuration	B:D:F D0:F0		Offset Start: 04h Offset End: 07h
	Memory Mapped IO	BAR ERBA_HUB		Offset: 04h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :01	00h	RO		Reserved.
00	0b	RW	SROMPMT	**Serial ROM Permit:** In order to write in Serial ROM, it is necessary to set this bit to "1".

4.2.3 Example of Serial ROM Data

4.2.3.1 When Not Using Initialize Function

Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data
0008h	00h	0009h	00h	000Ah	00h	000Bh	00h
000Ch	00h	000Dh	00h	000Eh	00h	000Fh	00h

Note: Even when not using Initialize, 8 bytes of "0" is required.

4.2.3.2 Only MAC Address Set

This example sets MAC-address = **12:34:56:78:9A:BC**

Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data
0008h	BCh	0009h	10h	000Ah	01h	000Bh	02h
000Ch	00h	000Dh	00h	000Eh	00h	000Fh	80h
0010h	BCh	0011h	10h	0012h	01h	0013h	18h
0014h	**12h**	0015h	**34h**	0016h	**56h**	0017h	**78h**
0018h	BCh	0019h	10h	001Ah	01h	001Bh	19h
001Ch	**9Ah**	001Dh	**BCh**	001Eh	00h	001Fh	00h

Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data	Serial ROM Address	Data
0020h	BCh	0021h	10h	0022h	01h	0023h	3Ah
0024h	01h	0025h	00h	0026h	00h	0027h	00h
0028h	00h	0029h	00h	002Ah	00h	0028h	00h
002Ch	00h	002Dh	00h	002Eh	00h	002Fh	00h

Note: ETHER_MODE (GbE offset 08h register) is changed into "1: Operates in GMII/RGMII Mode" by this SROM processing.

4.2.3.3 Only Subsystem ID or Subsystem Vendor ID Set

This example GPIO (Device No = 0, Func No = 2) set Subsystem ID = **3344h**

Serial ROM Address	Data	Serial ROM Address	Data	SERIAL ROM Address	Data	SERIAL ROM Address	Data
0008h	7Ch	0009h	00h	000Ah	02h	000Bh	0Bh
000Ch	00h	000Dh	00h	000Eh	**44h**	000Fh	**33h**
0010h	00h	0011h	00h	0012h	00h	0013h	00h
0014h	00h	0015h	00h	0016h	00h	0017h	00h

4.2.3.4 MAC Address & Subsystem ID or Subsystem Vendor ID Set

This example sets MAC-address= **89:AB:CD:EF:01:23**, IEE1588 (Device No = 12 Func No = 4)and sets Subsystem ID = **1234h**, Subsystem Vender ID= **FEDCh**

SERIAL ROM Address	Data	SERIAL ROM Address	Data	SERIAL ROM Address	Data	SERIAL ROM Address	Data
0008h	BCh	0009h	10h	000Ah	01h	000Bh	02h
000Ch	00h	000Dh	00h	000Eh	00h	000Fh	80h
0010h	BCh	0011h	10h	0012h	01h	0013h	18h
0014h	**89h**	0015h	**ABh**	0016h	**CDh**	0017h	**EFh**
0018h	BCh	0019h	10h	001Ah	01h	001Bh	19h
001Ch	**01h**	001Dh	**23h**	001Eh	00h	001Fh	00h
0020h	BCh	0021h	10h	0022h	01h	0023h	3Ah
0024h	01h	0025h	00h	0026h	00h	0027h	00h
0028h	7Ch	0029h	00h	002Ah	64h	002Bh	0Bh
002Ch	**DCh**	002Dh	**FEh**	002Eh	**34h**	002Fh	**12h**
0030h	00h	0031h	00h	0032h	00h	0033h	00h
0034h	00h	0035h	00h	0036h	00h	0037h	00h

Note: ETHER_MODE (GbE offset 08h register) is changed into "1: Operates in GMII/RGMII Mode" by this SROM processing.

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5.0 Clocks

5.1 Overview

This chapter describes the Intel® Platform Controller Hub EG20T clock system control. The Intel® PCH EG20T contains many clock frequency domains to support its various interfaces. Table 92 summarizes these domains and Figure 10 shows the Intel® PCH EG20T clock diagram. For additional information about clock and reset sequences, refer to Chapter 6.0, "Power Management".

5.2 Clock Description

Table 92. Clock Domains (Clock Inputs/Peripheral Clocks)

Clock Domain	Signal Name	Frequency	Source (Example)
PCI Express	pcie_clkp pcie_clkn	100 MHz	Clock Generator
SATA	sata0_clkp sata0_clkn	75 MHz	Clock Generator
USB host	usb_48mhz	48 MHz	Crystal oscillator
USB device			
Gigabit Ethernet / System Clock	sys_25mhz	25 MHz	Crystal oscillator
UART	uart_clk	Up to 64 MHz	Crystal oscillator or USB_48MHz or SYS_25MHz

Table 93. Clock Domains (Derivative Clocks/Peripheral Clocks) (Sheet 1 of 2)

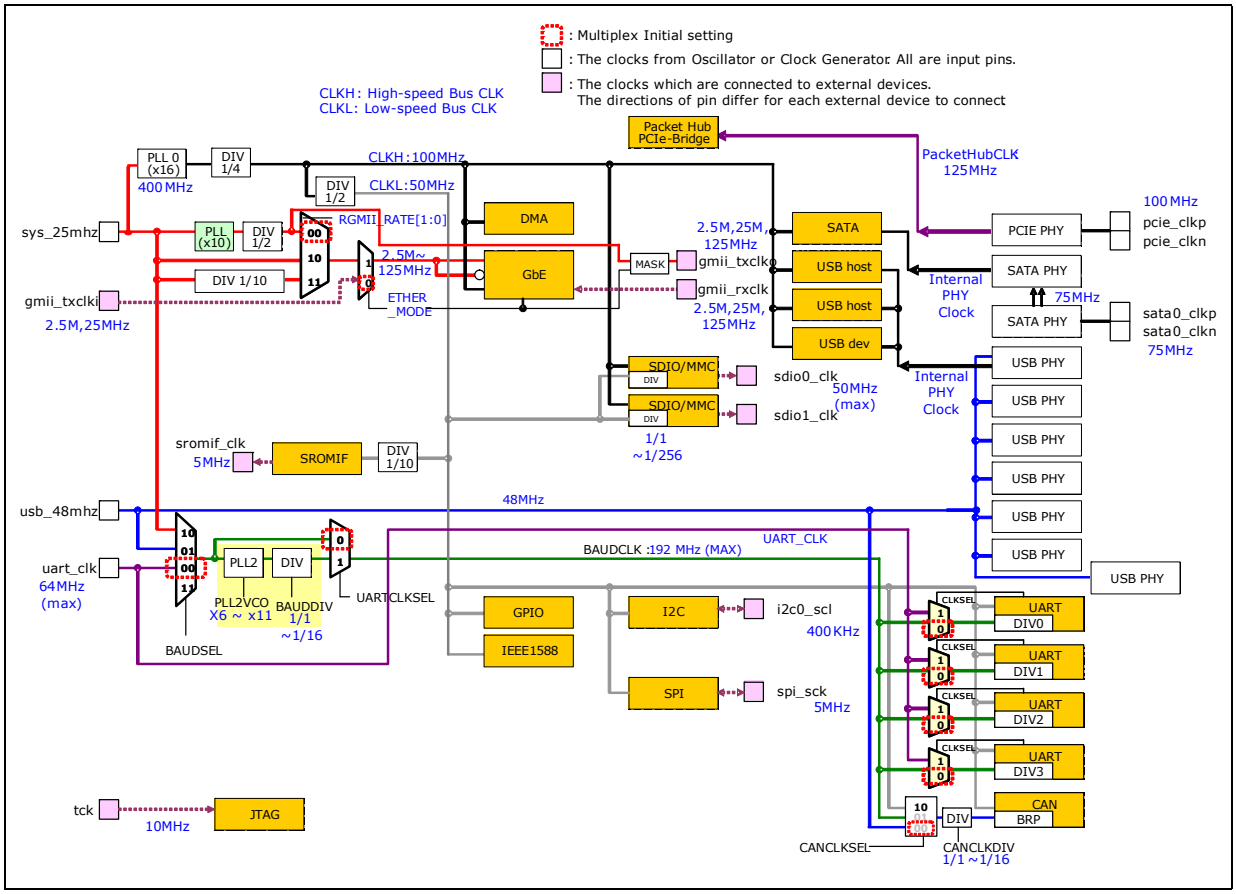
Clock Domain	Signal Name	Frequency	Source
Gigabit Ethernet	gmii_rxclk gmii_txclki gmii_txclko	Up to 125 MHz	Gigabit Ethernet PHY
SD/SDIO/MMC	sdio0_clk sdio1_clk	Up to 50 MHz	Intel® PCH EG20T (internal bus clock)
I^2C	i2c0_scl	400 KHz	Intel® PCH EG20T (internal bus clock) or External I^2C device
SPI	spi_sck	5 MHz	Intel® PCH EG20T (internal bus clock) or External SPI device
JTAG	tck	Up to 10 MHz	External JTAG clock
SROMIF	sromif_clk	5 MHz	SYS_25MHz (PLL0 output)
Baud Rate Clock for UART	BAUDCLK	Up to 192 MHz	PLL2 output

Table 93. Clock Domains (Derivative Clocks/Peripheral Clocks) (Sheet 2 of 2)

Clock Domain	Signal Name	Frequency	Source
Intel® PCH EG20T Internal	PacketHubCLK	125 MHz	PCI Express internal PLL output
	CLKH (High Speed Bus Clock)	100 MHz	SYS_25MHz (PLL0 output)
	CLKL (Low Speed Bus Clock)	50 MHz	SYS_25MHz (PLL0 output)

5.3 Clock Block Diagram

Figure 10. Intel® Platform Controller Hub EG20T Clock Block Diagram



Note: CANCLKSEL bit should be initialized to "1xb" by software.

5.4 Registers

5.4.1 Memory-Mapped I/O Registers

Table 94. List of Registers

Offset	Name	Symbol	Access	Size [bits]	Initial Value
PKTHubCTLBASE + 500h	CLOCK Configuration Register	CLKCFG	RW	32	20000C00

Note: PKTHubCTLBASE is the IO-BASE or MEM-BASE register of the Packet Hub (D0:F0).

5.4.1.1 Clock Configuration Register (CLKCFG)

Table 95. 500h: CLKCFG- Clock Configuration Register (Sheet 1 of 2)

Size: 32-bit			**Default:** 20000C00		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D0:F0		**Offset Start:** 500h **Offset End:** 503h
	Memory Mapped I/O		**BAR:** PKTHubCTLBASE		**Offset:** 500h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 : 28	0010b	RW	CANDIV	**Divider Setting for the CAN Clock** 0000= divided by 16 1000= divided by 8 0100= divided by 4 0010= divided by 2 0001= divided by 1 Other= Prohibited	
27	0b	RW	CAN_PWRCHG	This bit is used to choose how the power state changes when it changes to D3. 0 = The power State is changed to D3 in the state of IDLE of a CAN bus. 1 = The power State is immediately changed to D3 not related the state of a CAN bus.	
26	0b	RO		Reserved	
25 : 24	00b	RW	CANCLKSEL	**CAN Clock Selection**. This bit should be initialized to "1xb" by software before using CAN. 0x= Prohibited. 1x= CLKL (50MHz)	
23 : 20	0h	RW	BAUDDIV	**Divider Setting for the PLL2 Output**. 0000= divide by 16 1111= divide by 15 1110= divide by 14 : 0010= divide by 2 0001= divide by 1	
19	0b	RO		Reserved	
18	0b	RW	UARTCLKSEL	**UART Clock Select** 0 = Clock selected by BAUDSEL. 1 = PLL2 output	
17 : 16	00b	RW	BAUDSEL	**Baud Clock Select** 00= UART_CLK (From LSI pin) 01= USB_48MHz 1x= SYS_25MHz	

Table 95. 500h: CLKCFG- Clock Configuration Register (Sheet 2 of 2)

Size: 32-bit			**Default:** 20000C00		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D0:F0		**Offset Start:** 500h **Offset End:** 503h
		Memory Mapped I/O	**BAR:** PKTHubCTLBASE		**Offset:** 500h
Bit Range		**Default**	**Access**	**Acronym**	**Description**
15	: 13	000b	RO		Reserved
12	: 09	0110b	RW	PLL2VCO	**VCO Setting for PLL2**. 0110= x 6 0111= x 7 1000= x 8 1001= x 9 1010= x 10 1011= x 11 Other = prohibited
	08	0b	RW	PLL2PD	**PLL2 Power Down.** 0 = PLL2 Enable 1 = PLL2 Power Down
07	: 05	000b	RO		Reserved
	04	0b	RW	PLL1PD	**PLL1 Power Down.** 0 = PLL1 Enable 1 = PLL1 Power Down
03	: 01	000b	RO		Reserved
	00	0b	RW	PLL0PD	**PLL0 Power Down.** 0 = PLL0 Enable 1 = PLL0 Power Down

Note: Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

5.5 Functional Description

5.5.1 System Clock

5.5.1.1 Packet Hub Clock

The Packet Hub Block clock is supplied with PCI Express 125 MHz.

5.5.1.2 Internal BUS Clock of Each Function

Internal Bus Clocks (CLKH=100MHz, CLKL=50MHz) are derived from SYS_25MHz clock.

Until the oscillator and PLL0 output are stabilized, system reset input signal must be kept asserted. Refer to Section 6.0, "Power Management" on page 135 for further information about the clocks and resets.

5.5.2 Peripheral Clock

5.5.2.1 Baud Rate Clock (UART/CAN)

Figure 11 shows the structure of the baud rate generation for the UART blocks.

The baud rate clock is generated as follows:

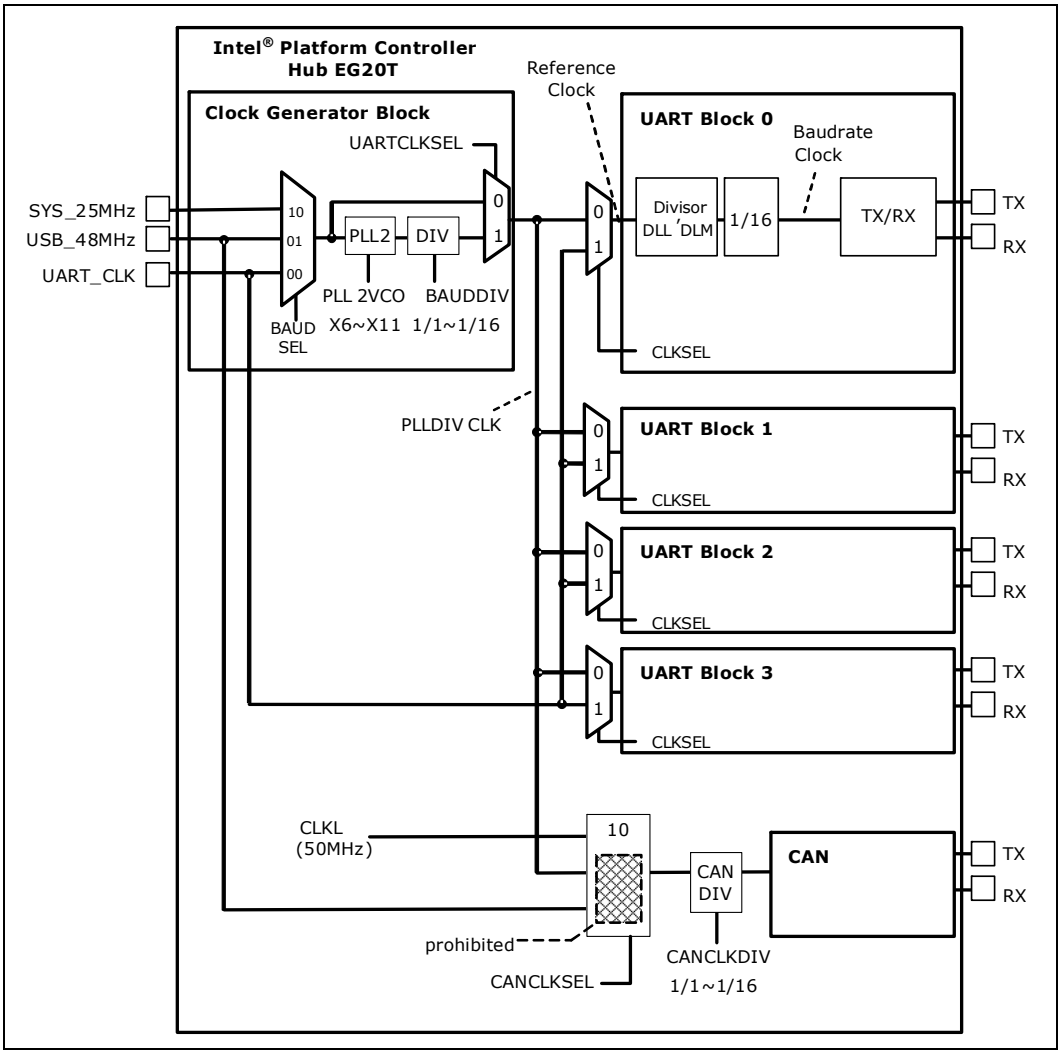
[Baud rate] = [Reference clock] / 16

The Reference Clock is selected from the external clock inputs by setting the registers BAUDSEL, PLL2VCO, and BAUDDIV. Table 96 and Table 98 show the examples of the frequency selection.

The frequency of the Reference Clock is up to 192 MHz. Also, the frequency of the PLL2 output is from 250 MHz to 450 MHz.

The Baud rate should be selected with the sequences described in the following sections. Refer to Chapter 17.0, "UART" for further information.

Figure 11. Baud Rate Generation



Note: CANCLKSEL bit is allowed only setting to "1xb".

Table 96. Baud Rate Generation Example_1

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz] BAUDDIV 1	2	3	4
SYS_ 25MHz	25	10b	6	150	150.00	75.00	50.00	37.50
			7	175	175.00	87.50	58.33	43.75
			8	200	200.00	100.00	66.67	50.00
			9	225	225.00	112.50	75.00	56.25
			10	250	250.00	125.00	83.33	62.50
			11	275	275.00	137.50	91.67	68.75
USB_ 48MHz	48	01b	6	288	288.00	144.00	96.00	72.00
			7	336	336.00	168.00	112.00	84.00
			8	384	384.00	192.00	128.00	96.00
			9	432	432.00	216.00	144.00	108.00
			10	480	480.00	240.00	160.00	120.00
			11	528	528.00	264.00	176.00	132.00
UART _CLK	64	00b	6	384	384.00	192.00	128.00	96.00
			7	448	448.00	224.00	149.33	112.00
			8	512	512.00	256.00	170.67	128.00
			9	576	576.00	288.00	192.00	144.00
			10	640	640.00	320.00	213.33	160.00
			11	704	704.00	352.00	234.67	176.00

Note: Gray cells: are prohibited.

Table 97. Baud Rate Generation Example_2 (Sheet 1 of 2)

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz] BAUDDIV 5	6	7	8
SYS_ 25MHz	25	10b	6	150	30.00	25.00	21.43	18.75
			7	175	35.00	29.17	25.00	21.88
			8	200	40.00	33.33	28.57	25.00
			9	225	45.00	37.50	32.14	28.13
			10	250	50.00	41.67	35.71	31.25
			11	275	55.00	45.83	39.29	34.38

Table 97. Baud Rate Generation Example_2 (Sheet 2 of 2)

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz] BAUDDIV 5	6	7	8
USB_ 48MHz	48	01b	6	288	57.60	48.00	41.14	36.00
			7	336	67.20	56.00	48.00	42.00
			8	384	76.80	64.00	54.86	48.00
			9	432	86.40	72.00	61.71	54.00
			10	480	96.00	80.00	68.57	60.00
			11	528	105.60	88.00	75.43	66.00
UART _CLK	64	00b	6	384	76.80	64.00	54.86	48.00
			7	448	89.60	74.67	64.00	56.00
			8	512	102.40	85.33	73.14	64.00
			9	576	115.20	96.00	82.29	72.00
			10	640	128.00	106.67	91.43	80.00
			11	704	140.80	117.33	100.57	88.00

Note: Gray cells are prohibited.

Table 98. Baud Rate Generation Example_3 (Sheet 1 of 2)

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz] BAUDDIV 9	10	11	12
SYS_ 25MHz	25	10b	6	150	16.67	15.00	13.64	12.50
			7	175	19.44	17.50	15.91	14.58
			8	200	22.22	20.00	18.18	16.67
			9	225	25.00	22.50	20.45	18.75
			10	250	27.78	25.00	22.73	20.83
			11	275	30.56	27.50	25.00	22.92
USB_ 48MHz	48	01b	6	288	32.00	28.80	26.18	24.00
			7	336	37.33	33.60	30.55	28.00
			8	384	42.67	38.40	34.91	32.00
			9	432	48.00	43.20	39.27	36.00
			10	480	53.33	48.00	43.64	40.00
			11	528	58.67	52.80	48.00	44.00

Table 98. Baud Rate Generation Example_3 (Sheet 2 of 2)

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz] BAUDDIV 9	10	11	12
UART _CLK	64	00b	6	384	42.67	38.40	34.91	32.00
			7	448	49.78	44.80	40.73	37.33
			8	512	56.89	51.20	46.55	42.67
			9	576	64.00	57.60	52.36	48.00
			10	640	71.11	64.00	58.18	53.33
			11	704	78.22	70.40	64.00	58.67

Note: Gray cells are prohibited

Table 99. Baud Rate Generation Example_4

Clock PIN	Input Frequency (maximum) [MHz]	BAUD SEL	PLL2 VCO	PLL Output Frequency [MHz]	Reference Clock Frequency [MHz] BAUDDIV 13	14	15	16
SYS_ 25MHz	25	10b	6	150	11.54	10.71	10.00	9.38
			7	175	13.46	12.50	11.67	10.94
			8	200	15.38	14.29	13.33	12.50
			9	225	17.31	16.07	15.00	14.06
			10	250	19.23	17.86	16.67	15.63
			11	275	21.15	19.64	18.33	17.19
USB_ 48MHz	48	01b	6	288	22.15	20.57	19.20	18.00
			7	336	25.85	24.00	22.40	21.00
			8	384	29.54	27.43	25.60	24.00
			9	432	33.23	30.86	28.80	27.00
			10	480	36.92	34.29	32.00	30.00
			11	528	40.62	37.71	35.20	33.00
UART _CLK	64	00b	6	384	29.54	27.43	25.60	24.00
			7	448	34.46	32.00	29.87	28.00
			8	512	39.38	36.57	34.13	32.00
			9	576	44.31	41.14	38.40	36.00
			10	640	49.23	45.71	42.67	40.00
			11	704	54.15	50.29	46.93	44.00

Note: Gray cells are prohibited

5.5.2.2 UART Clock Selection Sequence Without PLL Setting

Use the following sequence when the external clock is to be selected directly as a Reference Clock of the UART:

1. Assert the software reset of the UART block.
   (SOFT RESET Register or PWR_CNTL_STS Register)
2. Set UARTCLKSEL = 0 (CLKCFG register bit[18]).
   External clock is selected. (PLL2 is bypassed.)
3. Set PLL2PD = 1 (CLKCFG register bit[8]).
   PLL2 clock output is suspended.
4. Set BAUDSEL by setting CLKCFG register bit[17:16].
5. Set CLKSEL = 0.
   External clock is selected as the Reference Clock for UART.
6. Release the software reset of the UART block.

5.5.2.3 UART Clock Selection Sequence With PLL Setting

The following software sequence is required to use the PLL2 output to the Reference Clock of the UART:

1. Assert the software reset of the UART block.
   (SOFT RESET Register or PWR_CNTL_STS Register)
2. Set UARTCLKSEL = 0 (CLKCFG register bit[18]).
   PLL2 is bypassed.
3. Set PLL2PD = 1 (CLKCFG register bit[8]).
   PLL2 clock output is suspended.
4. Set BAUDSEL by setting CLKCFG register bit[17:16].
5. Set PLL2VCO by setting CLKCFG register bit[12:9].
6. Set PLL2PD = 0 (CLKCFG register bit[8]).
   PLL2 clock output starts running.
7. Wait 150 us.
8. Set UARTCLKSEL = 1 (CLKCFG register bit[18]).
   PLL2 output is selected as PLLDIVCLK.
9. Set CLKSEL = 0.
   PLL2 output is selected as the Reference Clock for UART.
10. Release the software reset of the UART block.

5.5.2.4 Gigabit Ethernet Transmission Clock Control

Input/output of the Transmission Clock in various modes of Gigabit Ethernet RGMII/ GMII/MII, differs based on the mode.

In RGMII mode, irrespective of the transfer rate, the clock is always supplied to external PHY from Gigabit Ethernet MAC. Input the clock of desired frequency generated within the Intel® PCH EG20T, from the gmii_txclki pin.

1. In GMII mode, the clock is supplied from the Gigabit Ethernet MAC to the external PHY. Input the 125 MHz Clock that was generated within the Intel® PCH EG20T from the gmii_txclki pin.

2. At the time of MII mode (10/100 Mbps), the clock is supplied from external PHY to Gigabit Ethernet MAC. Input the clock entered from the external pin of PHY-LSI in gmii_txclki.

Figure 12. Transmission Clock Control Example

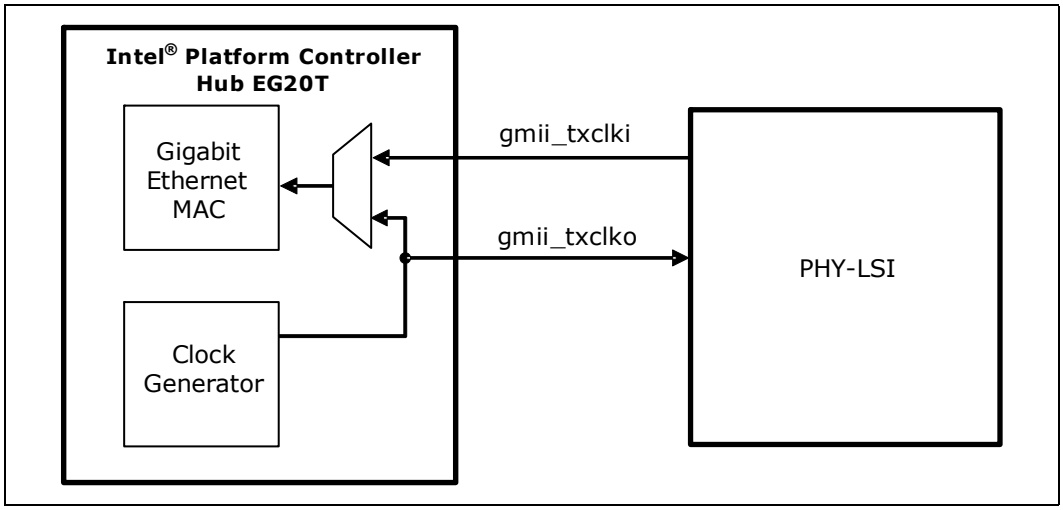


Table 100. Transmission Clock Control

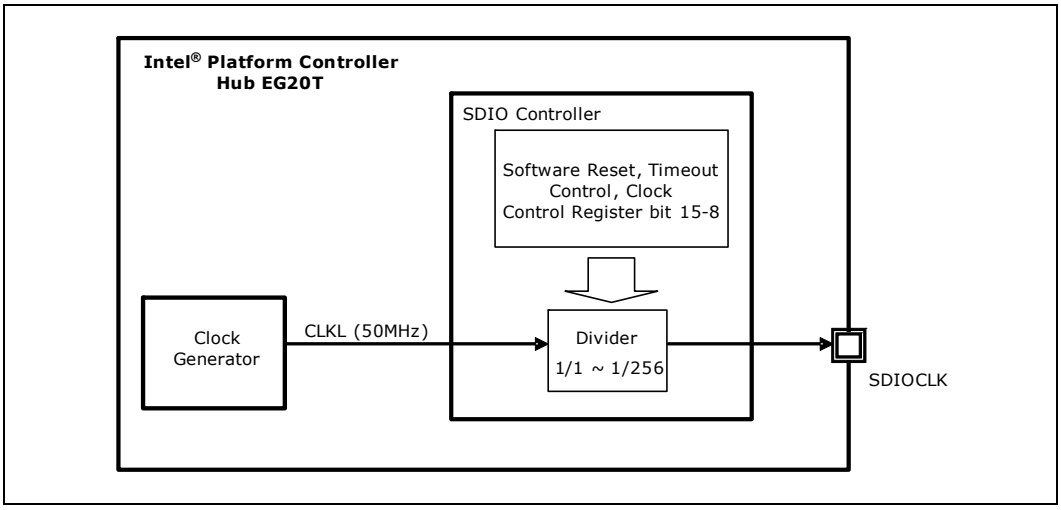
Mode	Transmit Clock	Mode Register	RGMII Control Register	
		ETHER_MODE	RGMII_MODE	RGMII_RATE
GMII	Intel® PCH EG20T -> PHY	1	0(initial)	00(initial)
MII(100Mbps)	External -> Intel® PCH EG20T	0	0(initial)	00(initial)
MII(10Mbps)	External -> Intel® PCH EG20T	0	0(initial)	00(initial)
RGMII(1000Mbps)	Intel® PCH EG20T -> PHY	1	1	0
RGMII(100Mbps)	Intel® PCH EG20T -> PHY	1	1	10
RGMII(10Mbps)	Intel® PCH EG20T -> PHY	1	1	11

5.5.2.5 SDIO Clock Control

Source clock of SDIOCLK is the Intel® PCH EG20T internal peripheral clock: CLKL (50 MHz).

Software Reset, Time-out Control, Clock Control Register bits 8-15 are used for selecting an SDIOCLK frequency (1/1 ~ 1/256 CLKL).

Figure 13. SDIO Clock Control Example



5.5.2.5.1 SDIO Clock Control

1. Acquire the SDIO Clock data in the Capabilities Register.
2. Set up the Internal Clock Enable and SDIOCLK Frequency Select after calculating a dividing ratio.
3. Confirm the Internal Clock Stable.
4. Set the SDIO Clock Enable to ON.

5.5.2.5.2 SDIO Clock Stop

1. Confirm that there is no transmission on SDIO bus by monitoring DAT&CMD in Present State Register.
2. Set the SDIO Clock Enable to OFF.

5.5.2.5.3 SDIO Clock Frequency Change

1. Suspend the SDIO clock according to the procedure of SDIO Clock Stop.
2. Set up the SDIOCLK Frequency Select after calculating a dividing ratio.
3. Confirm the Internal Clock Stable.
4. Set the SDIO Clock Enable to ON.

Note: Suspend the clock once before changing SD clock frequency.

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6.0 Power Management

6.1 Features

Features of the Power Management sub-system are as follows:

- Support for Advanced Configuration and Power Interface (ACPI) version 3.0
- System Clock Control
- System Sleep State Control
- Wake-up from the system sleep state.

6.1.1 Pin Description

Table 101. List of Pins

Pin Name	I/O	Initial Status	Initial Value	Description
rst_pla_n	I	I	-	RESET input for the power plane A
rst_plb_n	I	I	-	RESET input for the power plane B
rst_plc_n	I	I	-	RESET input for the power plane C
slp_plb_n	I	I	-	SLEEP state input for the power plane B
slp_plc_n	I	I	-	SLEEP state input for the power plane C
pwrgd	I	I	-	The system voltage supply becoming valid
wake_out_n	O	O	Hi-z (open drain)	Interrupt output derivative by wake-up event

6.2 Functional Description

6.2.1 Device State

6.2.1.1 Theory of Operation

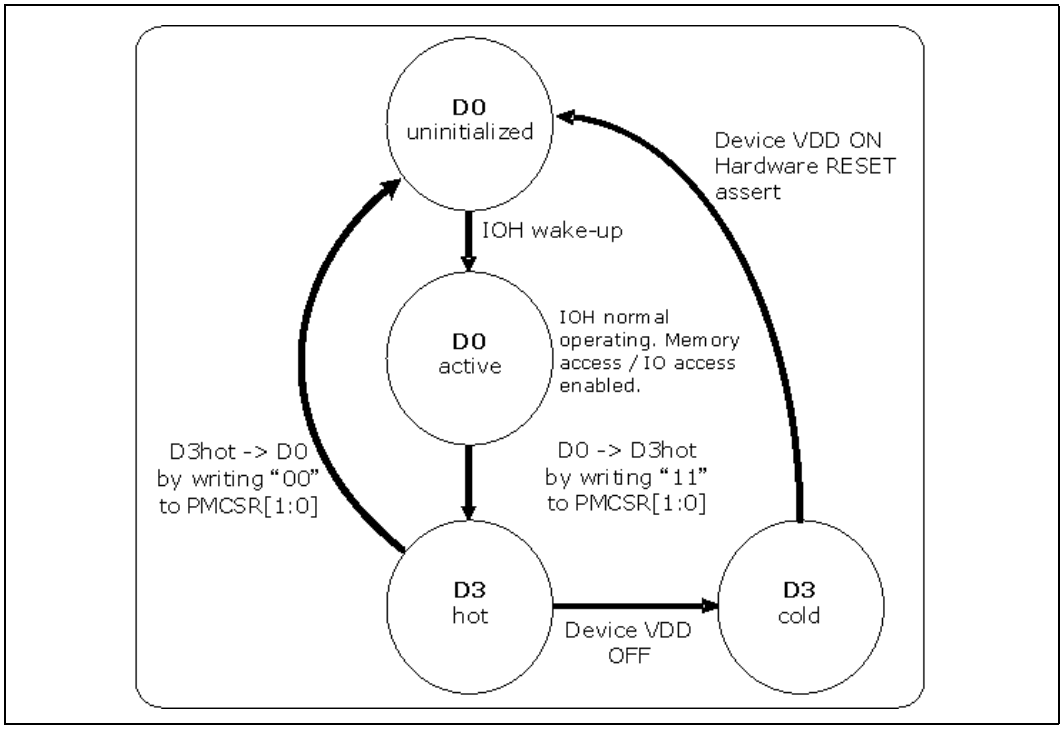
The state transition chart of the device state is shown in Figure 14.

The Intel® PCH EG20T supports these power states:

- D0
- D3hot

The power consumption at D0 is the highest and at D3hot is the lowest. When the Intel® PCH EG20T is initialized, the power state becomes D0 (D0 is in the state of normal operation). When changing from D3hot to D0 or asserting the power on reset, the Intel® PCH EG20T enters the D0 state.

Figure 14. State Transition Chart



Note: D0 is divided into two distinct sub-states, the "un-initialized" sub-state and the "active" sub-state. When a PCI Express* component initially has VDD power applied, it comes out of reset state and it defaults to the D0 uninitialized state. Components that are in this state are enumerated and configured by the PCI Express Hierarchy enumeration process. Following the completion of the enumeration and configuration process the function enters the D0 active state, the fully operational state for a PCI Express function. A function enters the D0 active state whenever any single or combination of the function's Memory Space Enable, I/O Space Enable, or Bus Master Enable bits have been enabled by system software.

6.2.2 Sleep States

6.2.2.1 Power Planes

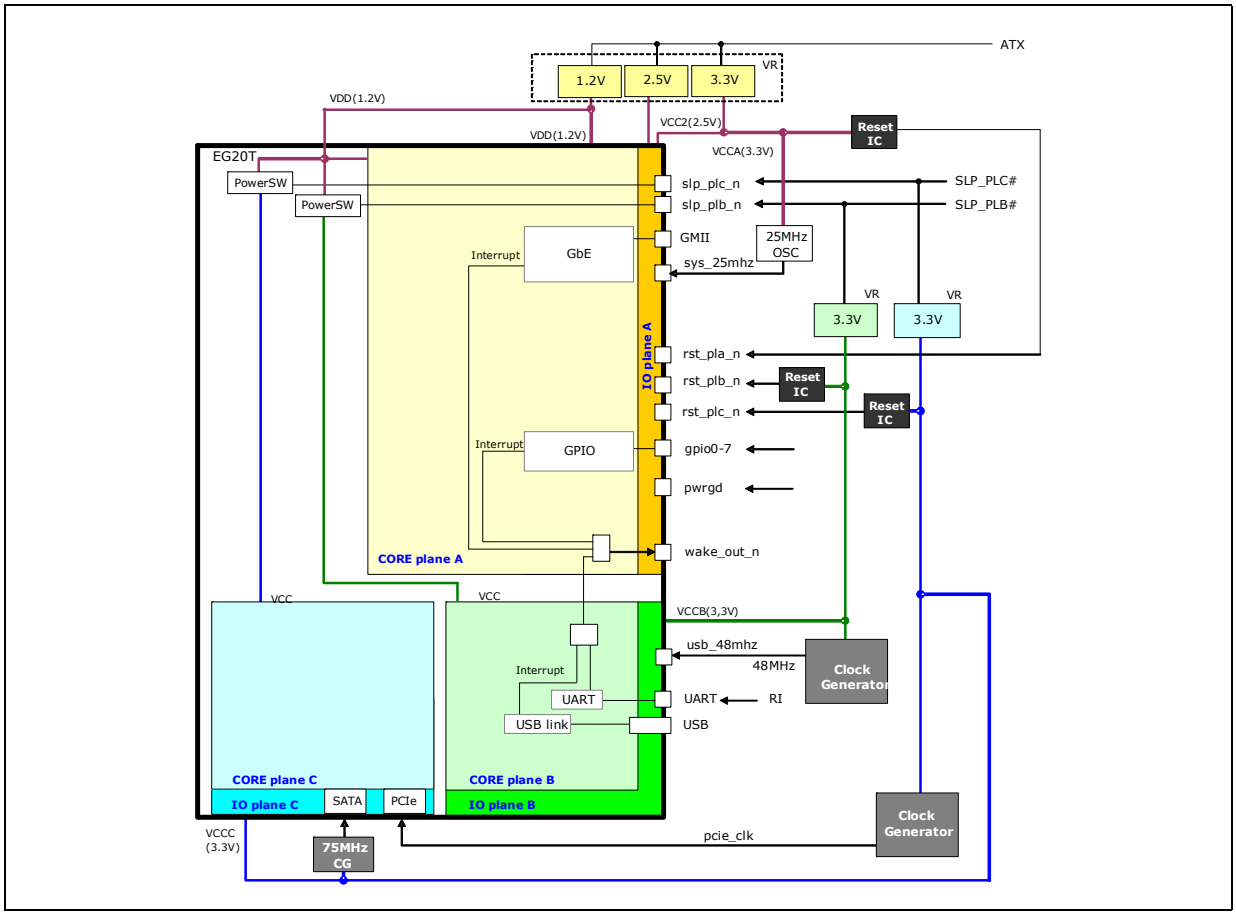
As shown in Table 102 and Figure 15, the Intel® PCH EG20T has three power planes, and Plane A and B of these three power planes can provide the wake-up function.

Table 102. Power Planes

Power Plane	Power Rail 6	Wake-up Function
Plane A	VCCA (I/O: 3.3V)	GPIO0-7 [2, 5]
		Gigabit Ethernet [2, 5]
	VCC2 (Gigabit Ether: 2.5V)	
	VDI0 (PLL0: 1.2V)	
	VDI1 (PLL1: 1.2V)	
	VDI2 (PLL2: 1.2V)	
	VDD (CORE 1.2V)	
Plane B	VCCB (I/O: 3.3V)	UART [3, 4, 5] USB Host [3, 5]
	AVDB* (USB: 3.3V)	
	AVDF1* (USB: 3.3V)	
	AVDF2* (USB: 1.2V)	
	AVDP* (USB PLL: 1.2V)	
	VDD (CORE 1.2V) [1]	
Plane C	VDN* (PCIe/SATA: 1.2V)	
	VDU* (PCIe/SATA: 1.2V)	
	VDP* (PCIe/SATA: 3.3V)	
	VCCC (I/O: 3.3V)	
	VDD (CORE 1.2V) [1]	

Notes:
1. Controlled with internal power switch
2. Wake up from S5/S4/S3
3. Wake up from S3
4. UART0 only
5. 25MHz clock input required.
6. For the current value of each power supply, refer to the Electrical Characteristics chapter.

Figure 15. Power Planes Concept Diagram (Example)



Each of power planes is powered ON/OFF according to the state of ACPI 3.0 Sleep State S and the use condition of wake-up function. Power ON/OFF condition and wake-up function are shown in Table 103.

Table 103. Power ON/OFF Condition and Wake-up Function

		When Wake-up Function is Used			When Wake-up Function is Not Used		
S State		**S0**	**S3**	**S4/S5**	**S0**	**S3**	**S4/S5**
Power ON/OFF Condition	**Plane A**	ON	ON	ON	ON	OFF	OFF
	Plane B	ON	ON	OFF	ON	OFF	OFF
	Plane C	ON	OFF	OFF	ON	OFF	OFF
Wake-up Function		-	GPIO0-7 Gigabit Ethernet UART0 USB Host	GPIO0-7 Gigabit Ethernet	-	-	-

6.2.2.2 Power Sequence with Wake-up Function

When Wake-up function is used, the power-on sequence for the power planes is clearly decided by the order of power-on, which always assumes Plane A -> Plane B -> Plane C.

Figure 16 and Figure 17 show power-on/off sequence of the power supply and the signals that relate to the three power planes.

Figure 16 and Figure 17 only show logical operation. For detailed timing requirements, refer to the Chapter 20.0, "Electrical Characteristics".

Figure 16. Power-on Sequence

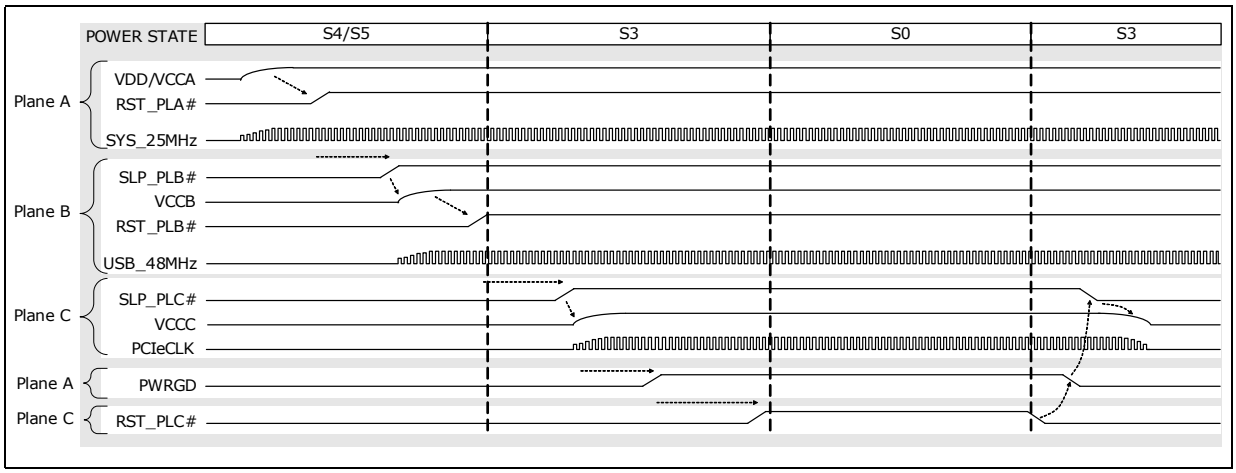
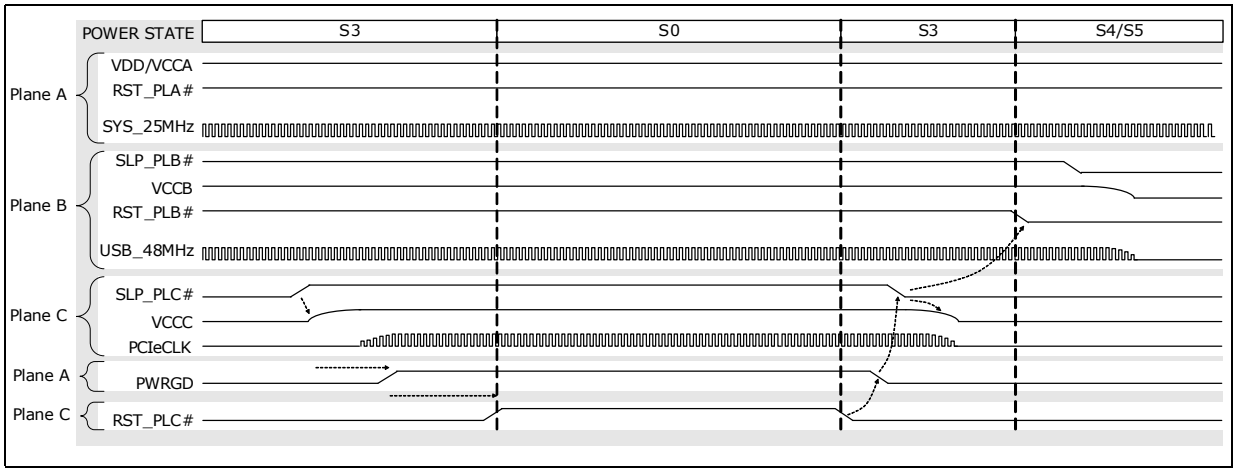


Figure 17. Power-off Sequence



6.2.2.3 Power Sequence with no Wake-up Function

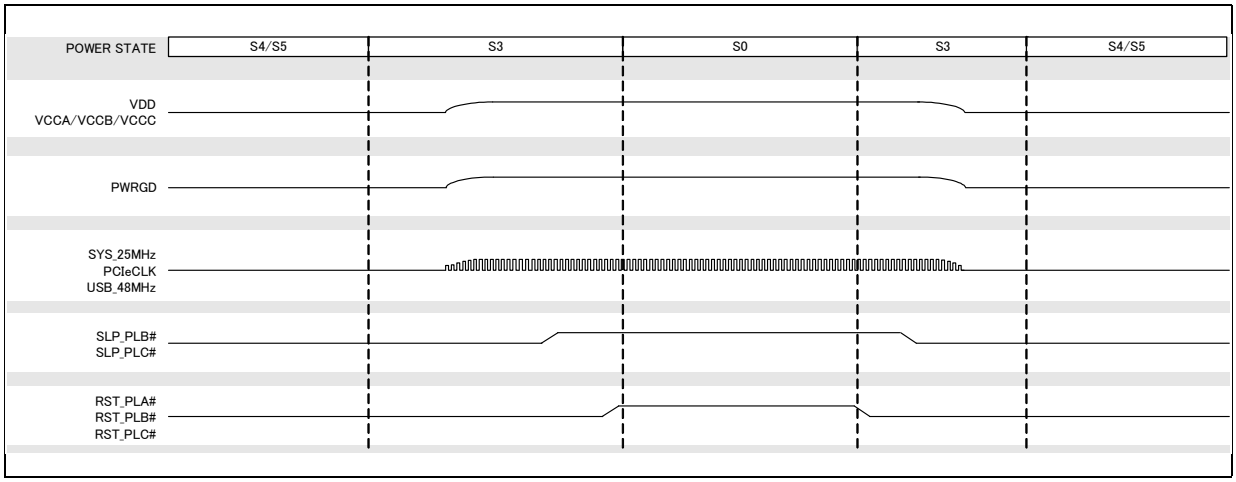
When Wake-up function is not used, each of the power planes has the same power-on sequence. The following differs compared with the case where Wake-up is used.

- PWRGD signal can be connected to VCC directly.
- RST_PLA#, RST_PLB# and RST_PLC# signals can be controlled as the same signal.
- SLP_PLB# and SLP_PLC# signals can be controlled as the same signals.

Figure 18 shows power-on/off sequence of the power supply and the signals that relate to the three power planes.

Figure 18 only shows logical operation. For detailed timing requirements, refer to Chapter 20.0, "Electrical Characteristics".

Figure 18. Power-on/off Sequence



6.2.2.4 Wake-Up Event

The wake-up event of each function is as follows:

1. Gigabit Ethernet MAC - Each interrupt of Gigabit Ethernet, such as Magic Packet with unique MAC address, can be a wake-up event.
2. GPIO - Each interrupt of GPIO0-7 can be a wake-up event.
3. USB Host - Each interrupt of USB Host can be a wake-up event.
4. UART0 (8-line only) - Each interrupt of UART, such as RI interrupt, can be a wake-up event.

A detailed content of the registers related to the interrupts are explained in the respective chapter for each function.

6.2.2.5 Hardware and Software Operation

The applicable functions are:

- Gigabit Ethernet MAC
- GPIO0-7
- USB Host
- UART0

The outline of flow from the occurrence of an event to the system startup is as follows:

1. PME bit of PMCSR register of each function is set to Enable (Software).
2. Wake-up event occurs in the system sleep state.
3. Gigabit Ethernet MAC /GPIO/USB host/UART0 generates interrupt signal (Hardware).
4. PME_STATUS bit is set (Hardware).
5. Asserting of internal wake-up signal occurs (Hardware).
6. Asserting of WAKE_OUT# signal occurs.

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7.0 SATA

7.1 Overview

The Serial Advanced Technology Attachment (SATA) Controller, implements the SATA storage interface for physical storage devices.

The features of the SATA Controller are as follows:

- Supports SATA 1.5-Gbps Generation 1 and 3-Gbps Generation 2 speeds
- Supports 2 ports
- Compliant with Serial ATA Specification 2.6, and Advanced Host Controller Interface (AHCI) Revision 1.1 specifications
- Supports power management features including automatic Partial to Slumber transition
- Internal DMA engine per port
- Supports hardware-assisted Native Command Queuing for up to 32 entries
- Supports Port Multiplier with command-based switching
- Supports Option ROM

7.2 Register Address Map

7.2.1 PCI Configuration Registers

Table 104. PCI Configuration Registers (Sheet 1 of 2)

Offset	Name	Symbol	Access	Initial Value
00h-01h	Vendor Identification Register	VID	RO	8086h
02h-03h	Device Identification Register	DID	RO	880Bh
04h-05h	PCI Command Register	PCICMD	RO, RW	0000h
06h-07h	PCI Status Register	PCISTS	RO, RWC	0010h
08h	Revision Identification Register	RID	RO	01h (A2) 02h (A3)
09h-0Bh	Class Code Register	CC	RO	010601h
0Dh	Master Latency Timer Register	MLT	RO	00h
0Eh	Header Type Register	HEADTYP	RO	00h
20h-23h	I/O Base Address Register	IO_BASE	RW, RO	00000001h
24h-27h	MEM Base Address Register	MEM_BASE	RW, RO	00000000h
2Ch-2Dh	Subsystem Vendor ID Register	SSVID	RWO	0000h
2Eh-2Fh	Subsystem ID Register	SSID	RWO	0000h
30h-33h	Extended ROM Base Address Register	ROM_BASE	RW, RO	0000h
34h	Capabilities Pointer Register	CAP_PTR	RO	40h
3Ch	Interrupt Line Register	INT_LN	RW	FFh
3Dh	Interrupt Pin Register	INT_PN	RO	04h
40h	MSI Capability ID Register	MSI_CAP	RO	05h

Table 104. PCI Configuration Registers (Sheet 2 of 2)

Offset	Name	Symbol	Access	Initial Value
41h	MSI Next Item Pointer Register	MSI_NPR	RO	50h
42h-43h	MSI Message Control Register	MSI_MCR	RO, RW	0000h
44h-47h	MSI Message Address Register	MSI_MAR	RO, RW	00000000h
48h-49h	MSI Message Data Register	MSI_MD	RW	0000h
50h	PCI Power Management Capability ID Register	PM_CAPID	RO	01h
51h	Next Item Pointer Register	PM_NPR	RO	60h
52h-53h	Power Management Capabilities Register	PM_CAP	RO	0002h
54h-55h	Power Management Control/Status Register	PWR_CNTL_STS	RO, RW RWC	0000h
60h	SATA Capability ID Register	SATA_CAPID	RO	12h
61h	Next Item Pointer Register	SATA_NPR	RO	00h
62h	Major Revision number and Minor Revision number of the SATA Capability Pointer Register	SATA_ MAJREV_MINREV	RO	10h
64h-66h	BAR Offset and BAR Location Register	SATA_BAROFST_ BARLOC	RO	0044h

7.2.2 I/O Registers

There are two registers at PCI I/O space, one is the AHCI Index Register and the other is the AHCI Index Data Register.

Table 105. PCI I/O Register Address Map

Offset Address	Register name	Symbol	Access	Reset
10h	AHCI Index Register	AIR	RW, RO	00000000h
14h	AHCI Index Data Register	AIDR	RW	xxxxxxxxh

7.2.3 Memory-Mapped I/O Registers (BAR: MEM_BASE)

This section provides high-level summary of the Generic and Port control register maps.

Table 106 shows the Generic Host Register Map.

Table 106. Generic Host Register Map (Sheet 1 of 2)

Offset Address	Register Name	Symbol	Access	Reset
00h	HBA Capabilities Register	CAP	RO	See detailed description
04h	Global HBA Control Register	GHC	See detailed description	80000000h
08h	Interrupt Status Register	IS	RWC	00000000h
0Ch	Ports Implemented Register	PI	RO	See detailed description
10h	AHCI Version Register	VS	RO	00010100h

Table 106. Generic Host Register Map (Sheet 2 of 2)

14h	Command Completion Coalescing Control	CCC_CTL	RW, RO	See detailed description
18h	Command Completion Coalescing Ports	CCC_PORTS	RW	00000000h
1Ch - 23h	Reserved		RO	0
24h	Reserved		RO	00000004h
28h - 9Fh	Reserved		RO	0
A0h	BIST Activate FIS Register	BISTAFR	RO	00000000h
A4h	BIST Control Register	BISTCR	RW, WO, RO	00000700h
A8h	BIST FIS Count Register	BISTFCTR	RO	00000000h
ACh	BIST Status Register	BISTSR	RO	00000000h
B0h	BIST DWORD Error Count Register	BISTDECR	RO	00000000h
B4h - BBh	Reserved		RO	0
BCh	OOB Register	OOBR	RW	00000000h
C0h - DFh	Reserved		RO	0
E0h	Timer 1 -ms Register	TIMER1 MS	RW, RO	00000000h
E4h - E7h	Reserved		RO	0
E8h	Global Parameter 1 Register	GPARAM1 R	RO	98000000h
ECh	Global Parameter 2 Register	GPARAM2R	RO	0000004Bh
F0h	Port Parameter Register	PPARAMR	RO	00000292h
F4h	Test Register	TESTR	RW	00000000h
F8h	Version Register	VERSIONR	RO	3133312Ah
FCh	ID Register	IDR	RO	00000000h

Table 107. Port Host Register Map (Sheet 1 of 2)

Offset Address	Register Name	Symbol	Access	Reset
100h	Port0 Command List Base Address Register	P0CLB	RW,RO	00000000h
104h	Port0 Command List Base Address Upper 32-Bits Register	P0CLBU	RO	00000000h
108h	Port0 FIS Base Address Register	P0FB	RW,RO	00000000h
10Ch	Port0 FIS Base Address Upper 32-Bits Register	P0FBU	RO	00000000h
110h	Port0 Interrupt Status Register	P0IS	RO,RWC	00000000h
114h	Port0 Interrupt Enable Register	P0IE	RW,RO	00000000h
118h	Port0 Command Register	P0CMD	RW,RO	Refer to Section 7.3.3.27
120h	Port0 Task File Data Register	P0TFD	RO	0000007Fh
124h	Port0 Signature Register	P0SIG	RO	FFFFFFFFh
128h	Port0 Serial ATA Status {SStatus} Register	P0SSTS	RO	00000000h
12Ch	Port0 Serial ATA Control {SControl} Register	P0SCTL	RW,RO	00000000h
130h	Port0 Serial ATA Error {SError} Register	P0SERR	RO,RWC	00000000h
134h	Port0 Serial ATA Active {SActive} Register	P0SACT	RO,RWS	00000000h
138h	Port0 Command Issue Register	P0CI	RO,RWS	00000000h

Table 107. Port Host Register Map (Sheet 2 of 2)

Offset Address	Register Name	Symbol	Access	Reset
13Ch	Port0 Serial ATA Notification Register	P0SNTF	RO,RWC	00000000h
170h	Port0 DMA Control Register	P0DMACR	RW,RO	00000046h
178h	Port0 PHY Control Register	P0PHYCR	RW,RO	00000000h
17Ch	Port0 PHY Status Register	P0PHYSR	RO	00000000h
180h	Port1 Command List Base Address Register	P1CLB	RW,RO	00000000h
184h	Port1 Command List Base Address Upper 32-Bits Register	P1CLBU	RO	00000000h
188h	Port1 FIS Base Address Register	P1FB	RW,RO	00000000h
18Ch	Port1 FIS Base Address Upper 32-Bits Register	P1FBU	RO	00000000h
190h	Port1 Interrupt Status Register	P1IS	RO,RWC	00000000h
194h	Port1 Interrupt Enable Register	P1IE	RW,RO	00000000h
198h	Port1 Command Register	P1CMD	RW,RO	Refer to Section 7.3.3.27
1A0h	Port1 Task File Data Register	P1TFD	RO	0000007Fh
1A4h	Port1 Signature Register	P1SIG	RO	FFFFFFFFh
1A8h	Port1 Serial ATA Status {SStatus} Register	P1SSTS	RO	00000000h
1ACh	Port1 Serial ATA Control {SControl} Register	P1SCTL	RW,RO	00000000h
1B0h	Port1 Serial ATA Error {SError} Register	P1SERR	RO,RWC	00000000h
1B4h	Port1 Serial ATA Active {SActive} Register	P1SACT	RO,RWS	00000000h
1B8h	Port1 Command Issue Register	P1CI	RO,RWS	00000000h
1BCh	Port1 Serial ATA Notification Register	P1SNTF	RO,RWC	00000000h
1F0h	Port1 DMA Control Register	P1DMACR	RW,RO	00000046h
1F8h	Port1 PHY Control Register	P1PHYCR	RW,RO	00000000h
1FCh	Port1 PHY Status Register	P1PHYSR	RO	00000000h
200h-3F7h	Reserved		RO	0
3F8h	Test Register 2	TESTR2	RW	00000000h
3FCh	PHY SOFT RESET Register (PSRST)	PSRST	RW	00000000h

7.3 Registers

7.3.1 PCI Configuration Registers

7.3.1.1 VID— Vendor Identification Register

Table 108. 00h: VID- Vendor Identification Register

Size: 16-bit			**Default:** 8086h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 00h **Offset End:** 01h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :00	8086h	RO	VID	**Vendor ID (VID):** This is a 16-bit value assigned to Intel.	

7.3.1.2 DID— Device Identification Register

Table 109. 02h: DID— Device Identification Register

Size: 16-bit			**Default:** 880Bh	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 02h **Offset End:** 03h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :00	880Bh	RO	DID	**Device ID (DID):** This is a 16-bit value assigned to the SATA CONTROLLER.

7.3.1.3 PCICMD— PCI Command Register

Table 110. 04h: PCICMD— PCI Command Register

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 04h **Offset End:** 05h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :11	0	RO		**Reserved**[1]
10	0	RW	ITRPDS	Interrupt Disable: 0 = Enable. The function is able to generate its interrupt to the interrupt controller. 1 = Disable. The function is not capable of generating interrupts. Interrupt enable does not affect PCISTS.IS.
09	0	RO		**Reserved**[1]
08	0	RW	SERR	**SERR# enable:** Send Error message (FATAL/NON_FATAL) Enable 0 = Disable 1 = Enable Sending
07	0	RO		**Reserved**[1]
06	0	RO	PER	Parity Error Response This bit is hardwired 0.
05 :03	0h	RO		**Reserved**[1]
02	0	RW	BME	**Bus Master Enable (BME):** 0 = Disable 1 = Enable. The Intel® PCH EG20T can act as a master on the PCI bus for SATA transfers.
01	0	RW	MEMSE	**Memory Space Enable (MEMSE):** This bit controls access to the Memory space registers. 0 = Disable 1 = Enable accesses to the Memory. The Base Address register for SATA CONTROLLER should be programmed before this bit is set.
00	0	RW	IOSE	I**/O Space Enable (IOSE):** This bit controls access to the I/O space registers. 0 = Disable 1 = Enable accesses to the SATA CONTROLLER I/O registers. The Base Address register for SATA CONTROLLER should be programmed before this bit is set.

Notes:
1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

7.3.1.4 PCISTS—PCI Status Register

Table 111. 06h: PCISTS—PCI Status Register

Size: 16-bit			Default: 0010h		Power Well: Core
Access	PCI Configuration		B:D:F D6:F0		Offset Start: 06h Offset End: 07h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15	0	RO		**Reserved**[1]	
14	0	RWC	SSE	**Signaled System Error:** This bit is set when this device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition. 0 = No send error message 1 = Send error message	
13	0	RWC	RMA	**Received Master Abort:** Primary received Unsupported Request Completion Status.	
12	0	RWC	RTA	**Received Target Abort:** Primary received Abort Completion Status	
11	0	RWC	STA	**Signaled Target Abort:** Primary transmitted Abort Completion Status	
10 :05	00h	RO		**Reserved**[1]	
04	1	RO	CPL	**Capabilities List:** This bit indicates the presence a capabilities list.	
03	0	RO	ITRPSTS	**Interrupt Status:** At the input of the enable/disable logic, this bit reflects the status of the interrupt of this function. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.	
02 :00	0	RO		**Reserved**[1]	

Notes:
1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

7.3.1.5 RID— Revision Identification Register

Table 112. 08h: RID— Revision Identification Register

Size: 8-bit			Default: 01h (A2) 02h (A3)		Power Well: Core
Access	PCI Configuration		B:D:F D6:F0		Offset Start: 08h Offset End: 08h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	01h (A2) 02h (A3)	RO		**Revision ID:** Refer to the Intel® Platform Controller Hub EG20T Specification Update for the value of the Revision ID Register.	

7.3.1.6 CC— Class Code Register

Table 113. 09h: CC— Class Code Register

Size: 24-bit			**Default:** 010601h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 09h **Offset End:** 0Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
23 :16	01h	RO	BCC	**Base Class Code (BCC):** 01h = Mass storage controller	
15 :08	06h	RO	SCC	**Sub Class Code (SCC):** 06h = SATA Controller	
07 :00	01h	RO	PI	**Programming Interface (PI):** 01h = AHCI 1.0 interface	

7.3.1.7 MLT— Master Latency Timer Register

Table 114. 0Dh: MLT— Master Latency Timer Register

Size: 8-bit			**Default:** 00h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 0Dh **Offset End:** 0Dh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	00h	RO	MLT	**Master Latency Timer (MLT):** Hardwired to 00h. The SATA CONTROLLER is implemented internally in the Intel® PCH EG20T and not arbitrated as a PCI device.	

7.3.1.8 HEADTYP— Header Type Register

Table 115. 0Eh: HEADTYP— Header Type Register

Size: 8-bit			**Default:** 00h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 0Eh **Offset End:** 0Eh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07	0b	RO	MFD	**Multi-Function Device:** 0 = Single-function device.	
06 :00	00h	RO	CONFIGLAYOUT	**Configuration Layout:** It indicates the standard PCI configuration layout.	

7.3.1.9 IO_BASE— I/O Base Address Register

Table 116. 20h: IO_BASE— I/O Base Address Register

Size: 32-bit			**Default:** 00000001h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 20h **Offset End:** 23h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :05	0000000h	RW	BA	**Base Address:** Bits 31:5 claim a 32-byte address space	
04 :01	0000b	RO		**Reserved**	
00	1b	RO	RTE	**Resource Type Indicator (RTE):** Hardwired to 1 to indicate that the base address field in this register maps to I/O space.	

7.3.1.10 MEM_BASE— MEM Base Address Register

Table 117. 24h: MEM_BASE— MEM Base Address Register

Size: 32-bit			**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 24h **Offset End:** 27h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :10	000000h	RW	BA	**Base Address:** Bits 31:10 claim a 1024-byte address space	
09 :04	00h	RO		**Reserved**[1]	
03	0b	RO	PREFETCHABLE	**Prefetchable:** Hardwired to 0 indicating that this range should not be prefetched.	
02 :01	00b	RO	TYPE	**Type:** Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.	
00	0b	RO	RTE	**Resource Type Indicator (RTE):** Hardwired to 0 indicating that the base address field in this register maps to memory space.	

Notes:
1. Reserved: This bit is reserved for future expansion. Only "0" is accepted as the write data to the reserved bit. When "1" is written, the operation is not guaranteed.

7.3.1.11 SSVID— Subsystem Vendor ID Register

Table 118. 2Ch: SSVID— Subsystem Vendor ID Register

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 2Ch **Offset End:** 2Dh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :00	0000h	RWO	SSVID	**Subsystem Vendor ID (SSVID):** BIOS writes this bit. No hardware action taken on this value.	

7.3.1.12 SSID— Subsystem ID Register

Table 119. 2Eh: SSID— Subsystem ID Register

Size: 16-bit		Default: 0000h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		Offset Start: 2Eh Offset End: 2Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :00	0000h	RWO	SSID	**Subsystem ID (SSID):** BIOS writes this bit. No hardware action taken on this value.

7.3.1.13 ROM_BASE— Extended ROM Base Address Register

Table 120. 30h: ROM_BASE— Extended ROM Base Address Register

Size: 32-bit		Default: 0000h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		Offset Start: 30h Offset End: 33h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :17	00000h	RW	BA	**Base Address:** Bits 31:16 claim a 64K byte address space
16 :01	000h	RO		**Reserved**
00	0h	RW	ADE	**Address Decode Enable (ADE):** If software sets this bit to 1, Extended ROM maps to Memory space.

7.3.1.14 CAP_PTR— Capabilities Pointer Register

Table 121. 34h: CAP_PTR— Capabilities Pointer Register

Size: 8-bit		Default: 40h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		Offset Start: 34h Offset End: 34h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	40h	RO	PTR	**Pointer (PTR):** This register points to the starting offset of the SATA capabilities ranges.

7.3.1.15 INT_LN— Interrupt Line Register

Table 122. 3Ch: INT_LN— Interrupt Line Register

Size: 8-bit		Default: FFh		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		Offset Start: 3Ch Offset End: 3Ch
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	FFh	RW	INT_LN	**Interrupt Line (INT_LN):** The Intel® PCH EG20T does not use this data. It is used to communicate to the software the interrupt line to which the interrupt pin is connected to.

7.3.1.16 INT_PN— Interrupt Pin Register

Table 123. 3Dh: INT_PN— Interrupt Pin Register

Size: 8-bit			**Default:** 04h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D6:F0		**Offset Start:** 3Dh **Offset End:** 3Dh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	04h	RO	INT_PN	**Interrupt Pin:** Hardwired to 04h indicating that this function corresponds to INTD#.	

7.3.1.17 MSI_CAPID—MSI Capability ID Register

Table 124. 40h: MSI_CAPID—MSI Capability ID Register

Size: 8-bit			**Default:** 05h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D6:F0		**Offset Start:** 40h **Offset End:** 40h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	05h	RO	MSI_CAPID	**MSI Capability ID**: A value of 05h indicates that this bit identifies the MSI register set.	

7.3.1.18 MSI_NPR—MSI Next Item Pointer Register

Table 125. 41h: MSI_NPR—MSI Next Item Pointer Register

Size: 8-bit			**Default:** 50h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D6:F0		**Offset Start:** 41h **Offset End:** 41h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	50h	RO	NEXT_PV	**Next Item Pointer Value:** Hardwired to 50h to indicate that this is power management registers capabilities list.	

7.3.1.19 MSI_MCR—MSI Message Control Register

Table 126. 42h: MSI_MCR—MSI Message Control Register (Sheet 1 of 2)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access		PCI Configuration	**B:D:F** D6:F0		**Offset Start:** 42h **Offset End:** 43h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :08	00h	RO		Reserved	
07	0b	RO	C64	**64-Bit Address Capable** 0 = 32-bit capable only	

Table 126. 42h: MSI_MCR—MSI Message Control Register (Sheet 2 of 2)

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 42h **Offset End:** 43h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
06 :04	000b	RW	MME	**Multiple Message Enable (MME):** Indicates the actual number of messages allocated to the device	
03 :01	000b	RO	MMC	**Multiple Message Capable (MMC):** Indicates that the SATA controller supports 1 interrupt message. This field is encoded as follows; 000b = 1 Message Requested 001b = 2 Messages Requested 010b = 4 Messages Requested 011b = 8 Messages Requested 100b = 16 Messages Requested 101b = 32 Messages Requested 110b = Reserved 111b = Reserved	
00	0b	RW	MSIE	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.	

7.3.1.20 MSI_MAR—MSI Message Address Register

Table 127. 44h: MSI_MAR—MSI Message Address Register

Size: 32-bit			**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 44h **Offset End:** 47h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :02	0000000h	RW	ADDR	**Address (ADDR):** Lower 32 bits of the system specified message address, always DWord aligned.	
01 :00	00b	RO		Reserved	

7.3.1.21 MSI_MD—MSI Message Data Register

Table 128. 48h: MSI_MD—MSI Message Data Register

Size: 16-bit			**Default:** 0000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 48h **Offset End:** 49h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
15 :00	0000h	RW	DATA	**Data (DATA):** When MSI is enabled; the system software programs this 16-bit field.	

7.3.1.22 PM_CAPID—PCI Power Management Capability ID Register

Table 129. 50h: PM_CAPID—PCI Power Management Capability ID Register

Size: 8-bit			**Default:** 01h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 50h **Offset End:** 50h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	01h	RO	PMC_ID	**Power Management Capability ID:** A value of 01h indicates that this is a PCI Power Management capabilities field.

7.3.1.23 PM_NPR—PM Next Item Pointer Register

Table 130. 51h: PM_NPR—PM Next Item Pointer Register

Size: 8-bit			**Default:** 60h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 51h **Offset End:** 51h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	60h	RO	NEXT_P1V	**Next Item Pointer Value:** Value of 60h indicates that this is a SATA registers capabilities list.

7.3.1.24 PM_CAP—Power Management Capabilities Register

Table 131. 52h: PM_CAP—Power Management Capabilities Register

Size: 16-bit			**Default:** 0002h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 52h **Offset End:** 53h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15 :11	00000b	RO	PME_SUP	**PME Support (PME_SUP):** This 5-bit field indicates the power states in which the Function may assert PME#. For all states, the SATA CONTROLLER is not capable of generating PME#. Software should never need to modify this field
10	0b	RO	D2_SUP	**D2 Support (D2_SUP).** 0 = D2 State is not supported
09	0b	RO	D1_SUP	**D1 Support (D1_SUP).** 0 = D1 State is not supported
08 :06	000b	RO	AUX_CUR	**Auxiliary Current (AUX_CUR):** This function does not support the D3cold state.
05	0b	RO	DSI	**Device Specific Initialization (DSI):** The Intel® PCH EG20T reports 0, indicating that no device-specific initialization is required.
04	0b	RO		Reserved
03	0b	RO	PME_CLK	**PME Clock (PME_CLK):** The Intel® PCH EG20T reports 0, indicating that no PCI clock is required to generate PME#.
02 :00	010b	RO	VER	**Version (VER):** The Intel® PCH EG20T reports 010b, indicating that it complies with the PCI Power Management Specification Revision 1.1.

7.3.1.25 PWR_CNTL_STS—Power Management Control/Status Register

Table 132. 54h: PWR_CNTL_STS—Power Management Control/Status Register

Size: 16-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 54h **Offset End:** 55h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
15	0b	RWC	STS	**PME Status (STS):** 0 = Writing a 1 to this bit will clear it and cause the internal PME to de-assert (if enabled). 1 = This bit is set when the SATA CONTROLLER would normally assert the PME# signal independent of the state of the PME_En bit. ***Note:*** Each time the operating system is loaded it must clear this bit explicitly.
14 :13	00b	RO	DSCA	**Data Scale (DSCA):** Hardwired to 00b indicating it does not support the associated Data register.
12 :09	0h	RO	DSEL	**Data Select (DSEL**): Hardwired to 0000b indicating it does not support the associated Data register.
08	0b	RW	EN	**PME Enable (EN):** 0 = Disable. 1 = Enable. Enables SATA CONTROLLER to generate an internal PME signal when PME_Status is 1. ***Note:*** The operating system must explicitly clear this bit each time it is initially loaded.
07 :02	00h	RO		**Reserved**
01 :00	00b	RW	POWERSTATE	**Power State:** This 2-bit field is used both to determine the current power state of SATA CONTROLLER function and to set a new power state. The definition of the field values are: 00b = D0 state 11b = D3hot state

7.3.1.26 SATA_CAPID—SATA Capability ID Register

Table 133. 60h: SATA_CAPID—SATA Capability ID Register

Size: 8-bit			**Default:** 0000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 60h **Offset End:** 60h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :00	12h	RO	CID	**Cap ID (CID):** Indicates that this pointer is a SATA Capability.

7.3.1.27 SATA_NPR—SATA Next Item Pointer Register

Table 134. 61h: SATA_NPR—SATA Next Item Pointer Register

Size: 8-bit			Default: 00h		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: 61h Offset End: 61h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	00h	RO	NEXT	**Next Capability (NEXT):** Indicates the location of the next capability item in the list. This can be other capability pointers or it can be the last item in the list.	

7.3.1.28 SATA_MAJREV_MINREV—Major Revision Number and Minor Revision Number of the SATA Capability Pointer Register

Table 135. 62h: SATA_MAJREV_MINREV—Major Revision Number and Minor Revision Number of the SATA Capability Pointer Register

Size: 8-bit			Default: 10h		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: 62h Offset End: 62h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :04	1h	RO	**MAJREV**	**Major Revision (MAJREV):** Major revision number of the SATA Capability Pointer implemented.	
03 :00	0h	RO	**MINREV**	**Minor Revision (MINREV):** Minor revision number of the SATA Capability Pointer implemented.	

7.3.1.29 SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register

Table 136. 64h: SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register (Sheet 1 of 2)

Size: 24-bit			Default: 0044h		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: 64h Offset End: 66h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
23 :04	004h	RO	BAROFST	**BAR Offset (BAROFST):** Indicates the offset into the BAR where the Index-Data Pair are located in DWord granularity. Possible values include: 000h = 0h offset 001h = 4h offset 002h = 8h offset 003h = Ch offset 004h = 10h offset … 3FFFh = FFFCh offset Maximum if Index-Data Pair is implemented in IO Space from 0-64 KB 3FFFFh = FFFFCh offset Maximum if Index-Data Pair is memory mapped in the 0 – (1MB – 4) range)	

Table 136. 64h: SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register (Sheet 2 of 2)

Size: 24-bit			**Default:** 0044h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 64h **Offset End:** 66h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
03 :00	8h	RO	BARLOC	**BAR Location (BARLOC):** Indicates the absolute PCI Configuration Register address of the BAR containing the Index-Data Pair in Dword granularity. Possible values are: 0100b = 10h (BAR0) 0101b = 14h (BAR1) 0110b = 18h (BAR2) 0111b = 1Ch (BAR3) 1000b = 20h (BAR4) 1001b = 24h (BAR5) 1111b = Index-Data Pair is implemented in Dwords directly following SATACR1 in the PCI configuration space. All other values are reserved.

7.3.2 I/O Registers

7.3.2.1 AHCI Index Register

Table 137. 10h: SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 10h **Offset End:** 12h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :11	00000h	RO		Reserved
10 :02	000h	RW	INDEX	**Index (INDEX)- RW:** This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
01 :00	00b	RO		Reserved

7.3.2.2 AHCI Index Data Register

Table 138. 14h: SATA_BAROFST_BARLOC—SATA BAR Offset and BAR Location Register

Size: 32-bit			Default: xxxxxxxxh		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: 14h Offset End: 17h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :00	xxxxxxxxh	RW	DATA	**Data (DATA)-** RW: This Data register is a "window" through which data is read or written to the AHCI memory mapped registers. A read or write to this Data register triggers a corresponding read or write to the memory mapped register pointed to by the Index register. The Index register must be set prior to any read or write to this Data register. A physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the "default" value is the same as the default value of the register pointed to by the Index register.	

7.3.3 Memory-Mapped I/O Registers (BAR: MEM_BASE)

7.3.3.1 HBA Capabilities Register

This register indicates basic capabilities of the SATA Controller to the software.

Table 139. 00h: HBA Capabilities Register (Sheet 1 of 2)

Size: 32-bit			Default: See table below		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: 00h Offset End: 03h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31	0b	RO	S64A	**Supports 64-bit Addressing** SATA Controller supports 64-bit addressable data structures by utilizing P#FBU and P#CLBU registers.	
30	1b	RO	SNCQ	**Supports Native Command Queuing** SATA Controller supports SATA native command queuing by handling DMA Setup FIS natively.	
29	1b	RO	SSNTF	**Supports SNotification Register** SATA Controller supports P#SNTF (SNotification) register and its associated functionality.	
28	0b	RO	SMPS	**Supports Mechanical Presence Switch** If the Mechanical Presence Switch is not implemented, this field is set as reserved.	
27	HwInit	RO	SSS	**Supports Staggered Spin-up** The system firmware/BIOS sets this bit to indicate platform support for staggered devices' spin-up. SATA Controller supports this feature through the P#CMD.SUD bit functionality.	
26	1b	RO	SALP	**Supports Aggressive Link Power Management** When there are no commands to process SATA Controller supports auto-generating (Port-initiated) Link Layer requests to the PARTIAL or SLUMBER power management states.	
25	1b	RO	SAL	**Supports Activity LED** SATA Controller supports activity indication using signal p#_act_led.	

Table 139. 00h: HBA Capabilities Register (Sheet 2 of 2)

Size: 32-bit			**Default:** See table below	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** 00h **Offset End:** 03h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
24	1b	RO	SCLO	**Supports Command List Override** SATA Controller supports the P#CMD.CLO bit functionality for Port Multiplier devices' enumeration.
23 :20	2h	RO	ISS	**Interface Speed Support** SATA Controller supports both Gen.1 and Gen.2 interface speeds.
19	0b	RO	SNZO	**Supports Non-Zero DMA Offsets** This feature is not supported.
18	1b	RO	SAM	**Supports AHCI Mode Only** SATA Controller supports AHCI mode only and does not support legacy task-file based register interface.
17	1b	RO	SPM	**Supports Port Multiplier** SATA Controller supports command-based switching Port Multiplier on any of its ports.
16	0b	RO	FBSS	**FIS-based Switching Supported** If FIS-based Switching is not implemented, this field is set as reserved.
15	1b	RO	PMD	**PIO Multiple DRQ Block** SATA Controller supports multiple DRQ block data transfers for the PIO command protocol.
14	1b	RO	SSC	**Slumber State Capable** SATA Controller supports transitions to the interface SLUMBER power management state.
13	1b	RO	PSC	**Partial State Capable** SATA Controller supports transitions to the interface PARTIAL power management state.
12 :08	1Fh	RO	NCS	**Number of Command Slots** SATA Controller supports 32 command slots per port.
07	1b	RO	CCCS	**Command Completion Coalescing Support** SATA Controller supports command completion coalescing.
06	0b	RO	EMS	**Enclosure Management Support** SATA Controller does not support enclosure management.
05	0b	RO	SXS	**Supports External SATA** This field is: 0 = Indicates that the SATA Controller has no ports that have a signal only connector, which is externally accessible. 1 = Indicates that the SATA Controller has one or more Ports that has a signal only connector (power is not part of that connector) that is externally accessible. When this bit is set to 1, the software can refer to the P#CMD.ESP bit to determine whether a specific Port has its signal connector externally accessible.
04 :00	00001b	RO	NP	**Number of Ports** 0's based value indicating the number of ports supported by the SATA Controller: The options for this field are: 1h: 2 Ports

7.3.3.2 Global HBA Control Register

This register controls various global actions of the SATA Controller.

Table 140. 04h: Global HBA Control Register

Size: 32-bit			Default: 80000000h	Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		Offset Start: 04h Offset End: 07h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31	1b	RO	AE	**AHCI Enable** This bit is always set since SATA Controller supports only AHCI mode as indicated by the CAP.SAM=1.
30 :03	0000000h	RO		Reserved
02	0b	RO	MRSM	**MSI Revert to Single Message** If MSI Revert to Single Message is not implemented, this field is set as reserved.
01	0b	RW	IE	**Interrupt Enable** This global bit enables interrupts from the SATA Controller. When cleared, all interrupt sources from all the ports are disabled (masked). When set, interrupts are enabled and any SATA Controller interrupt event causes intrq output assertion. This field is reset on Global reset (GHC.HR=1).
00	0b	WO	HR	**HBA Reset** When the software sets this bit, it causes an internal Global reset of the SATA Controller. When staggered spin-up is not supported, all state machines that relate to data transfers and queuing return to an idle state, and all the ports are re-initialized by sending COMRESET. When staggered spin-up is supported, the software must spin-up each port after this reset has completed. See "Global Reset" for details. The SATA Controller clears this bit when the reset action is done. A software write of 0 has no effect.

7.3.3.3 Interrupt Status Register

This register indicates the Ports within the SATA Controller that have an interrupt pending and requires service. This register is reset on Global reset (GHC.HR=1).

Table 141. 08h: Interrupt Status Register

Size: 32-bit			Default: 00000000h	Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		Offset Start: 08h Offset End: 0Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :03	0000000h	RO		Reserved
02	0b	RWC	IPS	**CCC_CTL.INT:** This bit is defined for the command completion coalescing interrupt defined by CCC_CTL.INT.
01 :00	00b	RWC	IPS	**Interrupt Pending Status** When set, this bit indicates that the corresponding port has an interrupt pending. The software can use this information to determine which ports require service after an interrupt. The bits of this field are set by the ports that have interrupt events pending in the P#IS bits and enabled by the P#IE. The software writes 1 to the bits that needs to be cleared.

7.3.3.4 Ports Implemented Register

Table 142. 0Ch: Ports Implemented Register

Size: 32-bit			Default: HwInit		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: 0Ch Offset End: 0Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :02	00000000h	RO		Reserved	
01 :00	HwInit	RO	PI	**Ports Implemented** This register is bit significant. 0 = The port is not available for the software to use. 1 = The corresponding port is available for the software to use. The maximum number of bits that can be set to 1 is CAP.NP+1. At least one bit must be set to 1. The contents of this register are relevant to the CCC_PORTS (Command Completion Coalescing Ports) register.	

7.3.3.5 AHCI Version Register

This register indicates the major and minor version of the AHCI specification that the SATA Controller implementation supports. The SATA Controller supports Version 1.20.

Note: The SATA Controller core currently complies fully with AHCI Version 1.10 and complies with AHCI version 1.20, except FIS-based switching. FIS-based switching is not currently supported.

Table 143. 10h: AHCI Version Register

Size: 32-bit			Default: 00010100h		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: 10h Offset End: 13h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :16	0001h	RO	MJR	**Major Version Number** Indicates that the major AHCI version is 1.0.	
15 :00	0100h	RO	MNR	**Minor Version Number** Indicates that the minor AHCI version is .20.	

7.3.3.6 Command Completion Coalescing Control

This register is used to configure the Command Completion Coalescing (CCC) feature for the SATA Controller core. It is reset on Global reset.

Table 144. 14h: Command Completion Coalescing Control

Size: 32-bit		Default: See below		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		Offset Start: 14h Offset End: 17h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :16	0001h	RW,RO	TV	**Time-out Value** This field specifies the CCC time-out value in 1ms intervals. The software loads this value prior to enabling CCC. The options for this field are: • RW when CCC_CTL.EN==0. • RO when CCC_CTL.EN==1. A time-out value of 0000h is reserved and should not be used.
15 :08	01h	RW,RO	CC	**Command Completions** This field specifies the number of command completions that are necessary to cause a CCC interrupt. The value 00h for this field disables CCC interrupts being generated based on the number of commands completed. In this case, CCC interrupts are only generated based on the timer. The software loads this value prior to enabling CCC: Field access is: • RW when CCC_CTL.EN==0 • RO when CCC_CTL.EN==1
07 :03	2h	RO	INT	**Interrupt** This field specifies the interrupt used by the CCC feature, using the number of ports configured for the core. When a CCC interrupt occurs, the field IS.IPS[INT] is set to 1.
04	0b	RW	PV	**Pattern Version** This bit is used to select either the short or long version of the SSOP, HTDP, LTDP, LFSCP, or COMP patterns. The options for this field are: 0 = Short pattern version 1 = Long pattern version
02 :01	00b	RO		Reserved
00	0b	RW	EN	**Enable** The options for this field are: 0 = CCC feature is disabled and no CCC interrupts are generated. 1 = CCC feature is enabled and CCC interrupts may be generated based on the time-out or command completion conditions. ***Note:*** When field CCC_CTL.EN=1, the software can not change the fields CCC_CTL.TV and CCC_CTL.CC.

7.3.3.7 Command Completion Coalescing Ports

This register specifies the ports that are coalesced as part of the CCC feature when CCC_CTL.EN==1. It is reset on Global reset.

Table 145. 18h: Command Completion Coalescing Ports

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**Offset Start:** 18h **Offset End:** 1Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RW	PRT	**Ports** This field is bit significant. Each bit corresponds to a particular port, where bit 0 corresponds to Port0. The options for this field are: 0 = the corresponding port is not part of the CCC feature. 1 = the corresponding port is part of the CCC feature. Bits set in this register must also have the corresponding bit set in the PI (Ports Implemented) register.

7.3.3.8 BIST Activate FIS Register

This register contains the pattern definition (bits [23:16] of the first DWORD) and data pattern (bits [7:0] of the second DWORD) fields of the received Built In Self Test (BIST) Activate FIS. These fields define the SATA Controller loopback responder mode requested by the device. It is updated every time a new BIST Activate FIS is received from the device. Reset on Global or Port reset.

Table 146. A0h: BIST Activate FIS Register (Sheet 1 of 2)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**Offset Start:** A0h **Offset End:** A3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :16	0000h	RO		Reserved
15 :08	00h	RO	NCP	**Non-Compliant Pattern** Least significant byte of the received BIST Activate FIS second DWORD (bits [7:0]). This value defines the required pattern for far-end transmit only mode (BISTAFR.PD=80h or A0h): F1h: Low transition density pattern (LTDP) B5h: High transition density pattern (HTDP) ABh: Low frequency spectral component pattern (LFSCP) 7Fh: Simultaneous switching outputs pattern (SSOP) 8Bh: Lone Bit pattern (LBP) 78h: Mid frequency test pattern (MFTP) 4Ah: High frequency test pattern (HFTP) 7Eh: Low frequency test pattern (LFTP) When none of these values is decoded, the simultaneous switching pattern is transmitted by default.

Table 146. A0h: BIST Activate FIS Register (Sheet 2 of 2)

Size: 32-bit			Default: 00000000h		Power Well: Core
Access	PCI Configuration		B:D:F D6:F0		Offset Start: A0h Offset End: A3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07 :00	00h	RO	PD	**Pattern Definition** Indicates the pattern definition field of the received BIST Activate FIS - bits [23:16] of the first DWORD. It is used to put the SATA Controller in one of the following BIST modes: 10h: Far-end retimed 08h: Far-end analog (when PHY supports this mode) 80h: Far-end transmit only A0h: Far-end transmit only with scrambler bypassed The device should not use other values, otherwise, the FIS is negatively acknowledged with R_ERRp. For far-end transmit only modes, BISTAFR.NCP field contains the required data pattern.	

7.3.3.9 BIST Control Register

This register is used in BIST initiator modes. The host software loads the register prior to sending BIST Activate FIS to the device (via TXBISTPD write). It is reset on a Global or Port reset.

Table 147. A4h: BIST Control Register (Sheet 1 of 3)

Size: 32-bit			Default: 00000700h		Power Well: Core
Access	PCI Configuration		B:D:F D6:F0		Offset Start: A4h Offset End: A7h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :21	000h	RO		Reserved	
20	0b	WO	FERLB	**Far-end Retimed Loopback** When set, this bit is used to put the SATA Controller Link into Far-end Retimed mode, without the BIST Activate FIS, regardless whether the device is connected or disconnected (Link in NOCOMM state). This field is one-shot type and reads returns 0.	
19	0b	RO		Reserved	
18	0b	WO	TXO	**Transmit Only** When the device is disconnected, this bit is used to initiate transmission of one of the non-compliant patterns defined by the BISTCR.PATTERN value.	
17	0b	WO	CNTCLR	**Counter Clear** This bit clears BIST error count registers. This field is one-shot type and reads returns 0. 1 = Clears BISTFCTR, BISTSR, and BISTDECR registers.	

Table 147. A4h: BIST Control Register (Sheet 2 of 3)

Size: 32-bit			**Default:** 00000700h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** A4h **Offset End:** A7h

Bit Range	Default	Access	Acronym	Description
16	0b	WO	NEALB	**Near-End Analog Loopback** This bit places the Port PHY into near-end analog loopback mode. This field is one-shot type and reads returns 0. 1 = Near-end analog loopback request. BISTCR.PATTERN field contains the appropriate pattern. This mode should be initiated either in the PARTIAL or SLUMBER power mode, or with the device disconnected from the Port PHY (Link NOCOMM state). BIST Activate FIS is not sent to the device in this mode.
15 :11	00000b	RO		Reserved
10 :08	7h	RW	LLC	**Link Layer Control** This field controls the Port Link Layer functions: scrambler, descrambler, and repeat primitive drop. Following are the different meanings for normal and BIST modes of operation: • Bit8—SCRAM The options for this field are: 0 = Scrambler disabled in normal mode, enabled in BIST mode 1 = Scrambler enabled in normal mode, disabled in BIST mode • Bit9—DESCRAM The options for this field are: 0 = Descrambler disabled in normal mode, enabled in BIST mode 1 = Descrambler enabled in normal mode, disabled in BIST mode • Bit10—RPD The options for this field are: 0 = Repeat primitive drop function disabled in normal mode, NA in BIST mode. 1 = 1: Repeat primitive drop function enabled in normal mode, NA in BIST mode. The port clears the SCRAM bit (enabled) when the port enters a responder far-end transmit BIST mode with scrambling enabled (BISTAFR.PD=80h). In normal mode, the Function's scrambler, descrambler, or RPD can be changed only during Port reset (P#SCTL.DET=1h)
07	0b	RO		Reserved
06	0b	RW	ERREN	**Error Enable** This bit is used to allow or filter (disable) PHY internal errors outside the FIS boundary, to set corresponding P#SERR bits. The options for this field are: 0 = Filter errors outside the FIS, allow errors inside the FIS 1 = Allow errors outside or inside the FIS
05	0b	RW	FLIP	**Flip Disparity** This bit is used to change disparity of the current test pattern to the opposite every time the software changes the state.
04	0b	RW	PV	**Pattern Version** This bit is used to select either the short or long version of the SSOP, HTDP, LTDP, LFSCP, and COMP patterns. The options for this field are: 0 = Short pattern version 1 = Long pattern version

Table 147. A4h: BIST Control Register (Sheet 3 of 3)

Size: 32-bit			Default: 00000700h		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: A4h Offset End: A7h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
03 :00	0h	RW	PATTERN	This field defines one of the following SATA compliant patterns for far-end retimed/ far-end analog/ near-end analog initiator modes, or non-compliant patterns for transmit-only responder mode when initiated by the software writing to the BISTCR.TXO bit: The options for this field are: 0000b: Simultaneous Switching Outputs Pattern (SSOP) 0001b: High Transition Density Pattern (HTDP) 0010b: Low Transition Density Pattern (LTDP) 0011b: Low frequency Spectral Component Pattern (LFSCP) 0100b: Composite pattern (COMP) 0101b: Lone Bit Pattern (LBP) 0110b: Mid Frequency Test Pattern (MFTP) 0111b: High Frequency Test Pattern (HFTP) 1000b: Low Frequency Test Pattern (LFTP) All other values are reserved and should not be used. If values other than the ones listed above are used, Composite pattern (COMP) is transmitted by default.	

7.3.3.10 BIST FIS Count Register

This register contains the received BIST FIS count in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST FIS is received. It is reset by Global reset, Port reset (COMRESET) or by setting the BISTCR.CNTCLR bit. This register does not roll over and freezes when the FFFF_FFFFh value is reached. It takes approximately 65 hours of continuous BIST operation to reach this value.

Table 148. A8h: BIST FIS Count Register

Size: 32-bit			Default: 00000000h		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: A8h Offset End: ABh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :00	00000000h	RO	RBFC	Received BIST FIS Count	

7.3.3.11 BIST Status Register

This register contains errors detected in the received BIST FIS in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST FIS is received. It is reset by Global reset, Port reset (COMRESET) or by setting the BISTCR.CNTCLR bit.

Table 149. ACh: BIST Status Register

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** ACh **Offset End:** AFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :24	00h	RO		Reserved
23 :16	00h	RO	BRSTERR	**Burst Error** This field contains the burst error count. It is accumulated each time a burst error condition is detected: DWORD error is detected in the received frame after 1.5 seconds (27,000 frames) passes since the previous burst error was detected. The BRSTERR value does not roll over and freezes at FFh. This field is updated when parameter BIST_MODE=DWORD.
15 :00	0000h	RO	FRAMERR	**Frame Error** This field contains the frame error count. It is accumulated (new value is added to the old value) each time a new BIST frame with a CRC error is received. The FRAMERR value does not roll over and freezes at FFFFh.

7.3.3.12 BIST DWORD Error Count Register

This register contains the number of DWORD errors detected in the received BIST frame in the loopback initiator far-end retimed, far-end analog and near-end analog modes. It is updated each time a new BIST frame is received. It is reset by Global reset, Port reset (COMRESET) or by setting the BISTCR.CNTCLR bit.

This register is updated only when the parameter BIST_MODE="DWORD".

Table 150. B0h: BIST DWORD Error Count Register

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** B0h **Offset End:** B3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RO	DWERR	**DWORD Error Count** This field contains the DWORD error count. It is accumulated (new value is added to the old value) each time a new BIST frame is received. The DWERR value does not roll over and freezes when it exceeds FFFFF000h.

7.3.3.13 OOB Register

This register is reserved.

Table 151. BCh: OOB Register

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** BCh **Offset End:** BFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RO		**Reserved.**

7.3.3.14 Timer 1 ms Register

This register is used to generate a 1 ms tick for the CCC logic, based on the bus clock frequency. The software must initialize this register with the required value after power-up before using the CCC feature. This register is reset to 100,000d (TIMV value for 100-MHz CLKH) on power-up and is not affected by Global reset.

Table 152. E0h: Timer 1 ms Register

Size: 32-bit			**Default:** 000186A0h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** E0h **Offset End:** E3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :20	000h	RO		Reserved	
19 :00	186A0h	RW/RO	TIMV	**1ms Timer Value** This field contains the following value for the internal timer to generate 1 ms tick: Fhclk x 1000 where Fhclk = BUS clock frequency in MHz The options for this field are: • RW when CCC_CTL.EN==0 • RO when CCC_CTL.EN==1.	

7.3.3.15 Global Parameter 1 Register

Table 153. E8h: Global Parameter 1 Register (Sheet 1 of 2)

Size: 32-bit			**Default:** 98000000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** E8h **Offset End:** EBh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31	1b	RO	ALIGN_M	**Rx Data Alignment** The valid values of the field are: 0 = Misaligned 1 = Aligned	
30	0b	RO	RX_BUFFER	**Rx Data Buffer** The valid values of the field are: 0 = Exclude 1 = Include	
29 :28	01b	RO	PHY_DATA	**PHY Data Width** The valid values of the field are: 0h = 1 1h = 2 2h = 4 Other values are reserved.	
27	1b	RO	PHY_RST	**PHY Reset Mode** The valid values of the field are: 0 = Low 1 = High	
26 :21	000000b	RO	PHY_CTRL	**PHY Control Width**	
20 :15	00h	RO	PHY_STAT	**PHY Status Width**	

Table 153. E8h: Global Parameter 1 Register (Sheet 2 of 2)

Size: 32-bit		**Default:** 98000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**Offset Start:** E8h **Offset End:** EBh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
14	0b	RO	LATCH_M	**LATCH_M** The valid values of the field are: 0 = Exclude 1 = Include
13	0b	RO	BIST_M	**BIST Loopback Checking Depth** The valid values of the field are: 0 = FIS 1 = DWORD
12	0b	RO	PHY_TYPE	**PHY Interface Type** The valid values of the field are: 0 = Configurable 1 = Synopsis
10	0b	RO	RETURN_ERR	**BUS Error Response** The valid values of the field are: 0 = False 1 = True
09 :08	00b	RO	BUS_ENDIAN	**Bus Endian** The valid values of the field are: 0 = Little 1 = Big 2 = Dynamic
07	0b	RO	S_HADDR	**BUS Slave Address Bus Width** The valid values of the field are: 0 = 32 bits 1 = 64 bits
06	0b	RO	M_HADDR	**BUS Master Address Bus Width** The valid values of the field are: 0 = 32 bits 1 = 64 bits
05 :00	00h	RO		Reserved

7.3.3.16 Global Parameter 2 Register

Table 154. ECh: Global Parameter 2 Register (Sheet 1 of 2)

Size: 32-bit		**Default:** 0000004Bh		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**Offset Start:** ECh **Offset End:** EFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :15	0000h	RO		Reserved
14	0b	RO	DEV_CP	**Cold Presence Detect** The valid values of the field are: 0 = Exclude 1 = Include

Table 154. ECh: Global Parameter 2 Register (Sheet 2 of 2)

Size: 32-bit			Default: 0000004Bh	Power Well: Core
Access	PCI Configuration		B:D:F D6:F0	Offset Start: ECh Offset End: EFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
13	0b	RO	DEV_MP	**Mechanical Presence Switch** The valid values of the field are: 0 = Exclude 1 = Include
12	0b	RO	ENCODE_M	**8b/10b Encoding/Decoding** The valid values of the field are: 0 = Exclude 1 = Include
11	0b	RO	RXOOB_CLK_M	**Rx OOB Clock Mode** The valid values of the field are: 0 = RxClock 1 = Separate
10	0b	RO	RX_OOB_M	**Rx OOB Mode** The valid values of the field are: 0 = Exclude 1 = Include
09	0b	RO	TX_OOB_M	**Tx OOB Mode** The valid values of the field are: 0 = Exclude 1 = Include
08 :00	04Bh	RO	RXOOB_CLK	**Rx OOB Clock Frequency**

7.3.3.17 Port Parameter Register

Table 155. F0h: Port Parameter Register (Sheet 1 of 2)

Size: 32-bit			Default: 00000292h	Power Well: Core
Access	PCI Configuration		B:D:F D6:F0	Offset Start: F0h Offset End: F3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :10	000000h	RO		Reserved
09	1b	RO	TX_MEM_M	**Tx FIFO Memory Read Port Type** The valid values of the field are: 0 = Async 1 = Sync
08	0b	RO	TX_MEM_S	**Tx FIFO Memory Type** The valid values of the field are: 0 = External 1 = Internal
07	1b	RO	RX_MEM_M	**Rx FIFO Memory Read Port Type** The valid values of the field are: 0 = Async 1 = Sync

Table 155. F0h: Port Parameter Register (Sheet 2 of 2)

Size: 32-bit			**Default:** 00000292h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** F0h **Offset End:** F3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
06	0b	RO	RA_MEM_S	**Rx FIFO Memory Type** The valid values of the field are: 0 = External 1 = Internal
05 :03	010b	RO	TXFIFO_DEPTH	**Tx FIFO Depth** The valid values of the field are: 0h = 32 1h = 64 2h = 128 3h = 256 4h = 512 5h = 1024 6h = 2048 7h = Reserved
02 :00	010b	RO	RXFIFO_DEPTH	**Rx FIFO Depth** The valid values of the field are: 0h = Reserved 1h = 64 2h = 128 3h = 256 4h = 512 5h = 1024 6h = 2048 7h = Reserved

7.3.3.18 Test Register

This register is used to put the SATA Controller slave interface into a test mode and to select a Port for BIST operation.

Table 156. F4h: Test Register (Sheet 1 of 2)

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** F4h **Offset End:** F7h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :19	0000h	RO		Reserved
18 :16	0h	RW	PSEL	**Port Select** The valid values of the field are: 0h = Port0 is selected 1h = Port1 is selected
15 :01	0000h	RO		Reserved

Table 156. F4h: Test Register (Sheet 2 of 2)

Size: 32-bit			Default: 00000000h		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: F4h Offset End: F7h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
00	0b	RW	TEST_IF	**TEST_IF: Test Interface** This bit is used to put the SATA Controller slave interface into the test mode: The options for this field are: 0 = Normal mode: The read back value of some registers is a function of the SATA Controller state and does not match the value written. 1 = Test mode: The read back value of the registers matches the value written. Normal operation is disabled. The following registers can be accessed in this mode: • GHC register IE bit • BISTAFR register NCP and PD bits become read-write • BISTCR register LLC, ERREN, FLIP, PV, PATTERN • BISTFCTR, BISTSR, BISTDECR become read-write • P#CLB/CLBU, P#FB/FBU registers • P#IS register RWC and UFS bits become read-write • P#IE register • P#CMD register ASP, ALPE, DLAE, ATAPI, PMA bits • P#TFD, P#SIG registers become read-write • P#SCTL register • P#SERR register RWC bits become read-write bits • P#SACT, P#CI, P#SNTF registers become read-write • P#DMACR register • P#PHYCR register • P#PHYSR register becomes read-write ***Notes:*** 1. Interrupt is asserted when any of the IS register bits is set after setting the corresponding P#IS and P#IE registers and GHC.IE=1. 2. CAP.SMPS/SSS, PI, P#CMD.ESP/CPD/MPSP/HPCP register bits are HwInit type and can not be used in Test mode. They are written once after power-on reset and become read-only. 3. Global SATA Controller reset must be issued (GHC.HR=1) after TEST_WHEN bit is cleared following the Test mode operation.	

7.3.3.19 Version Register

This 32-bit read-only register contains hard-coded hexadecimal SATA Controller component version value set by the AHSATA_VERSION_NUM parameter. The value represents an ASCII code of the version number.

Table 157. F8h: Version Register

Size: 32-bit			Default: See below		Power Well: Core
Access		PCI Configuration	B:D:F D6:F0		Offset Start: F8h Offset End: FBh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :00	3133312Ah	RO	VERSION	SATA Controller hard-coded hexadecimal version value.	

7.3.3.20 ID Register

This register contains a hard-coded hexadecimal SATA Controller identification value.

Table 158. FCh: ID Register

Size: 32-bit			**Default:** See below	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**Offset Start:** FCh **Offset End:** FFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RO	IDV	SATA Controller hard-coded hexadecimal identification value.

7.3.3.21 Port# Command List Base Address Register (P#CLB)

Table 159. 100h: Port# Command List Base Address Register (P#CLB)

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**#:** 0 / 1 **Offset Start:** 100h/180h **Offset End:** 103h/183h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :10	000000h	RW	CLB	**Command List Base Address** Indicates the 32-bit base physical address for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1 KB in length. This address must be 1 KB aligned as indicated by bits [9:0] being read only.
09 :00	000h	RO		Reserved

7.3.3.22 Port# Command List Base Address Upper 32-Bits Register (P#CLBU)

Table 160. 104h: Port# Command List Base Address Upper 32-Bits Register (P#CLBU)

Size: 32-bit			**Default:** 00000000h	**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0	**#:** 0 / 1 **Offset Start:** 104h/184h **Offset End:** 107h/187h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RO	CLBU	**Command List Base Address Upper** This location is reserved.

7.3.3.23 Port# FIS Base Address Register (P#FB)

Table 161. 108h: Port# FIS Base Address Register (P#FB)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 108h/188h **Offset End:** 10Bh/18Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :08	000000h	RW	FB	**FIS Base Address** Indicates the 32-bit base physical address for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256 byte aligned as indicated by bits [7:0], which are read only.
07 :00	00h	RO		Reserved

7.3.3.24 Port# FIS Base Address Upper 32-Bits Register (P#FBU)

Table 162. 110h: Port# FIS Base Address Upper 32-Bits Register (P#FBU)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 10Ch/10Fh **Offset End:** 18Ch/18Fh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RO	FBU	**FIS Base Address Upper** This location is reserved.

7.3.3.25 Port# Interrupt Status Register (P#IS)

This register is used to generate SATA interrupt when any of the bits are set. Bits in this register are set by some internal conditions and cleared by the software writing ones in the positions it wants to clear.

This register is reset on Global SATA reset.

Table 163. 110h: Port# Interrupt Status Register (P#IS) (Sheet 1 of 3)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 110h/190h **Offset End:** 113h/193h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31	0b	RO	CPDS	**Cold Port Detect Status** This field is reserved.
30	0b	RWC	TFES	**Task File Error Status** This bit is set whenever the P#TFD.STS register is updated by the device and the error bit (bit 0) is set.

Table 163. 110h: Port# Interrupt Status Register (P#IS) (Sheet 2 of 3)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 110h/190h **Offset End:** 113h/193h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
29	0b	RWC	HBFS	**Host Bus Fatal Error Status** This bit is set when the BUS Master of the SATA controller detects an ERROR response from the slave.
28	0b	RWC	HBDS	**Host Bus Data Error Status** This bit is always cleared to 0.

27	0b	RWC	IFS	**Interface Fatal Error Status**
				This bit is set when any of the following conditions is detected:
				• SYNC escape is received from the device during H2D Register or Data FIS transmission
				• One or more of the following errors are detected during Data FIS transfer:
				  • 10B to 8B Decode Error (P#SERR.DIAG_B)
				  • Protocol (P#SERR.ERR_P)
				  • CRC (P#SERR.DIAG_C)
				  • Handshake (P#SERR.DIAG_H)
				  • PHY Not Ready (P#SERR.ERR_C)
				  • Unknown FIS is received with good CRC, but the length exceeds 64 bytes
				  • PRD table byte count is zero
				Port DMA transitions to a fatal state until the software clears P#CMD.ST bit or resets the interface by way of Port or Global reset.

25	0b	RO		Reserved.
24	0b	RWC	OFS	**Overflow Status** This bit is set when command list overflow is detected during read or write operation, when the software builds command table that has fever total bytes than the transaction given to the device. Port DMA transitions to a fatal state until the software clears P#CMD.ST bit or resets the interface by way of Port or Global reset.
23	0b	RWC	IPMS	**Incorrect Port Multiplier Status** Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. This bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. The software must use the IPMS bit only after enumeration is complete on the Port Multiplier.
22	0b	RO	PRCS	**PHY Ready Change Status** This bit reflects the state of the P#SERR.DIAG_N bit. When set to 1, indicates the internal p#_phy_ready signal changed state. To clear this bit, the software must clear the P#SERR.DIAG_N bit to 0.
21 :08	0h	RO		Reserved.
07	0b	RO	DMPS	**Device Mechanical Presence Status** This field is reserved.
06	0b	RO	PCS	**Port Connect Change Status** This bit reflects the state of the P#SERR.DIAG_X bit: 0 = No change in Current Connect Status. 1 = Change in Current Connect Status; This bit is cleared only when P#SERR.DIAG_X is cleared.

Table 163. 110h: Port# Interrupt Status Register (P#IS) (Sheet 3 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		#: 0 / 1 Offset Start: 110h/190h Offset End: 113h/193h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
05	0b	RWC	DPS	**Descriptor Processed** A PRD with the I bit set has transferred all of its data. ***Note:*** This is an opportunistic interrupt and must not be used to definitively indicate the end of a transfer. Two PRD interrupts could happen close in time together such that the second interrupt is missed when the first PRD interrupt is being cleared.
04	0b	RO	UFS	**Unknown FIS Interrupt** When set to 1, indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by the software clearing the P#SERR.DIAG_F bit to 0. ***Note:*** The UFS bit does not directly reflect the P#SERR.DIAG_F bit. P#SERR.DIAG_F bit is set immediately when an unknown FIS is detected, whereas the UFS bit is set when that FIS is posted to memory. The software should wait to act on an unknown FIS until the UFS bit is set to 1 or the two bits may become out of sync.
03	0b	RWC	SDBS	**Set Device Bits Interrupt** A Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.
02	0b	RWC	DSS	**DMA Setup FIS Interrupt** A DMA Setup FIS has been received with the 'I' bit set and has been copied into system memory.
01	0b	RWC	PSS	**PIO Setup FIS Interrupt** A PIO Setup FIS has been received with the 'I' bit set, has been copied into system memory, and the data related to that FIS has been transferred. This bit is set even when the data transfer results in an error.
00	0b	RWC	DHRS	**Device to Host Register FIS Interrupt** A D2H Register FIS has been received with the 'I' bit set, and has been copied into system memory.

7.3.3.26 Port# Interrupt Enable Register (P#IE)

This register enables and disables the reporting of the corresponding interrupt to the software. When a bit is set (1) and the corresponding interrupt condition is active, the SATA intrq output is asserted.

Interrupt sources that are disabled (0) are still reflected in the status registers. This register is symmetrical with the P#IS register. This register is reset on Global SATA reset.

Table 164. 114h: Port# Interrupt Enable Register (P#IE) (Sheet 1 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		#: 0 / 1 Offset Start: 114h/194h Offset End: 117h/197h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31	0b	RO	CPDE	**Cold Port Detect Enable** This field is reserved.

Table 164. 114h: Port# Interrupt Enable Register (P#IE) (Sheet 2 of 3)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 114h/194h **Offset End:** 117h/197h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
30	0b	RW	TFEE	**Task File Error Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.TFES=1
29	0b	RW	HBFE	**Host Bus Fatal Error Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.HBFS=1
28	0b	RW	HBDE	**Host Bus Data Error Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.HBDS=1
27	0b	RW	IFE	**Interface Fatal Error Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.IFS=1
26	0b	RW	INFE	**Interface Non-Fatal Error Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.INFS=1
25	0b	RO		Reserved.
24	0b	RW	OFE	**Overflow Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.OFS=1
23	0b	RW	IPME	**Incorrect Port Multiplier Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.IPMS=1
22	0b	RW	PRCE	**PHY Ready Change Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.PRCS=1
21 :08	0000h	RO		Reserved.

Table 164. 114h: Port# Interrupt Enable Register (P#IE) (Sheet 3 of 3)

Size: 32-bit			Default: 00000000h		Power Well: Core
Access	PCI Configuration		B:D:F D6:F0		#: 0 / 1 Offset Start: 114h/194h Offset End: 117h/197h
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
07	0b	RO	DMPE	**Device Mechanical Presence Enable** This field is reserved.	
06	0b	RW	PCE	**Port Change Interrupt Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.PCS=1	
05	0b	RW	DPE	**Descriptor Processed Interrupt Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.DPS=1	
04	0b	RW	UFE	**Unknown FIS Interrupt Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.UFS=1	
03	0b	RW	SDBE	**Set Device Bits FIS Interrupt Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.SDBS=1	
02	0b	RW	DSE	**DMA Setup FIS Interrupt Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.DSS=1	
01	0b	RW	PSE	**PIO Setup FIS Interrupt Enable** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.PSS=1	
00	0b	RW	DHRE	**Device to Host Register FIS Interrupt** Dependencies: When the following conditions are true, the intrq output signal is asserted: • This bit=1 • GHC.IE=1 • P#IS.DHRS=1	

7.3.3.27 Port# Command Register (P#CMD)

This register contains bits controlling various Port functions. All RW bits are reset on Global reset.

Table 165. 118h: Port# Command Register (P#CMD) (Sheet 1 of 4)

Size: 32-bit		**Default:** See below		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 118h/198h **Offset End:** 11Bh/19Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :28	0h	RW	ICC	**Interface Communication Control** This field is used to control power management states of the interface. When the Link layer is currently in the L_IDLE state, writes to this field causes the port to initiate a transition to the interface power management state requested. When the Link layer is not currently in the L_IDLE state, writes to this field have no effect. • Fh.- 7h: Reserved • 6h: Slumber. This causes the port to request a transition of the interface to the Slumber state. The SATA device can reject the request and the interface remains in its current state. • 5h.- 3h: Reserved • 2h: Partial. This causes the port to request a transition of the interface to the Partial state. The SATA device can reject the request and the interface remains in its current state. • 1h: Active. This causes the port to request a transition of the interface into the active state. • 0h: No-Op/ Idle. This value indicates to the software that the Port# is ready to accept a new interface control command, although the transition to the previously selected state may not yet have occurred. When the software writes a non-reserved value other than No-Op (0h), the Port performs the action and updates this field back to Idle (0h). When the software writes to this field to change the state to a state where the link is already in (i.e., interface is in the active state and a request is made to go to the active state), the port takes no action and returns this field to Idle. When the interface is in a low power state and the software wants to transition to a different low power state, the software must first bring the link to active and then initiate the transition to the desired low power state.
27	0b	RW	ASP	**Aggressive Slumber/ Partial** The options for this field are: • When set to 1, and P#CMD.ALPE=1, the Port aggressively enters the SLUMBER state when one of the following conditions is true: • The Port clears the P#CI and the P#SACT register is cleared. • The Port clears the P#SACT register and P#CI is cleared. • When cleared to 0, and P#CMD.ALPE=1, the Port aggressively enters the PARTIAL state when one of the following conditions is true: • The Port clears the P#CI register and the P#SACT register is cleared. • The Port clears the P#SACT register and P#CI is cleared.
26	0b	RW	ALPE	**Aggressive Link Power Management Enable** When set to 1, the Port aggressively enters a lower link power state (PARTIAL or SLUMBER) based on the setting of the P#CMD.ASP bit. When cleared to 0, aggressive power management state transition is disabled.
25	0b	RW	DLAE	**Drive LED on ATAPI Enable** When set to 1, P#CMD.ATAPI=1, and commands are active, and the Port asserts p#_act_led output.
24	0b	RW	ATAPI	**Device is ATAPI** This bit is used by the port to control whether to assert p#_act_led output, when commands are active. The options for this field are: 0 = non-ATAPI device 1 = ATAPI device

Table 165. 118h: Port# Command Register (P#CMD) (Sheet 2 of 4)

Size: 32-bit		**Default:** See below		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 118h/198h **Offset End:** 11Bh/19Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
23	0b	RW	APSTE	**Automatic Partial to Slumber Transitions Enable** When this bit is set, the SATA Link layer transitions from its Partial power management state into Slumber state automatically, regardless of whether it was host software-, Port (aggressive)-, or device initiated.
22	0b	RO		Reserved.
21	HwInit	RW	ESP	**External SATA Port** When set to 1, indicates that this Port's signal only connector is externally accessible. When set to 1, CAP.SXS is also set to 1. When cleared to 0, indicates that this Port's signal only connector is not externally accessible. ***Note:*** The ESP bit is mutually exclusive with #CMD.HPCP.
20	0b	RO	CPD	**Cold Presence Detection** This field is reserved.
19	0b	RO	MPSP	**Mechanical Presence Switch Attached to Port** This field is reserved.
18	HwInit	RO	HPCP	**Hot Plug Capable Port** The options for this field are: 0 = Indicates that this Port's signal and power connectors are not externally accessible. 1 = Indicates that this Port's signal and power connectors are externally accessible via a joint signal-power connector for blindmate device hot plug. ***Note:*** The HPCP bit is mutually exclusive with P#CMD.ESP.
17	0b	RW	PMA	**Port Multiplier Attached** The software is responsible for detecting whether a Port Multiplier is present; the SATA Port does not auto-detect the presence of a Port Multiplier. The options for this field are: 0 = A Port Multiplier is not attached to this port. 1 = A Port Multiplier is attached to this port.
16	0b	RO	CPS	**Cold Presence State** This bit reports whether a device is currently detected on this port as indicated by the p#_cp_det input state (assuming P#CMD.CPD=1). The options for this field are: 0 = no device attached to this Port 1 = device is attached to this Port
15	0b	RO	CR	**Command List Running** When this bit is set to '1', the command list DMA engine for this port is running. See AHCI state machine in AHCI specification section 5.3.2 for details on when this bit is set and cleared by the port.
14	0b	RO	FR	**FIS Receive Running** When set to '1', the FIS Receive DMA engine for the port is running. See AHCI specification section 10.3.2 for details on when this bit is set and cleared by the port.

Table 165. 118h: Port# Command Register (P#CMD) (Sheet 3 of 4)

Size: 32-bit		**Default:** See below		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 118h/198h **Offset End:** 11Bh/19Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
13	0b	RO	MPSS	**Mechanical Presence Switch State** The software must use this bit only when both CAP.SMPS and P#CMD.MPSP are set. This bit reports the state of a mechanical presence switch attached to this port as indicated by the p#_mp_switch input state (assuming CAP.SMPS=1 and #CMD.MPSP=1). The options for this field are: 0 = Switch is closed 1 = Switch is open When CAP.SMPS=0, this bit is cleared to 0.
12 :08	00h	RO	CCS	**Current Command Slot** This field is set to the command slot value of the command that is currently being issued by the Port. • When P#CMD.ST transitions from 1 to 0, this field is re-cleared to 00h. • After P#CMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is P#CMD.CCS+1. For example, after the port has issued its first command, when CCS=00h and P#CI is cleared to 3h, the next command issued is from command slot 1. This field is valid only when P#CMD.ST is set to 1.
07 :05	000b	RO		Reserved.
04	0b	RW	FRE	**FIS Receive Enable** When set to 1, the port may post received FISes into the FIS receive area pointed to by P#FB. When cleared, received FISes are not accepted by the port, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. The software must not set this bit until P#FB has been programmed with a valid pointer to the FIS receive area. When the software wishes to move the base, this bit must first be cleared, and the software must wait for the P#CMD.FR bit to be cleared.
03	0b	WO	CLO	**Command List Override** Setting this bit to 1 causes P#TFD.STS.BSY and P#TFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the P#TFD.STS register. This bit is cleared to 0, when P#TFD.STS.BSY and P#TFD.STS.DRQ have been cleared to 0. A write to this register with a value of '0' has no effect. This bit should only be set to 1 immediately prior to setting P#CMD.ST bit to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and results in indeterminate behavior.
02	0b	RO	POD	**Power On Device** This field is reserved.
01	0/1b	RW,RO	SUD	**Spin-Up Device** This bit is read/write when staggered spin-up is supported as indicated by the CAP.SSS=1. This bit is read-only 1 when staggered spin-up is not supported and CAP.SSS=0. On an edge detect from 0 to 1, the port starts a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. ***Note:*** The SUD bit is read-only 0 on power-up until, CAP.SSS bit is written with the required value.

Table 165. 118h: Port# Command Register (P#CMD) (Sheet 4 of 4)

Size: 32-bit		Default: See below		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		#: 0 / 1 Offset Start: 118h/198h Offset End: 11Bh/19Bh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
00	0b	RW	ST	**Start** When set to 1, the port processes the command list. When cleared, the port does not process the command list. Whenever this bit is changed from a 0 to a 1, the port starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the P#CI register is cleared by the port upon transition into an idle state. Refer to AHCI specification, section 10.3.1, for important restrictions on when this bit can be set to 1. ***Note:*** P#SERR register must be cleared prior to setting ST bit to 1.

7.3.3.28 Port# Task File Data Register (P#TFD)

This register contains Error and Status registers updated every time a new Register FIS, PIO Setup FIS or Set Device Bits FIS is received from the device. Reset on Global or Port reset (COMRESET).

Table 166. 120h: Port# Task File Data Register (P#TFD)

Size: 32-bit		Default: 0000007Fh		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		#: 0 / 1 Offset Start: 120h/1A0h Offset End: 123h/1A3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :16	0000h	RO		Reserved.
15 :08	00h	RO	ERR	**Error** This field contains the latest copy of the task file error register.
07 :00	7Fh	RO	STS	**Status** This field contains the latest copy of the task file status register. The bits that affect SATA operation are: • Bit [7] BSY - Indicates the interface is busy • Bits [6:4] cs - Command specific • Bit [3] DRQ - Indicates a data transfer is requested • Bits [2:1] cs - Command specific • Bit [0] ERR - Indicates an error during the transfer ***Note:*** The Port updates the entire 8-bit field, not just the bits noted above.

7.3.3.29 Port# Signature Register (P#SIG)

Table 167. 124h: Port# Signature Register (P#SIG)

Size: 32-bit		**Default:** FFFFFFFFh		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 124h/1A4h **Offset End:** 127h/1A7h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	FFFFFFFFh	RO	SIG	**Signature** This field contains the signature received from a device on the first D2H Register FIS. The bit order as follows: • Bits [31:24] - LBA High (Cylinder High) Register • Bits [23:16] - LBA Mid (Cylinder Low) Register • Bits [15:8] - LBA Low (Sector Number) Register • Bits [7:0] - Sector Count Register This field is updated once after a reset sequence. Reset on Global or Port reset.

7.3.3.30 Port# Serial ATA Status {SStatus} Register (P#SSTS)

This 32-bit register conveys the current state of the interface and host. The Port updates it continuously and asynchronously. When the Port transmits a COMRESET to the device, this register is updated to its reset values (i.e., Global reset, Port reset, or COMINIT from the device.

Table 168. 128h: Port# Serial ATA Status {SStatus} Register (P#SSTS) (Sheet 1 of 2)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 128h/1A8h **Offset End:** 12Bh/1ABh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :12	00000h	RO		Reserved.
11 :08	0h	RO	IPM	**Interface Power Management** Indicates the current interface state. The options for this field are: 0h: Device not present or communication not established 1h: Interface in active state 2h: Interface in Partial power management state 6h: Interface in Slumber power management state All other values are reserved.
07 :04	0h	RO	SPD	**Current Interface Speed** Indicates the negotiated interface communication speed. The options for this field are: 0h: Device not present or communication not established 1h: Generation 1 communication rate negotiated 2h: Generation 2 communication rate negotiated All other values reserved.

Table 168. 128h: Port# Serial ATA Status {SStatus} Register (P#SSTS) (Sheet 2 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		#: 0 / 1 Offset Start: 128h/1A8h Offset End: 12Bh/1ABh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
03 :00	0h	RO	DET	**Device Detection** Indicates the interface device detection and PHY state. The options for this field are: 0h: No device detected and PHY communication not established 1h: Device presence detected but PHY communication not established (COMINIT is detected) 3h: Device presence detected and PHY communication established ("PHY Ready" is detected) 4h: PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved.

7.3.3.31 Port# Serial ATA Control {SControl} Register (P#SCTL)

This 32-bit read-write register is used by the software to control SATA interface capabilities. Writes to this register result in an action being taken by the Port PHY interface. Reads from the register return the last value written to it. Reset on Global reset.

These bits are static and should not be changed frequently due to the clock crossing between the Transport and Link Layers. The software must wait for at least seven periods of the slower clock (clk_asic# or CLKH) before changing this register.

Table 169. 12Ch: Port# Serial ATA Control {SControl} Register (P#SCTL) (Sheet 1 of 2)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		#: 0 / 1 Offset Start: 12Ch/1ACh Offset End: 12Fh/1AFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :12	000000h	RW		Reserved.
11 :08	0h	RW	IPM	**Interface Power Management Transitions Allowed** This field indicates the power states that the Port PHY interface is allowed to transition to. When an interface power management state is disabled, the port does not initiate that state and any request from the device to enter that state is rejected via PMNAKp. The options for this field are: 0h: No interface power management state restrictions 1h: Transitions to the Partial state disabled 2h: Transitions to the Slumber state disabled 3h: Transitions to both Partial and Slumber states disabled All other values reserved and should not be used.

Table 169. 12Ch: Port# Serial ATA Control {SControl} Register (P#SCTL) (Sheet 2 of 2)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 12Ch/1ACh **Offset End:** 12Fh/1AFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
07 :04	0h	RW	SPD	**Speed Allowed** This field indicates the highest allowable speed of the Port PHY interface. The options for this field are: 0h: No speed negotiation restrictions 1h: Limit speed negotiation to Generation 1 communication rate 2h: Limit speed negotiation to a rate not greater than Generation 2 communication rate All other values reserved and should not be used. ***Note:*** When the host software must change this field value, the host must also reset the port (P#SCTL.DET = 1h) at the same time to ensure proper speed negotiation.
03 :00	0h	RW	DET	**Device Detection Initialization** Controls the device detection and interface initialization of the port. The options for this field are: 0h: No device detection or initialization action requested 1h: Perform interface initialization sequence to establish communication. This results in the interface being reset and communication re-initialized. 4h: Disable the Serial ATA interface and put the Port PHY in offline mode. All other values reserved. ***Notes:*** 1. This field may only be modified when P#CMD.ST is 0. 2. Changing the field while the P#CMD.ST=1 results in undefined behavior. When P#CMD.ST is set to 1, this field should have a value of 0h.

7.3.3.32 Port# Serial ATA Error {SError} Register (P#SERR)

This 32-bit register represents all the detected interface errors accumulated since the last time it was cleared.

The set bits in the SError register indicate that the corresponding error condition became true one or more times since the last time the bit was cleared. The set bits in this register are explicitly cleared by a write operation to the register, Global reset, or Port reset (COMRESET). The value written to clear the set error bits should have ones encoded in the bit positions corresponding to the bits that are to be cleared. All bits in the following table have a reset value of 0.

Table 170. 130h: Port# Serial ATA Error {SError} Register (P#SERR) (Sheet 1 of 3)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 130h/1B0h **Offset End:** 133h/1B3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :27	00000b	RO		Reserved.
26	0b	RWC	DIAG_X	**Exchanged** This bit is set to 1 when PHY COMINIT signal is detected. This bit is reflected in the P#IS.PCS bit.

Table 170. 130h: Port# Serial ATA Error {SError} Register (P#SERR) (Sheet 2 of 3)

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		#: 0 / 1 Offset Start: 130h/1B0h Offset End: 133h/1B3h

Bit Range	Default	Access	Acronym	Description
25	0b	RWC	DIAG_F	**Unknown FIS Type** This bit indicates that one or more FISes were received by the Transport layer with good CRC, but had a type field that was not recognized/known and the length was less than or equal to 64bytes. ***Note:*** When the unknown FIS length exceeds 64 bytes, the DIAG_F bit is not set and the DIAG_T bit is set instead.
24	0b	RWC	DIAG_T	**Transport State Transition Error** This bit indicates that a Transport Layer protocol violation was detected since the last time this bit was cleared.
23	0b	RWC	DIAG_S	**Link Sequence Error** This bit indicates that one or more Link state machine error conditions were encountered. One of the conditions that caused this bit to be set is device doing SYNC escape during FIS transmission.
22	0b	RWC	DIAG_H	**Handshake Error** This bit indicates that one or more R_ERRp was received in response to frame transmission. Such errors may be the result of a CRC error detected by the device, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	0b	RWC	DIAG_C	**CRC Error** This bit indicates that one or more CRC errors were detected by the Link layer during FIS reception.
20	0b	RO	DIAG_D	**Disparity Error** This bit is always cleared to 0 since it is not used by the AHCI specification.
19	0b	RWC	DIAG_B	**10B to 8B Decode Error** This bit indicates errors were detected by 10b8b decoder. ***Note:*** This bit is set only when an error is detected on the received FIS data dword. This bit is not set when an error is detected on the primitive, regardless whether it is inside or outside the FIS.
18	0b	RWC	DIAG_W	**Comm Wake** This bit is set when PHY COMWAKE signal is detected.
17	0b	RWC	DIAG_I	**PHY Internal Error** This bit is set when the PHY detects some internal error as indicated by the assertion of the p#_phy_rx_err input. ***Note:*** The setting of this bit is controlled by the BISTCR.ERREN bit: when ERREN==0 (default), only errors occurring inside the received FIS cause DIAG_I bit to be set; when ERREN==1, any error inside or outside the FIS causes the DIAG_I bit to be set.
16	0b	RWC	DIAG_N	**PHY Ready Change** This bit indicates that the PHY Ready signal changed state. This bit is reflected in the P#IS.PRCS bit.
15 :12	0h	RO		Reserved.
11	0b	RWC	ERR_E	**Internal Error** This bit is set to 1 when one or more BUS ERROR responses are detected on the master or the slave interfaces.
10	0b	RWC	ERR_P	**Protocol Error** This bit is set to 1 when any of the following conditions are detected. • Transport state transition error (DIAG_T) • Link sequence error (DIAG_S) • RxFIFO overflow • Link bad end error (WTRM instead of EOF is received).

Table 170. 130h: Port# Serial ATA Error {SError} Register (P#SERR) (Sheet 3 of 3)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 130h/1B0h **Offset End:** 133h/1B3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
09	0b	RWC	ERR_C	**Non-Recovered Persistent Communication Error** This bit is set to 1 when PHY Ready signal is de-asserted due to the loss of communication with the device or problems with interface, but not after transition from Active to Partial or Slumber power management state.
08	0b	RWC	ERR_T	**Non-Recovered Transient Data Integrity Error** This bit is set when any of the following P#SERR register bits is set during Data FIS transfer: • ERR_P (Protocol) • DIAG_C (CRC) • DIAG_H (Handshake) • ERR_C (“PHY Ready” negation)
07 :02	000000b	RO		Reserved.
01	0b	RWC	ERR_M	**Recovered Communication Error** This bit is set to 1 when PHY Ready condition is detected after interface initialization, but not after transition from Partial or Slumber power management state to active state.
00	0b	RWC	ERR_I	**Recovered Data Integrity** This bit is set when any of the following P#SERR register bits is set during non-Data FIS transfer: • ERR_P (Protocol) • DIAG_C (CRC) • DIAG_H (Handshake) • ERR_C (“PHY Ready” negation)

7.3.3.33 Port# Serial ATA Active {SActive} Register (P#SACT)

Table 171. 134h: Port# Serial ATA Active {SActive} Register (P#SACT)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 134h/1B4h **Offset End:** 137h/1B7h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RWS	DS	**Device Status** This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. Software sets this field prior to issuing a native queued command for a particular command slot. Prior to writing P#CI[TAG] to 1, the software sets DS[TAG] to 1 to indicate that a command with that TAG is outstanding. This field is cleared to 0 when: • The software writes P#CMD.ST from a 1 to a 0. • The device sends a Set Device Bits FIS to the Port. The port clears bits in this field that are set in the SActive field of the Set Device Bits FIS. The port clears only bits that correspond to native queued commands that have completed successfully. This field is not cleared by the following: • Port reset (COMRESET). • Software reset. Software must write this field only when P#CMD.ST bit is set to 1.

7.3.3.34 Port# Command Issue Register (P#CI)

Table 172. 138h: Port# Command Issue Register(P#CI)

Size: 32-bit		**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 138h/1B8h **Offset End:** 13Bh/1BBh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :00	00000000h	RWS	CI	**Command Issued** This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by the software to indicate to the port that a command has been built in system memory for a command slot and may be sent to the device. When the Port receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field can only be set to 1 by the software when P#CMD.ST is set to 1. This field is reset when P#CMD.ST is written from a 1 to a 0 by the software.

7.3.3.35 Port# Serial ATA Notification Register (P#SNTF)

This register is used to determine when asynchronous notification events have occurred for directly connected devices and devices connected to a Port Multiplier.

Table 173. 13Ch: Port# Serial ATA Notification Register (P#SNTF)

Size: 32-bit		**Default:** 00000044h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 13Ch/13Fh **Offset End:** 1BCh/1BFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31: 16	0000h	RO		Reserved.
15 :00	0000h	RWC	PMN	**PM Notify** This field indicates whether a particular device with the corresponding PM Port number has issued a Set Device Bits FIS to the SATA Port with the Notification bit set: • PM Port 0h sets bit 0, • PM Port 1h sets bit 1, ... • PM Port Fh sets bit 15. Individual bits are cleared by the software writing 1s to the corresponding bit positions. This field is reset on Global reset, but it is not reset by Port reset (COMRESET) or software reset.

7.3.3.36 Port# DMA Control Register (P#DMACR)

This register contains bits for controlling the Port DMA engine. The software can change the fields of this register only when P#CMD.ST=0. Power-up (system reset), Global reset or Port reset (COMRESET) reset this register to the default value.

Table 174. 170h: Port# DMA Control Register (P#DMACR) (Sheet 1 of 2)

Size: 32-bit		**Default:** 00000046h		**Power Well:** Core
Access	PCI Configuration	**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 170h/1F0h **Offset End:** 173h/1F3h
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :16	0000h	RO		Reserved.
15 :12	0h	RW,RO	RXABL	**Receive BUS Burst Limit** This field allows the software to limit the BUS master write burst size. The options for this field are: • 0h, 9h - Fh: Limit BUS burst size to 256 DWORDs • 1h: Limit BUS burst size to 1 DWORD • 2h: Limit BUS burst size to 2 DWORDs • 3h: Limit BUS burst size to 4 DWORDs • 4h: Limit BUS burst size to 8 DWORDs • 5h: Limit BUS burst size to 16 DWORDs • 6h: Limit BUS burst size to 32 DWORDs • 7h: Limit BUS burst size to 64 DWORDs • 8h: Limit BUS burst size to 128 DWORDs ***Notes:*** 1. SATA Controller BUS master breaks the burst at 1 KB address boundary regardless of the RXABL value. 2. This field is read-write when P#CMD.ST=0 and read-only when P#CMD.ST=1.

Table 174. 170h: Port# DMA Control Register (P#DMACR) (Sheet 2 of 2)

Size: 32-bit		Default: 00000046h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		#: 0 / 1 Offset Start: 170h/1F0h Offset End: 173h/1F3h

Bit Range	Default	Access	Acronym	Description
11 :08	0h	RW,RO	TXABL	**Transmit BUS Burst Limit** This field allows the software to limit the BUS master read burst size. The options for this field are: • 0h, 9h - Fh: Limit BUS burst size to 256 DWORDs • 1h: Limit BUS burst size to 1 DWORD • 2h: Limit BUS burst size to 2 DWORDs • 3h: Limit BUS burst size to 4 DWORDs • 4h: Limit BUS burst size to 8 DWORDs • 5h: Limit BUS burst size to 16 DWORDs • 6h: Limit BUS burst size to 32 DWORDs • 7h: Limit BUS burst size to 64 DWORDs • 8h: Limit BUS burst size to 128 DWORDs ***Notes:*** 1. SATA controller BUS master breaks the burst at 1 KB address boundary regardless of the TXABL value. 2. This field is read-write when P#CMD.ST=0 and read-only when P#CMD.ST=1.
07 :04	4h	RW,RO	RXTS	**Receive Transaction Size** This field defines the Port DMA transaction size in DWORDs for receive (system bus write, device read) operation. The options for this field are: • 0h: 1 DWORD • 1h: 2 DWORDs • 2h: 4 DWORDs • 3h: 8 DWORDs • 4h: 16 DWORDs • 5h: 32 DWORDs • 6h: 64 DWORDs (maximum value) All other values are reserved and should not be used. This field is read-write when P#CMD.ST=0 and read-only when P#CMD.ST=1. The maximum value of this field is determined by the RxFIFO depth set by the P#_RXFIFO_DEPTH parameter. When the software attempts to write a value exceeding this value, the maximum value would be set instead.
03 :00	6h	RW,RO	TXTS	**Transmit Transaction Size** This field defines the DMA transaction size in DWORDs for transmit (system bus read, device write) operation. The options for this field are: • 0h: 1 DWORD • 1h: 2 DWORDs • 2h: 4 DWORDs • 3h: 8 DWORDs • 4h: 16 DWORDs • 5h: 32 DWORDs • 6h: 64 DWORDs (maximum value) All other values are reserved and should not be used. This field is read-write when P#CMD.ST=0 and read-only when P#CMD.ST=1. The maximum value of this field is determined by the TxFIFO depth set by the P#_TXFIFO_DEPTH parameter. When the software attempts to write a value exceeding this value, the maximum value would be set instead.

7.3.3.37 Port# PHY Control Register (P#PHYCR)

This register is used for Port PHY control.

Table 175. 178h: Port# PHY Control Register (P#PHYCR)

Size: 32-bit			**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 178h/1F8h **Offset End:** 17Bh/1FBh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :00	00000000h	RO	PPC	**Port PHY Control** This location is reserved.	

7.3.3.38 Port# PHY Status Register (P#PHYSR)

This register is used to monitor PHY status.

Table 176. 17Ch: Port# PHY Status Register (P#PHYSR)

Size: 32-bit			**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**#:** 0 / 1 **Offset Start:** 17Ch/1FCh **Offset End:** 17Fh/1FFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :00	00000000h	RO	PPS	**Port PHY Status.** This location is reserved.	

7.3.3.39 Test Register 2 (TESTR2)

This register is used only for Port Test. Writing to this register during normal operation is prohibited.

Table 177. 3F8h: TEST Register 2

Size: 32-bit			**Default:** 00000000h		**Power Well:** Core
Access	PCI Configuration		**B:D:F** D6:F0		**Offset Start:** 3F8h **Offset End:** 3FBh
Bit Range	**Default**	**Access**	**Acronym**	**Description**	
31 :03	00000000h	RO		Reserved	
02	0b	RW		**Force PHY ready for Port0/1 Test**: This bit enables only at bit0=1 0 = Normal 1 = Force to PHY ready state	
01	0b	RW		**Force PHY speed for Port0/1 test:** This bit enables only at bit0=1 0 = Gen1 only 1 = Gen1 and Gen2	

Table 177. 3F8h: TEST Register 2

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		Offset Start: 3F8h Offset End: 3FBh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
00	0b	RW	PSRST0	**Test mode enable:** Allows writing to this register only at test (e.g., compliance test). 0 = Disable 1 = Enable

7.3.3.40 PHY SOFT RESET Register (PSRST)

Table 178. 3FCh: PHY SOFT PHY RESET Register

Size: 32-bit		Default: 00000000h		Power Well: Core
Access	PCI Configuration	B:D:F D6:F0		Offset Start: 3FCh Offset End: 3FFh
Bit Range	**Default**	**Access**	**Acronym**	**Description**
31 :02	00000000h	RO		Reserved
01	0b	RW	PSRST1	**PHY Reset 1:** This register controls the reset signal of SATA PHY#1. When the register is set to"1", SATA PHY#1 is reset (ON). When the register is set to"0", the reset state of the SATA PHY#1 is released (OFF). Only the hardware reset signal clears this register. This register does not clear itself. 0 = Reset de-assert 1 = Reset assert
00	0b	RW	PSRST0	**PHY Reset 0:** This register controls the reset signal of SATA PHY#0. When the register is set to"1", SATA PHY#is reset (ON). When the register is set to"0", the reset state of the SATA PHY#is released (OFF). Only the hardware reset signal clears this register. This register does not clear itself. 0 = Reset de-assert 1 = Reset assert

7.4 Functional Description

7.4.1 Operation Details

7.4.1.1 Data Transfer

Each SATA Controller Port has its own DMA engine implemented in the Polarization division multiple access (PDMA) module. Its operation is based on the AHCI specification Port State Machine. The following sections outline examples of the ATA DMA read and write transfers.

7.4.1.1.1 ATA DMA Read

Following is the DMA read sequence:

1. Software finds a free command slot by reading the P#CI register, then builds a DMA read command in the Command List for the port to execute, and sets the bit corresponding to this command slot in the P#CI register.
2. The PDMA fetches the Command Header from system memory.
3. The PDMA fetches the Command Register FIS from system memory and transfers it to the device.
4. Since this was a DMA read command, the device responds with a number of Data FISes. When they arrive, PDMA performs the following operations:
   a. Fetches the first PRD from system memory.
   b. Transfers data from the RxFIFO to system memory until the byte count for this PRD is satisfied.
   c. Continues to fetch PRDs and transfer data until the byte count for the command is satisfied.
5. Device sends D2H Register FIS with the command ending status and when the I-bit is set, interrupt is generated. D2H Register FIS is posted to the Received FIS memory structure.
6. When this is the last command and the SATA Controller is enabled for aggressive power management, the PDMA requests the Link Layer to enter either Partial or Slumber state.

7.4.1.1.2 ATA DMA Write

The DMA write sequence is as follows:

1. Software finds a free command slot by reading the P#CI register, then builds a DMA write command in the Command List for the port to execute and sets the bit corresponding to this command slot in the P#CI register.
2. The PDMA fetches the Command Header from system memory.
3. The PDMA fetches the command Register FIS from system memory and transfers it to the device.
4. Device responds with DMA Activate FIS. When it arrives, PDMA performs the following operations:
   a. Fetches the first PRD from system memory;
   b. Transfers data from system memory to TxFIFO until the PRD byte count is satisfied or 8-KB FIS boundary is reached. The Link layer sends Data FIS to the device. If more than one FIS is needed, device sends DMA Activate FIS for each Data FIS;
   c. Continues to fetch PRDs and transfer data until the byte count for the command is satisfied.
5. Device sends D2H Register FIS with the command ending status and when the I-bit is set, interrupt is generated. D2H Register FIS is posted to the Received FIS memory structure.
6. When this is the last command and the SATA Controller is enabled for aggressive power management, the PDMA requests the Link Layer to enter either Partial or Slumber state.

7.4.1.1.3 Native Queued Command (NCQ) Transfers

The SATA Controller supports N CQ feature (READ/WRITE FPDMA QUEUED commands). Data transfers are activated via the DMA Setup FIS, and command completion is performed via the Set Device Bits FIS.

Note: Device must also support NCQ; otherwise it aborts READ/WRITE FPDMA QUEUED commands. The non-zero buffer offset feature should be disabled in the device.

7.4.1.1.4 PIO Transfer

The SATA Controller supports multiple DRQ block PIO operation (CAP.PMD=1). From the SATA Controller point of view, PIO transfer looks like a DMA transfer: a command table is set up and the PDMA module transfers the data from or to system memory.

7.4.1.1.5 Transfer Size

Normally, all SATA Controller BUS master transfers are done with 32-bit transfer size and 32-bit-aligned addresses. When the transfer count for a command has odd number of 16-bit words (e.g., 257 words, or 514 bytes), then on device reads the device pad bits [31:16] of the last Data FIS DWORD with zeroes, and on device writes, SATA Controller would clear bits [31:16] of the last Data FIS DWORD sent to the device.

Odd-word transfer count implies creating a PRD with odd-word byte count and possibly 16-bit-aligned data address.

Setting PRD Data Base Address (DBA) or Byte Count (DBC) to a 16-bit-aligned value (e.g., 2, 6, 10, etc.) results in 16-bit single transfers on BUS master interface regardless of the P#DMACR.RXTS/TXTS values. This is due to the fact that SATA Controller operation is optimized for 32-bit operation when both DBA and DBC are 32-bit-aligned (for example, 4, 8, and so forth).

Note: To achieve maximum performance with odd-word transfer, it is recommended that the PRD with the odd-word byte count is the last and the smallest PRD of all the PRDs for the command and the rest of the PRDs are all 32-bit-aligned. This assumes that the starting address of the data is 32-bit-aligned

7.4.1.2 Power Management

The software, the port itself or the device can initiate the SATA Controller Port power management states (PARTIAL or SLUMBER). The power state machine is implemented in the Link Layer power management module. It asserts corresponding signal to the PHY to enter the power management state.

Software requests transition to either PARTIAL or SLUMBER state using the P#CMD.ICC field, however, the port acts on it when the Link Layer is currently in the L_IDLE state, otherwise this request is ignored.

The device requests power management state by transmitting PMREQ_Pp or PMREQ_Sp primitives to the Port. Software can disable transition to power management states using the P#SCTL.IPM field.

The SATA Controller supports aggressive power management states that allow the port to initiate an interface power management state as soon as there are no commands outstanding to the device. The P#CMD.ALPE bit defines whether the feature is enabled and the P#CMD.ASP field controls whether PARTIAL or SLUMBER power

The Port when enabled, initiates the SLUMBER state. When P#CMD.ALPE='1' and the port recognizes that there are no commands to process, the port transitions to PARTIAL or SLUMBER state based upon the P#CMD.ASP setting. The port recognizes no commands to transmit as either:

- P#SACT is cleared to 0h and the P#CI is updated from a non-zero value to 0h.
- P#CI is cleared to 0h and a Set Device Bits FIS is received, which updates P#SACT from a non-zero value to 0h.

SATA Controller supports automatic PARTIAL to SLUMBER power state transition feature. When the software sets the bit P#CMD.APSTE, this is enabled. When P#CMD.APSTE=1 and the SATA Controller Link is in PARTIAL state, the core automatically transitions to SLUMBER state regardless of whether it was host software-initiated, Port (aggressive)- initiated, or device-initiated.

The power management state is terminated when either one of the following conditions becomes true:

- Software requests transition to active state by writing P#CMD.ICC=1h
- Device requests interface Wake-up by transmitting COMWAKE OOB sequence

The state of the interface (active, PARTIAL, or SLUMBER power management) is reflected in the P#SSTS.IPM field.

7.4.1.3 Port Multiplier Support

The SATA Controller supports Port Multiplier functionality with command-based switching. When a port is connected to a Port Multiplier, software must first enumerate it by issuing software reset to Port 0Fh (control Port) on the Port Multiplier. When the signature returned corresponds to a Port Multiplier, a Port Multiplier is attached. When the signature returned corresponds to another device type, a Port Multiplier is not attached.

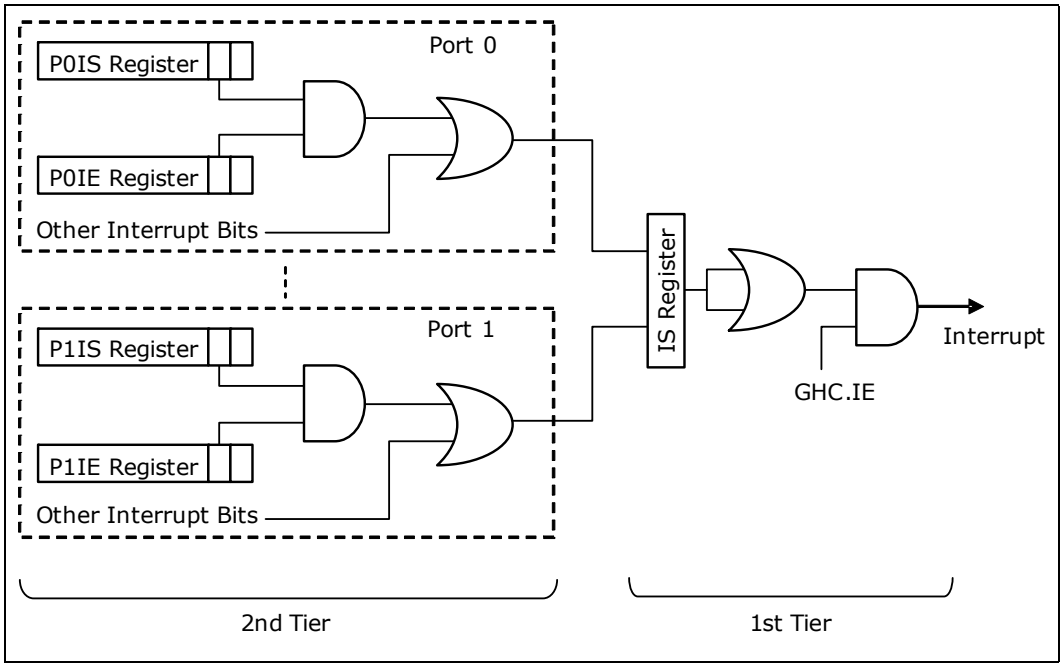
The SATA Controller provides command list override feature (as indicated by the CAP.SCLO=1) via P#CMD.CLO to help software reliably enumerate the Port Multiplier:

- Software ensures that P#CMD.ST bit is '0';
- Software constructs the two Register FISes required for a software reset in the command list, where the PM Port field value in the Register FIS is cleared to 0Fh;
- Software sets P#CMD.CLO to '1' to force the BSY and DRQ bits in the P#TFD register to be cleared;
- Software sets P#CMD.ST bit to '1' and set appropriate P#CI bits in order to begin execution of the software reset command.

7.4.1.4 Interrupts

The SATA Controller uses a two-tiered interrupt structure defined in the AHCI specification. The following figure shows the SATA Controller Interrupt Tiers.

Figure 19. SATA Controller Interrupt Tiers



7.4.1.4.1 First Tier (IS Register)

The IS and GHC registers identify the first tier. GHC.IE bit enables interrupts for the entire

SATA Controller: When it is cleared, intrq output is not asserted regardless of any bits set in the IS register. GHC.IE bit acts as a mask and does not affect the setting of any interrupt status bits.

The 32-bit IS register reports whether a port has an interrupt pending. This is a bit-mapped register indicating a bit for each of the implemented ports in the SATA Controller. When a port has one or more interrupt status bits set and the enables for those bits are also set, then the IS bit corresponding to this port is set.

7.4.1.4.2 Second Tier (P#IS Registers)

The second tier is identified in each port through the P#IS (status) and P#IE (interrupt enable) register. The P#IS register has various interrupt bits that can be individually enabled or disabled by setting the corresponding bit in the P#IE. The status bit in the P#IS is always set regardless of the setting of the corresponding P#IE bit.

7.4.1.5 PHY and Link Control

The BISTCR.LLC field (BISTCR is located in the GCSR module) controls the Port Link Layer features (scrambler, descrambler, and repeat drop) and can be disabled in normal operation, such as for testing purposes, by clearing the corresponding bits. The required port is selected using TESTR.PSEL register.

BISTCR.LLC bits are set on power up enabling scrambler, descrambler, RPD functions by default. To disable these functions, software must perform the following steps:

1. Set P#SCTL.DET to 1h.
2. Clear the required BISTCR.LLC bits.

3. Clear P#SCTL.DET to 0.

7.4.1.6 Reset Conditions

7.4.1.6.1 System Reset

System bus resets SATA Controller by asserting asynchronous bus reset. It is usually initiated on power-up or during system bus failure. All components of the SATA Controller are initialized, including ports, generic registers, and BIU.

7.4.1.6.2 Global Reset

Software may globally reset SATA Controller by setting GH C.H R to '1'. When software sets the GHCHR bit to '1', the SATA Controller performs an internal reset action; then clears this bit to '0' when the reset is complete. A software write of '0' to GH C.H R has no effect.

Note: This reset clears the field P#SCTL.SPD. All port communication is restarted with the maximum allowable speed.

To perform the global reset, software sets GH C.H R to '1' and may poll until this bit is read to be '0', indicating the reset completion. The steps for initializing the SATA Controller are as follows:

1. GHC.AE, GHC.IE, the IS register and all port register fields (except P#FB/P#FBU/ P#CLB/P#CLBU) that are not H wInit in the register memory space are reset
2. All other global registers/bits and any HwInit bits in the port-specific registers are not affected by setting GH C.H R to '1'
3. The port-specific registers P#FB, P#FBU, P#CLB, P#CLBU are not affected by setting GH C.H R to '1'
4. P#CMD.SUD bit is reset to '0';software is responsible for setting the P#CMD.SUD and P#SCTL.DET fields appropriately such that communication can be established on the SATA link.

7.4.1.6.3 Port Reset (COMRESET)

Software causes a Port reset by writing 1h to the P#SCTL.DET field to invoke COMRESET on the interface and start a re-establishment of the PHY Layer communication. Software should wait at least 1ms before clearing P#SCTL.DET to 0h; this ensures that at least one COMRESET signal is sent over the interface. After clearing P#SCTL.DET to 0h, software should wait for communication to be re-established as indicated by bit 0 of P#SSTS.DET being set to '1'. Then software should write all ones to the P#SERR register to clear any bits that were set as part of the Port reset.

7.4.1.6.4 Software Reset

Software builds two H 2D Register FISes in the command list. The first Register FIS has the SRST bit set to '1' in the Control field of the Register FIS. The 'C' bit is cleared to '0' in the Register FIS, and the command table has the CH [R] (reset) and CH [C] (clear BSY on R_OK) bits set to '1'. The CH [R] (reset) bit causes the port to perform a SYN C escape when necessary to put the device into an idle condition before sending the software reset. The CH[C] (clear BSY on R_OK) bit needs to be set for the first Register FIS to clear the BSY bit and proceed to issue the next Register FIS since the device does not send a response to the first Register FIS in a software reset sequence. The second Register FIS has SRST='0' in the Control field of the Register FIS, the 'C' bit is cleared to '0' in the Register FIS, and the command table has the CH [R] (reset) and CH [C] (clear BSY on R_OK) bits cleared to '0'. When issuing a software reset sequence, there should not be other commands in the command list. Before issuing the software reset, software must clear P#CMD.ST, wait for the port to be idle (P#CMD.CR='0'), and

then re-set P#CMD.ST. P#TFD.STS.BSY and P#TFD.STS.DRQ must be cleared prior to issuing the reset. When P#TFD.STS.BSY or P#TFD.STS.DRQ is still set based on the failed command, then a Port reset should be attempted or command list override (P#CMD.CLO) should be used.

Note: A Port reset (COMRESET) is the preferred mechanism for error recovery and should be used in place of software reset.

7.4.1.7 Interface Speed Support

The SATA Controller supports both 1.5-Gbps (Gen1) and 3-Gbps (Gen2) interface speeds as indicated by the CAP.ISS=2h.

Software can limit a port's speed to 1.5 Gbps by setting P#SCTL.SPD field to 1h.

7.4.1.8 Staggered Spin-up

The SATA Controller supports staggered spin-up operation when CAP.SSS='1'. This feature is used to individually spin-up attached devices, thus reducing power supply requirements for multiple devices power-up.

Note: In order for a system to support staggered spin-up, the devices and BIOS/driver software must also support.

The P#CMD.SUD bit is used to manipulate the PHY behavior. P#SCTL.DET and P#CMD.SUD must be set correctly in order to avoid illegal combinations of the two values.

The following table describes interaction between the P#CMD.SUD and P#SCTL.DET bits.

Table 179. Interaction Between P#CMD.SUD and P#SCTL.DET Bits

P#SCTL.DET	P#CMD.SUD	Mode	Behavior
0h	0	Listen	Interface is in a reduced power state. When COMINIT is received then P#SERR.DIAG_X is set and no response (OOB signal) is sent to the device. COMWAKE is ignored. The application must place the port into this state only when no device is detected as connected to this port. In this mode, the port forces the PHY into a low power state without requesting a SLUMBER transition on the link.
0h	0 -> 1	Spin-Up	Port sends COMRESET, begins initialization sequence.
0h	1	Normal	Normal operating state when the port is performing data transfers.
1h	0	Illegal	This combination is prohibited in hardware, i.e. P#CMD.SUD can not be cleared when P#SCTL.DET=1h, and P#SCTL.DET can not be set to 1h when P#CMD.SUD=0.
1h	1	Reset	Port continuously transmits COMRESET and does not listen for COMINIT. When COMINIT is received in this state, the P#SERR.DIAG_X bit is set.
1h -> 0h	1	Initialize	Port stops sending COMRESET, begins initialization sequence.
4h	NA	Off	Port PHY is off.

Software must only clear P#CMD.SUD, when it believes that no device is attached. In Listen Mode (P#SCTL.DET=0h and P#CMD.SUD=0), the Port PHY enters a reduced power state, equivalent to the SLUMBER power management state. The Port PHY enters this state without negotiating a transition to SLUMBER on the link, as asking for a transition to SLUMBER when no device is attached fails, and therefore the PHY remains in a high power state. To avoid this, software should ensure that P#SSTS.DET=0h indicating that no device is present before clearing P#CMD.SUD.

7.4.1.9 Activity LED

The CAP.SAL=1 indicates that the activity LED feature is enabled to software. P#_act_led output is used to drive an external LED based upon the activity of the port:

- 1 - LED On (Port active)
- 0 - LED Off (Port inactive)

The port drives the LED active (p#_act_led=1) if:

- (P#CI != 0h or P#SACT != 0h) and P#CMD.ATAPI = 0;
- (P#CI != 0h or P#SACT != 0h) and P#CMD.ATAPI = 1 and P#CMD.DLAE = 1.

The port drives the LED off (p#_act_led='0') when P#CI and P#SACT are both cleared to 0h.

7.4.1.10 Asynchronous Notification

The SATA Controller supports asynchronous notification feature as indicated by the CAP.SSNT=1. This feature allows an ATAPI device to send a signal to the host when media is inserted or removed and avoids polling the device for media changes. The signal sent to the host is a Set Device Bits FIS with the 'I' (interrupt) and 'N' (notification) bits set to 1.

To use asynchronous notification, software should set the P#IS.SDBS bit to enable interrupt notification on a Set Device Bits FIS. When accesses to the ATAPI device are idle, software should place the device in a low power state. When the device has a media change, it signals this to the SATA Controller Port with a Set Device Bits FIS. In response to receiving a P#IS.SDBS interrupt on an idle port, the software should interrogate the device to determine the cause of the interrupt.

The first DWORD of any FIS received by the host contains a 4-bit Port Multiplier Port (PM Port) field. The second DWORD of the BIST Activate FIS least significant byte (bits [7:0]) is stored in the BISTAFR.N CP field. The PM Port field indicates which port/target behind the Port Multiplier issued the FIS to the SATA Controller Port. When a Set Device Bits FIS is received by the SATA Controller Port and the 'N' (notification) bit is set, the bit position in the P#SNTF register corresponding to the PM Port field is set. The SATA Controller Port sets the P#IS.SDBS to 1 when the 'I' (interrupt) bit is set in the Set Device Bits FIS. This causes an interrupt to be generated when that interrupt is enabled.

Note: When a Port Multiplier is not present, the PM Port field in the Set Device Bits FIS is 0h, causing bit 0 of the P#SNTF register to be set.

7.4.1.11 BIST Operation

Each SATA Controller Port can be put into one of the BIST loopback modes described in the following subsections

Note: When the bits BISTCR.LLC SCRAM and DESCRAM prior to entering BIST mode, the Scrambler and Descrambler are bypassed (disabled) in the Port Link layer in all BIST modes, by default.

7.4.1.11.1 Loopback Responder

Software must ensure that the port is in idle state and there are no outstanding commands by checking whether the P#CI and P#SACT registers are both cleared, and the P#TFD.STS register BSY, DRQ and ERR bits are all cleared.

The SATA controller supports the following loopback responder modes:

- Far-end retimes
  - The port receives BIST Activate FIS with Pattern Definition field (bits [23:16] of the first DWORD) = 10h from the RxFIFO and stores it in the BISTAFR.PD field..
  - All the data received from the device in the form of a SATA-compliant pattern is retimed in the Link Layer and transmitted back to the device.
  - Alternately, this mode can be initiated with device disconnected from the Port PHY (Link is in N OCOMM state) when software writes BISTCR.FERLB=1. After the device is connected to the SATA Controller, the device must transmit the number of ALIGN s required for the PHY to sync.
- Far-end analog (Port PHY must support this mode)
  - The port receives BIST Activate FIS with Pattern Definition field (bits [23:16] of the first DWORD) = 08h from the RxFIFO and stores it in the BISTAFR.PD field
  - The port asserts p#_phy_farafelb signal to the PHY to put it to the Far-end analog loopback mode. The PHY receives and retransmits the raw data without retiming
- Far-end transmit only
  - The Port receives BIST Activate FIS with Pattern Definition field (bits [23:16] of the first DWORD) = 80h (scrambling is enabled) or A0h (scrambling is bypassed) from the RxFIFO. The port stores it in the BISTAFR.PD. The second DWORD of the BIST Activate FIS least significant byte (bits [7:0]) is stored in the BISTAFR.N CP field.
  - The port transmits a SATA non-compliant test pattern to the device based on the BISTAFR.N CP value:
    - F1h: Low Transition Density Pattern (LTDP)
    - B5h: High Transition Density Pattern (HTDP)
    - ABh: Low Frequency Spectral Component Pattern (LFSCP)
    - 7Fh: Simultaneous Switching Outputs Pattern (SSOP)
    - 8Bh: Lone Bit Pattern (LBP)
    - 78h: Mid Frequency Test Pattern (MFTP)
    - 4Ah: High Frequency Test Pattern (H FTP)
    - 7Eh: Low Frequency Test Pattern (LFTP)
    - Alternately, this mode can be initiated with device disconnected from the Port PHY (Link NOCOMM state), when software writes a one to the BISTCR.TXO bit. SATA Controller transmits non-compliant BIST pattern defined by the value in the BISTCR.PATTERN field.

Loopback responder BIST modes can be exited either when the device signals COMINIT OOB condition, or when the software initiates Port reset (COMRESET).

7.4.1.11.2 Loopback Initiator

The software first selects the port for BIST operation by writing the Port number to the TESTR.PSEL field, then the required pattern by writing to the BISTCR.PATTERN field.