32-Bit, 10 kSPS, Sigma-Delta ADC with 100 µs Settling and True Rail-to-Rail Buffers

Data Sheet **AD7177-2**

FEATURES

- 32-bit data output
- Fast and flexible output rate: 5 SPS to 10 kSPS
- Channel scan data rate of 10 kSPS/channel (100 µs settling)
- Performance specifications
  - 19.1 noise free bits at 10 kSPS
  - 20.2 noise free bits at 2.5 kSPS
  - 24.6 noise free bits at 5 SPS
  - INL: ±1 ppm of FSR
- 85 dB filter rejection of 50 Hz and 60 Hz with 50 ms settling
- User configurable input channels
  - 2 fully differential channels or 4 single-ended channels
  - Crosspoint multiplexer
- On-chip 2.5 V reference (±2 ppm/°C drift)
- True rail-to-rail analog and reference input buffers
- Internal or external clock
- Power supply: AVDD1 − AVSS = 5 V, AVDD2 = IOVDD = 2.5 V to 5 V
  - Split supply with AVDD1/AVSS at ±2.5 V
- ADC current: 8.4 mA
- Temperature range: −40°C to +105°C
- 3- or 4-wire serial digital interface (Schmitt trigger on SCLK)
  - Serial port interface (SPI), QSPI, MICROWIRE, and DSP compatible

APPLICATIONS

- Process control: PLC/DCS modules
- Temperature and pressure measurement
- Medical and scientific multichannel instrumentation
- Chromatography

GENERAL DESCRIPTION

The AD7177-2 is a 32-bit low noise, fast settling, multiplexed, 2-/4-channel (fully/pseudo differential) Σ-Δ analog-to-digital converter (ADC) for low bandwidth inputs. It has a maximum channel scan rate of 10 kSPS (100 µs) for fully settled data. The output data rates range from 5 SPS to 10 kSPS.

The AD7177-2 integrates key analog and digital signal conditioning blocks to allow users to configure an individual setup for each analog input channel in use. Each feature can be user selected on a per channel basis. Integrated true rail-to-rail buffers on the analog inputs and external reference inputs provide easy to drive high impedance inputs. The precision 2.5 V low drift (2 ppm/°C) band gap internal reference (with output reference buffer) adds embedded functionality to reduce external component count.

The digital filter allows simultaneous 50 Hz and 60 Hz rejection at a 27.27 SPS output data rate. The user can switch between different filter options according to the demands of each channel in the application. The ADC automatically switches through each selected channel. Further digital processing functions include offset and gain calibration registers, configurable on a per channel basis.

The device operates with a 5 V AVDD1 supply, or with ±2.5 V AVDD1/AVSS, and 2 V to 5 V AVDD2 and IOVDD supplies. The specified operating temperature range is −40°C to +105°C. The AD7177-2 is available in a 24-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM

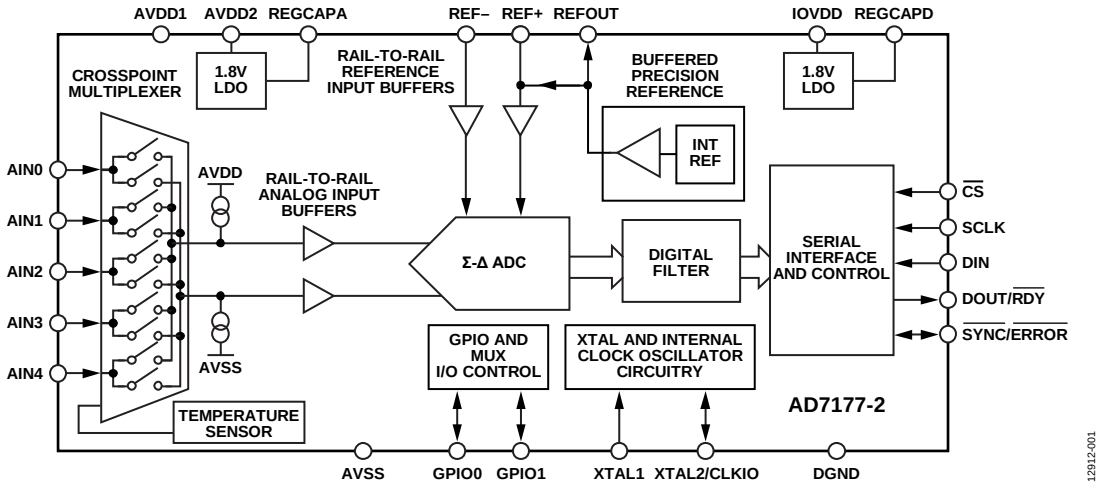

Figure 1.

Rev. B Document Feedback

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