Femtoampere Input Bias Current Electrometer Amplifier

Data Sheet

ADA4530-1

FEATURES

- Low input bias current
  - ±20 fA maximum at T_A = 25°C (guaranteed at production test)
  - ±20 fA maximum at −40°C < T_A < +85°C
  - ±250 fA maximum at −40°C < T_A < +125°C (guaranteed at production test)
- Low offset voltage: 50 µV maximum over specified CMRR range
- Offset voltage drift: ±0.13 µV/°C typical, ±0.5 µV/°C maximum
- Integrated guard buffer with 100 µV maximum offset
- Low voltage noise density: 14 nV/√Hz at 10 kHz
- Wide bandwidth: 2 MHz unity-gain crossover
- Supply voltage: 4.5 V to 16 V (±2.25 V to ±8 V)
- Operating temperature: −40°C to +125°C
- Long-term offset voltage drift (10,000 hours): 0.5 µV typical
- Temperature hysteresis: 1.5 µV typical

APPLICATIONS

- Laboratory and analytical instrumentation: spectrophotometers, chromatographs, mass spectrometers, and potentiostatic and amperostatic coulometry
- Instrumentation: picoammeters and coulombmeters
- Transimpedance amplifier (TIA) for photodiodes, ion chambers, and working electrode measurements
- High impedance buffering for chemical sensors and capacitive sensors

PIN CONNECTION DIAGRAM

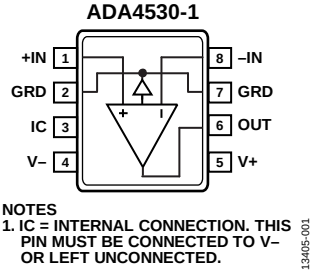

Figure 1.

GENERAL DESCRIPTION

The ADA4530-1 is a femtoampere (10^{-15} A) level input bias current operational amplifier suitable for use as an electrometer that also includes an integrated guard buffer. It has an operating voltage range of 4.5 V to 16 V, enabling it to operate in conventional 5 V and 10 V single supply systems as well as ±2.5 V and ±5 V dual supply systems.

It provides ultralow input bias currents that are production tested at 25°C and at 125°C to ensure the device meets its performance goals in user systems. The integrated guard buffer isolates the input pins from leakage in the printed circuit board (PCB), minimizes board component count, and enables easy system design. The ADA4530-1 is available in an industry-standard surface-mount 8-lead SOIC package with a unique pinout optimized to prevent signals from coupling between the sensitive input pins, the power supplies, and the output pin while enabling easy routing of the guard ring traces.

The ADA4530-1 also offers low offset voltage, low offset drift, and low voltage and current noise needed for the types of applications that require such low leakages.

To maximize the dynamic range of the system, the ADA4530-1 has a rail-to-rail output stage that can typically drive to within 30 mV of the supply rails under a 10 kΩ load.

The ADA4530-1 operates over the −40°C to +125°C industrial temperature range and is available in an 8-lead SOIC package.

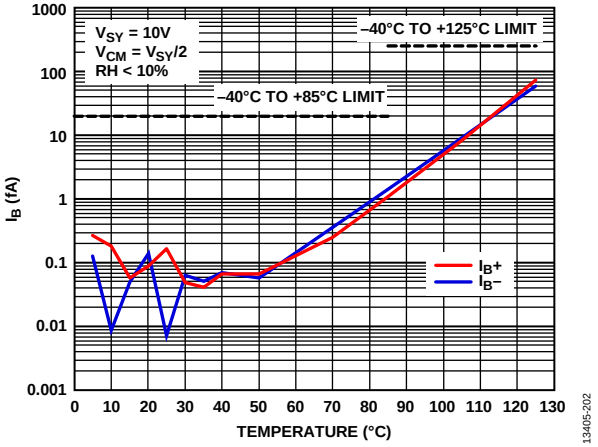

Figure 2. Input Bias Current (I_B) vs. Temperature, V_{SY} = 10 V

Rev. B
Document Feedback

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5/2017—Rev. A to Rev. B

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Moved Figure 114 38
Changes to Current Noise Considerations Section 41
Added Long-Term Drift Section, Temperature Hysteresis Section, Figure 136, Figure 137, and Figure 138; Renumbered Sequentially 51
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3/2016—Rev. 0 to Rev. A

Changed DNC Pin to IC Pin ..... Throughout
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Added Power Supply Recommendations Section, Power Supply Considerations Section, Table 16, and Figure 133 to Figure 135 49

10/2015—Revision 0: Initial Version

SPECIFICATIONS

5 V NOMINAL ELECTRICAL CHARACTERISTICS

Supply voltage (V_{SY}) = 4.5 V, common-mode voltage (V_{CM}) = V_{SY}/2, T_A = 25°C, unless otherwise specified. Typical specifications are equal to the average of the distribution from characterization, unless otherwise noted. Minimum and maximum specifications are tested in production, unless otherwise noted.

Table 1.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Bias Current[2, 3]	I_B	RH < 50%		<1	±20	fA
		−40°C < T_A < +85°C, RH < 50%			±20	fA
		−40°C < T_A < +125°C, RH < 50%			±250	fA
Input Offset Current[3]	I_{OS}	RH < 50%		<1	±20	fA
		−40°C < T_A < +125°C, RH < 50%			±150	fA
Input Offset Voltage[2, 4]	V_{OS}			+8	±40	µV
		V_{CM} = 1.5 V to 3 V		+9	±50	µV
		V_{CM} = 1.5 V to 3 V, 0°C < T_A < 125°C			±70	µV
		V_{CM} = 1.5 V to 3 V, −40°C < T_A < 0°C			±150	µV
		V_{CM} = 0 V to 3 V			±300	µV
Offset Voltage Drift[2, 4]	$\Delta V_{OS}/\Delta T$	0°C < T_A < 125°C		+0.13	±0.5	µV/°C
		−40°C < T_A < 0°C		−0.7	±2.8	µV/°C
Input Voltage Range	IVR		0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.5 V to 3 V	92	114		dB
		−40°C < T_A < +125°C	90			dB
		V_{CM} = 0 V to 3 V	73			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ to V_{CM}, V_{OUT} = 0.2 V to 4.3 V	120	143		dB
		−40°C < T_A < +125°C	120			dB
Input Resistance	R_{IN}	−40°C < T_A < +125°C		>100		TΩ
Input Capacitance	C_{IN}			8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.47	4.49		V
		−40°C < T_A < +125°C	4.46			V
		R_L = 2 kΩ to V_{CM}	4.4	4.45		V
		−40°C < T_A < +125°C	4.38			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		10	30	mV
		−40°C < T_A < +125°C			40	mV
		R_L = 2 kΩ to V_{CM}		30	100	mV
		−40°C < T_A < +125°C			120	mV
Short-Circuit Current	I_{SC}					
Source				15		mA
Sink				−30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		20		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4.5 V to 16 V	130	150		dB
		−40°C < T_A < +125°C	130			dB
Supply Current	I_{SY}	I_{OUT} = 0 mA		0.9	1.3	mA
		−40°C < T_A < +125°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 10 pF, A_V = 1		1.4		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		2		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		2		MHz

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN}=10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		6		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		62		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 0.5 V step, R_L = 10 kΩ, C_L= 10 pF, A_V = −1		5		µs
EMI Rejection Ratio of +IN	EMIRR	V_{IN} = 100 mV peak, f = 400 MHz		50		dB
		V_{IN} = 100 mV peak, f = 900 MHz		60		dB
		V_{IN} = 100 mV peak, f = 1800 MHz		80		dB
		V_{IN} = 100 mV peak, f = 2400 MHz		90		dB
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		80		nV/√Hz
		f = 1 kHz		16		nV/√Hz
		f = 10 kHz		14		nV/√Hz
Current Noise Density	I_N	f = 0.1 Hz		0.07		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 1 kHz, V_{IN} = 0.5 V rms				
Bandwidth = 90 kHz				0.003		%
Bandwidth = 500 kHz				0.0045		%
GUARD BUFFER						
Guard Offset Voltage[2, 4, 5]	V_{GOS}	V_{CM} = 1.5 V to 3 V		15	100	µV
		V_{CM} = 1.5 V to 3 V, 0°C < T_A < 125°C			120	µV
		V_{CM} = 1.5 V to 3 V, −40°C < T_A < 0°C			250	µV
		V_{CM} = 0.1 V to 3 V			150	µV
Guard Offset Voltage Drift[2, 4]	$\Delta V_{GOS}/\Delta T$	0°C < T_A < +125°C		0.18	1	µV/°C
		−40°C < T_A < 0°C		1.4	7	µV/°C
Output Impedance	Z_{GOUT}			1		kΩ
Output Voltage Range		V_{GOS} < 150 µV	0.1		3	V
−3 dB Bandwidth	$f_{-3dBGUARD}$	V_{IN} = 10 mV rms, C_L = 10 pF		5.5		MHz

[1] These specifications represent the performance for 5 V ± 10% power supplies. All specifications are measured at the worst case 4.5 V supply voltage.
[2] The maximum specifications at −40°C < T_A < +85°C and −40°C < T_A < 0°C are guaranteed from characterization.
[3] RH is relative humidity (see the Humidity Effects section for more information).
[4] The typical specifications are equal to the average plus the standard deviation of the distribution from characterization.
[5] The guard offset voltage is the voltage difference between the guard output and the noninverting input.