

MKE02P64M40SF0

KE02 Sub-Family Data Sheet

Supports the following:

MKE02Z16VLC4(R),
MKE02Z32VLC4(R),
MKE02Z64VLC4(R),
MKE02Z16VLD4(R),
MKE02Z32VLD4(R),
MKE02Z64VLD4(R),
MKE02Z32VLH4(R),
MKE02Z64VLH4(R),
MKE02Z32VQH4(R),
MKE02Z64VQH4(R),
MKE02Z16VFM4(R),
MKE02Z32VFM4(R), and
MKE02Z64VFM4(R)

Key features

- Operating characteristics
 - Voltage range: 2.7 to 5.5 V
 - Flash write voltage range: 2.7 to 5.5 V
 - Temperature range (ambient): -40 to 105°C
- Performance
 - Up to 40 MHz Arm® Cortex-M0+ core and up to 20 MHz bus clock
 - Single cycle 32-bit x 32-bit multiplier
 - Single cycle I/O access port
- Memories and memory interfaces
 - Up to 64 KB flash
 - Up to 256 B EEPROM
 - Up to 4 KB RAM
- Clocks
 - Oscillator (OSC) - supports 32.768 kHz crystal or 4 MHz to 20 MHz crystal or ceramic resonator; choice of low power or high gain oscillators
 - Internal clock source (ICS) - internal FLL with internal or external reference, 31.25 kHz pre-trimmed internal reference for 32 MHz system clock (able to be trimmed for up to 40 MHz system clock)
 - Internal 1 kHz low-power oscillator (LPO)
- System peripherals
 - Power management module (PMC) with three power modes: Run, Wait, Stop
 - Low-voltage detection (LVD) with reset or interrupt, selectable trip points
 - Watchdog with independent clock source (WDOG)
 - Programmable cyclic redundancy check module (CRC)
 - Serial wire debug interface (SWD)
 - Bit manipulation engine (BME)
- Security and integrity modules
 - 64-bit unique identification (ID) number per chip
- Human-machine interface
 - Up to 57 general-purpose input/output (GPIO)
 - Two up to 8-bit keyboard interrupt modules (KBI)
 - External interrupt (IRQ)
- Analog modules
 - One up to 16-channel 12-bit SAR ADC, operation in Stop mode, optional hardware trigger (ADC)
 - Two analog comparators containing a 6-bit DAC and programmable reference input (ACMP)



- Timers
 - One 6-channel FlexTimer/PWM (FTM)
 - Two 2-channel FlexTimer/PWM (FTM)
 - One 2-channel periodic interrupt timer (PIT)
 - One real-time clock (RTC)
- Communication interfaces
 - Two SPI modules (SPI)
 - Up to three UART modules (UART)
 - One I2C module (I2C)
- Package options
 - 64-pin QFP/LQFP
 - 44-pin LQFP
 - 32-pin LQFP
 - 32-pin QFN

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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: KE02Z.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|-------|---------------------------|--|
| Q | Qualification status | <ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification |
| KE## | Kinetis family | <ul style="list-style-type: none"> KE02 |
| A | Key attribute | <ul style="list-style-type: none"> Z = M0+ core |
| FFF | Program flash memory size | <ul style="list-style-type: none"> 16 = 16 KB 32 = 32 KB 64 = 64 KB |
| R | Silicon revision | <ul style="list-style-type: none"> (Blank) = Main A = Revision after main |

Table continues on the next page...

| Field | Description | Values |
|-------|-----------------------------|--|
| T | Temperature range (°C) | <ul style="list-style-type: none"> • V = -40 to 105 |
| PP | Package identifier | <ul style="list-style-type: none"> • LC = 32 LQFP (7 mm x 7 mm) • FM = 32 QFN (5 mm x 5 mm) • LD = 44 LQFP (10 mm x 10 mm) • QH = 64 QFP (14 mm x 14 mm) • LH = 64 LQFP (10 mm x 10 mm) |
| CC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> • 4 = 40 MHz |
| N | Packaging type | <ul style="list-style-type: none"> • R = Tape and reel • (Blank) = Trays |

2.4 Example

This is an example part number:

MKE02Z64VQH4

3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter classifications

| | |
|---|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T _{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T _{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V _{HBM} | Electrostatic discharge voltage, human body model | -6000 | +6000 | V | 1 |
| V _{CDM} | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| I _{LAT} | Latch-up current at ambient temperature of 125°C | -100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, *IC Latch-up Test*.
 - Test was performed at 125 °C case temperature (Class II).
 - I/O pins pass ±100 mA I-test with I_{DD} current limit at 800 mA.
 - I/O pins pass +60/-100 mA I-test with I_{DD} current limit at 1000 mA.
 - Supply groups pass 1.5 V_{ccmax}.
 - RESET pin was only tested with negative I-test due to product conditioning requirement.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 2. Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|-----------|---|----------------|-----------------------------|------|
| V_{DD} | Digital supply voltage | -0.3 | 6.0 | V |
| I_{DD} | Maximum current into V_{DD} | — | 120 | mA |
| V_{IN} | Input voltage except true open drain pins | -0.3 | $V_{DD} + 0.3$ ¹ | V |
| | Input voltage of true open drain pins | -0.3 | 6 | V |
| I_D | Instantaneous maximum current single pin limit (applies to all port pins) | -25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |

1. Maximum rating of V_{DD} also applies to V_{IN} .

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 3. DC characteristics

| Symbol | C | Descriptions | Min | Typical ¹ | Max | Unit |
|--------|---|--------------------------------|-----|----------------------|-----|------|
| — | — | Operating voltage ² | 2.7 | — | 5.5 | V |

Table continues on the next page...

Table 3. DC characteristics (continued)

| Symbol | C | Descriptions | | Min | Typical ¹ | Max | Unit | |
|------------------------------|---|--|--|---|------------------------|-----|------------------------|----|
| V _{OH} | P | Output high voltage | All I/O pins, except PTA2 and PTA3, standard-drive strength | 5 V, I _{load} = -5 mA | V _{DD} - 0.8 | — | — | V |
| | C | | | 3 V, I _{load} = -2.5 mA | V _{DD} - 0.8 | — | — | V |
| | P | | High current drive pins, high-drive strength ³ | 5 V, I _{load} = -20 mA | V _{DD} - 0.8 | — | — | V |
| | C | | | 3 V, I _{load} = -10 mA | V _{DD} - 0.8 | — | — | V |
| I _{OHT} | D | Output high current | Max total I _{OH} for all ports | 5 V | — | — | -100 | mA |
| | | | | 3 V | — | — | -60 | |
| V _{OL} | P | Output low voltage | All I/O pins, standard-drive strength | 5 V, I _{load} = 5 mA | — | — | 0.8 | V |
| | C | | | 3 V, I _{load} = 2.5 mA | — | — | 0.8 | V |
| | P | | High current drive pins, high-drive strength ³ | 5 V, I _{load} = 20 mA | — | — | 0.8 | V |
| | C | | | 3 V, I _{load} = 10 mA | — | — | 0.8 | V |
| I _{OLT} | D | Output low current | Max total I _{OL} for all ports | 5 V | — | — | 100 | mA |
| | | | | 3 V | — | — | 60 | |
| V _{IH} | P | Input high voltage | All digital inputs | 4.5 ≤ V _{DD} < 5.5 V | 0.65 × V _{DD} | — | — | V |
| | | | | 2.7 ≤ V _{DD} < 4.5 V | 0.70 × V _{DD} | — | — | |
| V _{IL} | P | Input low voltage | All digital inputs | 4.5 ≤ V _{DD} < 5.5 V | — | — | 0.35 × V _{DD} | V |
| | | | | 2.7 ≤ V _{DD} < 4.5 V | — | — | 0.30 × V _{DD} | |
| V _{hys} | C | Input hysteresis | All digital inputs | — | 0.06 × V _{DD} | — | — | mV |
| I _{IN} | P | Input leakage current | Per pin (pins in high impedance input mode) | V _{IN} = V _{DD} or V _{SS} | — | 0.1 | 1 | μA |
| I _{INTOT} | C | Total leakage combined for all port pins | Pins in high impedance input mode | V _{IN} = V _{DD} or V _{SS} | — | — | 2 | μA |
| R _{PU} | P | Pullup resistors | All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3) | — | 30.0 | — | 50.0 | kΩ |
| R _{PU} ⁴ | P | Pullup resistors | PTA2 and PTA3 pins | — | 30.0 | — | 60.0 | kΩ |
| I _{IC} | D | DC injection current ^{5, 6, 7} | Single pin limit | V _{IN} < V _{SS} , V _{IN} > V _{DD} | -2 | — | 2 | mA |
| | | | Total MCU limit, includes sum of all stressed pins | | -5 | — | 25 | |
| C _{in} | C | Input capacitance, all pins | | — | — | — | 7 | pF |
| V _{RAM} | C | RAM retention voltage | | — | 2.0 | — | — | V |

1. Typical values are measured at 25 °C. Characterized, not tested.
 2. Maximum power supply VDD ramp-up rate is 70V/ms, characterized on samples of different lots.

- Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support high current output.
- The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
- All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD} . PTA2 and PTA3 are true open drain I/O pins that are internally clamped to V_{SS} .
- Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
- Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{in} > V_{DD}$) is higher than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 4. LVD and POR specification

| Symbol | C | Description | Min | Typ | Max | Unit | |
|-------------|---|---|-----------------------------|------|------|------|---|
| V_{POR} | D | POR re-arm voltage ¹ | 1.5 | 1.75 | 2.0 | V | |
| V_{LVDH} | C | Falling low-voltage detect threshold—high range (LVDV = 1) ² | 4.2 | 4.3 | 4.4 | V | |
| V_{LVW1H} | C | Falling low-voltage warning threshold—high range | Level 1 falling (LVWV = 00) | 4.3 | 4.4 | 4.5 | V |
| V_{LVW2H} | C | | Level 2 falling (LVWV = 01) | 4.5 | 4.5 | 4.6 | V |
| V_{LVW3H} | C | | Level 3 falling (LVWV = 10) | 4.6 | 4.6 | 4.7 | V |
| V_{LVW4H} | C | | Level 4 falling (LVWV = 11) | 4.7 | 4.7 | 4.8 | V |
| V_{HYSH} | C | High range low-voltage detect/warning hysteresis | — | 100 | — | mV | |
| V_{LVDL} | C | Falling low-voltage detect threshold—low range (LVDV = 0) | 2.56 | 2.61 | 2.66 | V | |
| V_{LVW1L} | C | Falling low-voltage warning threshold—low range | Level 1 falling (LVWV = 00) | 2.62 | 2.7 | 2.78 | V |
| V_{LVW2L} | C | | Level 2 falling (LVWV = 01) | 2.72 | 2.8 | 2.88 | V |
| V_{LVW3L} | C | | Level 3 falling (LVWV = 10) | 2.82 | 2.9 | 2.98 | V |
| V_{LVW4L} | C | | Level 4 falling (LVWV = 11) | 2.92 | 3.0 | 3.08 | V |
| V_{HYSDL} | C | Low range low-voltage detect hysteresis | — | 40 | — | mV | |
| V_{HYSWL} | C | Low range low-voltage warning hysteresis | — | 80 | — | mV | |
| V_{BG} | P | Buffered bandgap output ³ | 1.14 | 1.16 | 1.18 | V | |

- Maximum is highest voltage that POR is guaranteed.
- Rising thresholds are falling threshold + hysteresis.
- voltage Factory trimmed at $V_{DD} = 5.0$ V, Temp = 25 °C

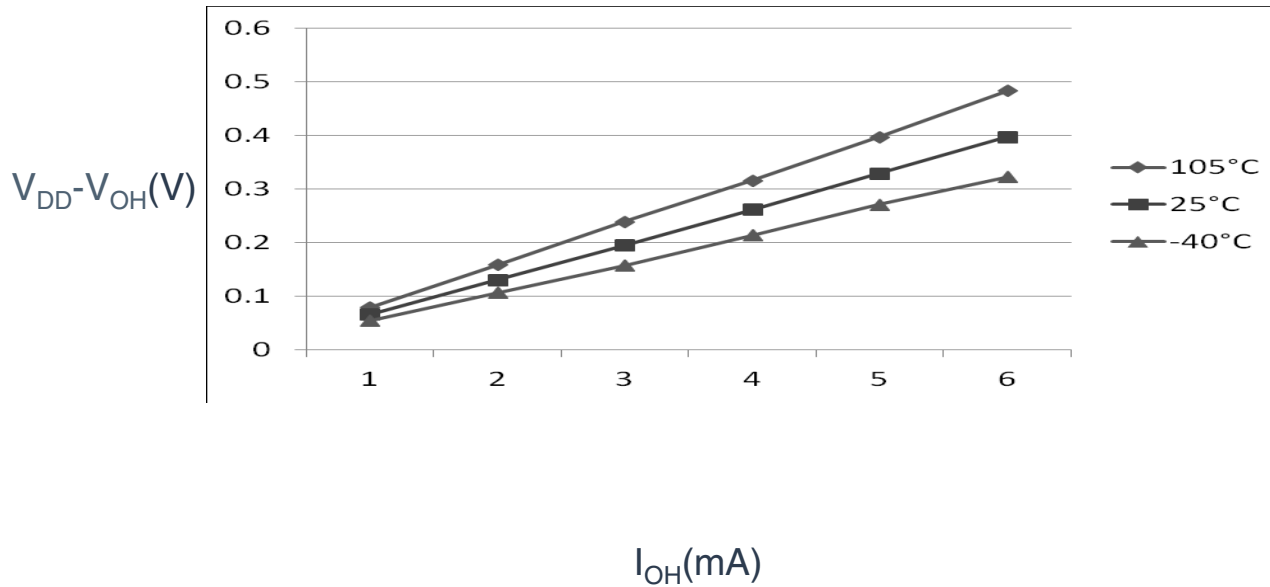


Figure 1. Typical $V_{DD}-V_{OH}$ Vs. I_{OH} (standard drive strength) ($V_{DD} = 5$ V)

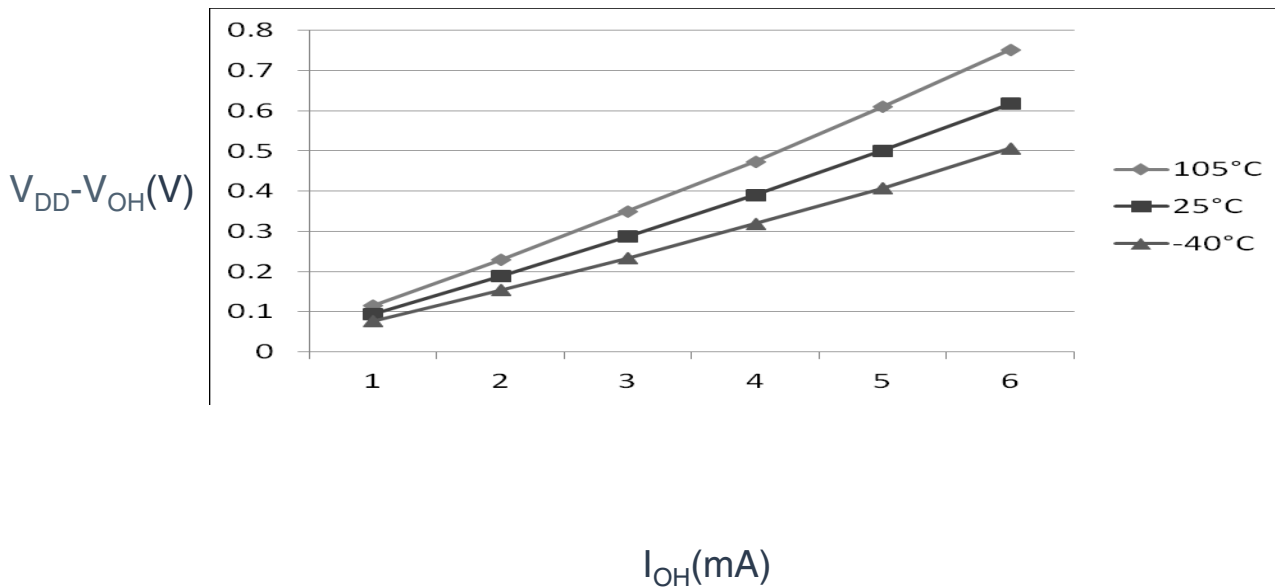


Figure 2. Typical $V_{DD}-V_{OH}$ Vs. I_{OH} (standard drive strength) ($V_{DD} = 3$ V)

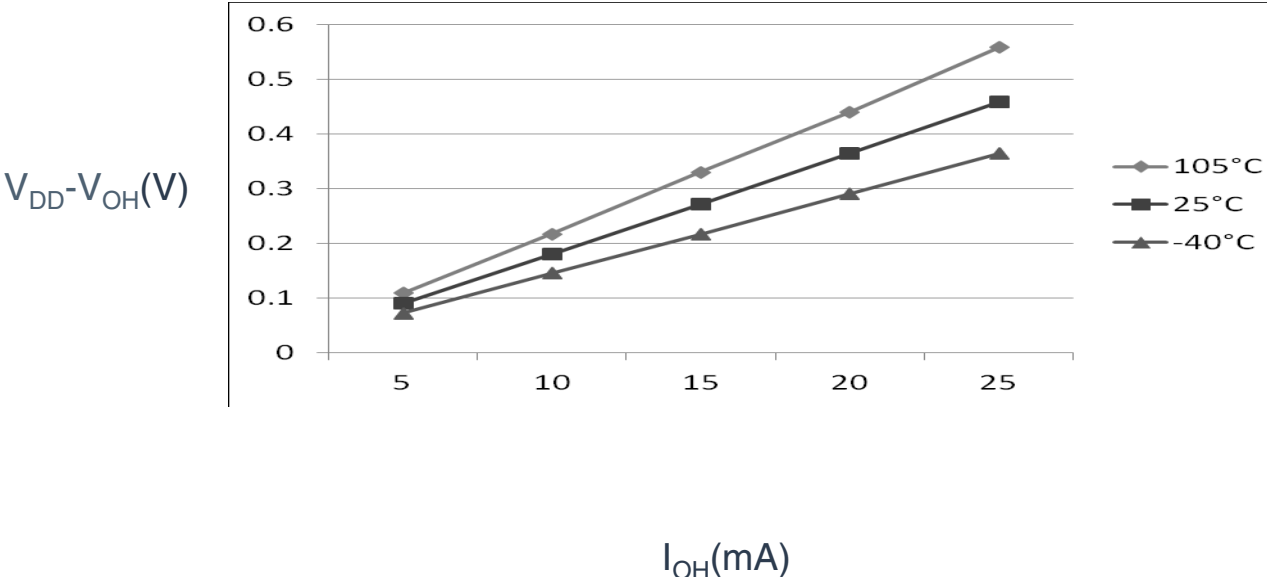


Figure 3. Typical $V_{DD}-V_{OH}$ Vs. I_{OH} (high drive strength) ($V_{DD} = 5V$)

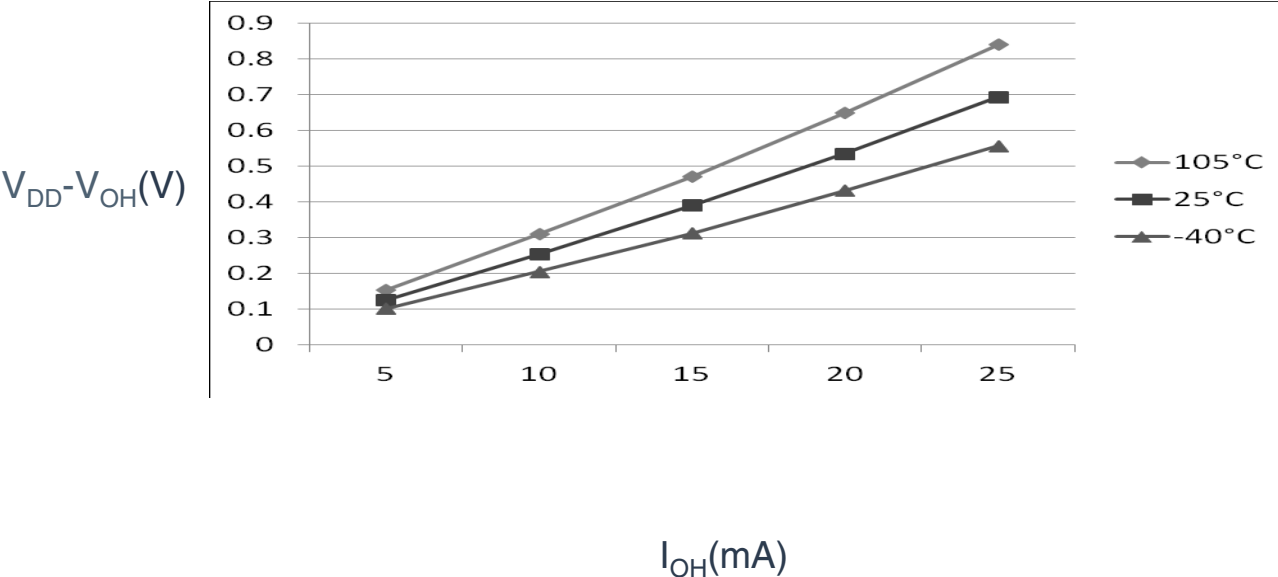


Figure 4. Typical $V_{DD}-V_{OH}$ Vs. I_{OH} (high drive strength) ($V_{DD} = 3V$)

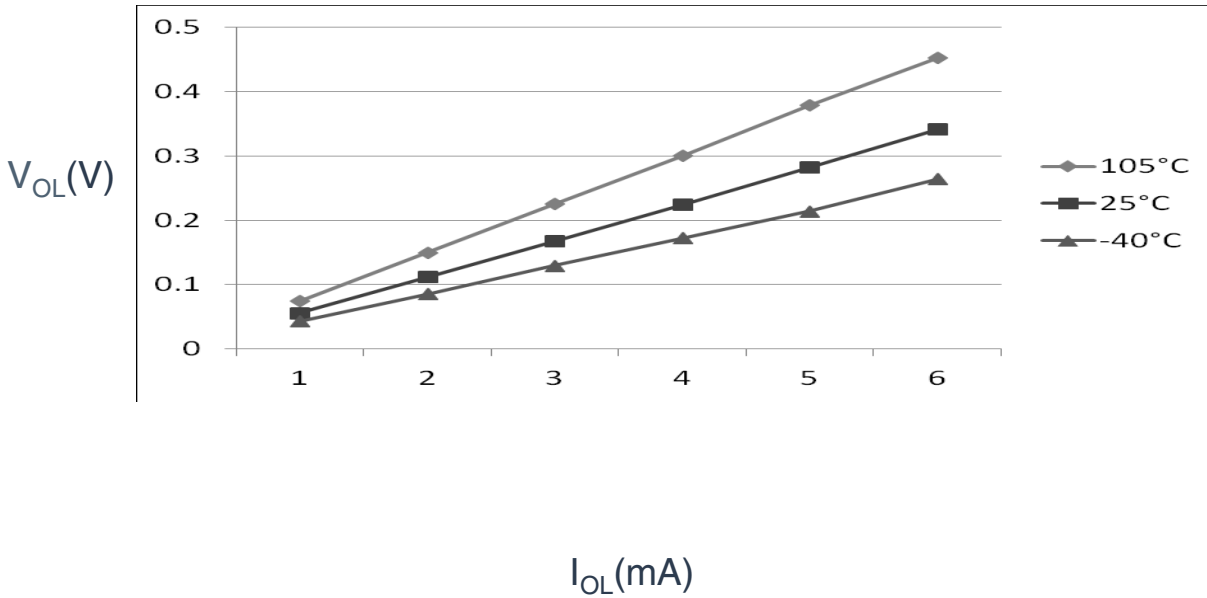


Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 5 V)

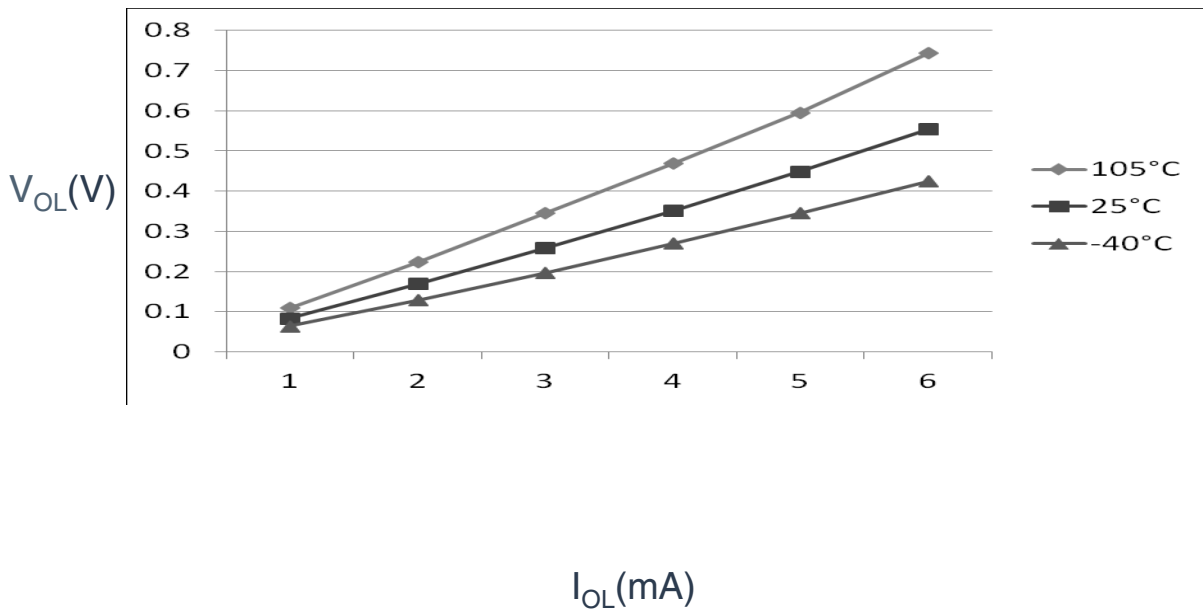


Figure 6. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 3 V)

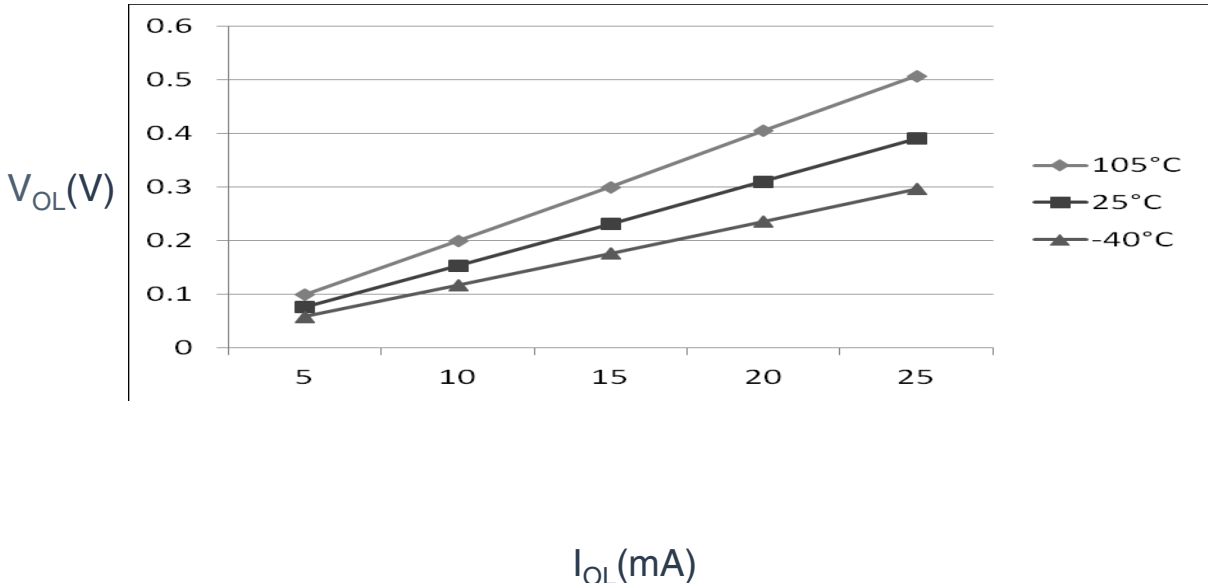


Figure 7. Typical V_{OL} Vs. I_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

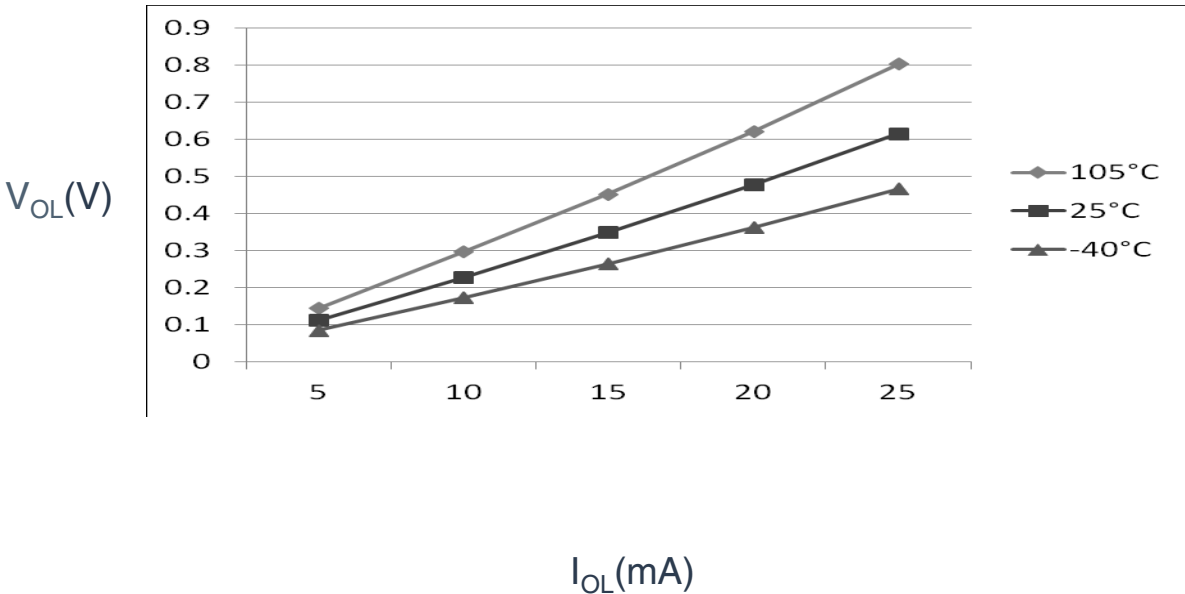


Figure 8. Typical V_{OL} Vs. I_{OL} (high drive strength) ($V_{DD} = 3\text{ V}$)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 5. Supply current characteristics

| C | Parameter | Symbol | Core/Bus Freq | V _{DD} (V) | Typical ¹ | Max ² | Unit | Temp |
|---|--|------------------|---------------|---------------------|----------------------|------------------|------|---------------|
| C | Run supply current FEI mode, all modules clocks enabled; run from flash | R _{IDD} | 40/20 MHz | 5 | 7.8 | — | mA | -40 to 105 °C |
| C | | | 20/20 MHz | | 6.7 | — | | |
| C | | | 10/10 MHz | | 4.5 | — | | |
| C | | | 1/1 MHz | | 1.5 | — | | |
| C | | | 40/20 MHz | 3 | 7.7 | — | | |
| C | | | 20/20 MHz | | 6.6 | — | | |
| C | | | 10/10 MHz | | 4.4 | — | | |
| C | | | 1/1 MHz | | 1.45 | — | | |
| C | Run supply current FEI mode, all modules clocks disabled; run from flash | R _{IDD} | 40/20 MHz | 5 | 6.3 | — | mA | -40 to 105 °C |
| C | | | 20/20 MHz | | 5.3 | — | | |
| C | | | 10/10 MHz | | 3.7 | — | | |
| C | | | 1/1 MHz | | 1.5 | — | | |
| C | | | 40/20 MHz | 3 | 6.2 | — | | |
| C | | | 20/20 MHz | | 5.3 | — | | |
| C | | | 10/10 MHz | | 3.7 | — | | |
| C | | | 1/1 MHz | | 1.4 | — | | |
| C | Run supply current FBE mode, all modules clocks enabled; run from RAM | R _{IDD} | 40/20 MHz | 5 | 10.3 | — | mA | -40 to 105 °C |
| P | | | 20/20 MHz | | 9 | 14.8 | | |
| C | | | 10/10 MHz | | 5.2 | — | | |
| C | | | 1/1 MHz | | 1.45 | — | | |
| C | | | 40/20 MHz | 3 | 10.2 | — | | |
| P | | | 20/20 MHz | | 8.8 | 11.8 | | |
| C | | | 10/10 MHz | | 5.1 | — | | |
| C | | | 1/1 MHz | | 1.4 | — | | |
| C | Run supply current FBE mode, all modules clocks disabled; run from RAM | R _{IDD} | 40/20 MHz | 5 | 8.9 | — | mA | -40 to 105 °C |
| P | | | 20/20 MHz | | 8 | 12.3 | | |
| C | | | 10/10 MHz | | 4.4 | — | | |
| C | | | 1/1 MHz | | 1.35 | — | | |
| C | | | 40/20 MHz | 3 | 8.8 | — | | |
| P | | | 20/20 MHz | | 7.8 | 9.2 | | |
| C | | | 10/10 MHz | | 4.2 | — | | |
| C | | | 1/1 MHz | | 1.3 | — | | |

Table continues on the next page...

Table 5. Supply current characteristics (continued)

| C | Parameter | Symbol | Core/Bus Freq | V _{DD} (V) | Typical ¹ | Max ² | Unit | Temp |
|---|--|------------------|---------------|---------------------|--|------------------|------|---------------|
| C | Wait mode current FEI mode, all modules clocks enabled | W _{IDD} | 40/20 MHz | 5 | 6.4 | — | mA | –40 to 105 °C |
| P | | | 20/20 MHz | | 5.5 | — | | |
| C | | | 20/10 MHz | | 3.5 | — | | |
| C | | | 1/1 MHz | | 1.4 | — | | |
| C | | | 40/20 MHz | 3 | 6.3 | — | | |
| C | | | 20/20 MHz | | 5.4 | — | | |
| C | | | 10/10 MHz | | 3.4 | — | | |
| C | | | 1/1 MHz | | 1.4 | — | | |
| P | Stop mode supply current no clocks active (except 1 kHz LPO clock) ³ | S _{IDD} | — | 5 | 2 | 85 | μA | –40 to 105 °C |
| P | | | — | 3 | 1.9 | 80 | | –40 to 105 °C |
| C | ADC adder to Stop ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B | — | — | 5 | 86 (64-, 44-pin packages) 42 (32-pin package) | — | μA | –40 to 105 °C |
| C | | | | 3 | 82 (64-, 44-pin packages) 41 (32-pin package) | — | | |
| C | ACMP adder to Stop | — | — | 5 | 12 | — | μA | –40 to 105 °C |
| C | | | | 3 | 12 | — | | |
| C | LVD adder to stop ⁴ | — | — | 5 | 128 | — | μA | –40 to 105 °C |
| C | | | | 3 | 124 | — | | |

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The Max current is observed at high temperature of 105 °C.
3. RTC adder causes I_{DD} to increase typically by less than 1 μA; RTC clock source is 1 kHz LPO clock.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following applications notes, available on nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers

Switching specifications

- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.1.3.1 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors for 64-pin QFP package

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---------------------|------------------------------------|----------------------|------|------------|-------|
| V _{RE1} | Radiated emissions voltage, band 1 | 0.15–50 | 14 | dB μ V | 1, 2 |
| V _{RE2} | Radiated emissions voltage, band 2 | 50–150 | 15 | dB μ V | |
| V _{RE3} | Radiated emissions voltage, band 3 | 150–500 | 3 | dB μ V | |
| V _{RE4} | Radiated emissions voltage, band 4 | 500–1000 | 4 | dB μ V | |
| V _{RE_IEC} | IEC level | 0.15–1000 | M | — | 2, 3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 5.0 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{BUS} = 20 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2 Switching specifications

5.2.1 Control timing

Table 7. Control timing

| Num | C | Rating | | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|--------------------------------|---------------------|------------------------|----------------------|------|------|
| 1 | D | System and core clock | | f _{Sys} | DC | — | 40 | MHz |
| 2 | P | Bus frequency (t _{cyc} = 1/f _{Bus}) | | f _{Bus} | DC | — | 20 | MHz |
| 3 | P | Internal low power oscillator frequency | | f _{LPO} | 0.67 | 1.0 | 1.25 | KHz |
| 4 | D | External reset pulse width ² | | t _{extrst} | 1.5 × t _{cyc} | — | — | ns |
| 5 | D | Reset low drive | | t _{rstdrv} | 34 × t _{cyc} | — | — | ns |
| 6 | D | IRQ pulse width | Asynchronous path ² | t _{LIH} | 100 | — | — | ns |
| | D | | Synchronous path ³ | t _{IHIL} | 1.5 × t _{cyc} | — | — | ns |

Table continues on the next page...

Table 7. Control timing (continued)

| Num | C | Rating | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|---|--------------------------------|------------|----------------------|------|------|
| 7 | D | Keyboard interrupt pulse width | Asynchronous path ² | t_{LIH} | 100 | — | ns |
| | D | | Synchronous path | t_{HIL} | $1.5 \times t_{cyc}$ | — | ns |
| 8 | C | Port rise and fall time - Normal drive strength (load = 50 pF) ⁴ | — | t_{Rise} | — | 10.2 | ns |
| | C | | — | t_{Fall} | — | 9.5 | ns |
| | C | Port rise and fall time - high drive strength (load = 50 pF) ⁴ | — | t_{Rise} | — | 5.4 | ns |
| | C | | — | t_{Fall} | — | 4.6 | ns |

1. Typical values are based on characterization data at $V_{DD} = 5.0\text{ V}$, $25\text{ }^\circ\text{C}$ unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a RESET pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40\text{ }^\circ\text{C}$ to $105\text{ }^\circ\text{C}$.

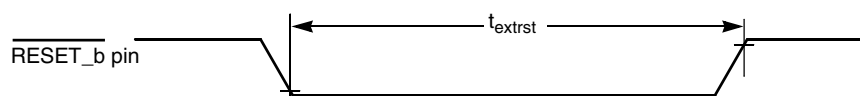


Figure 9. Reset timing

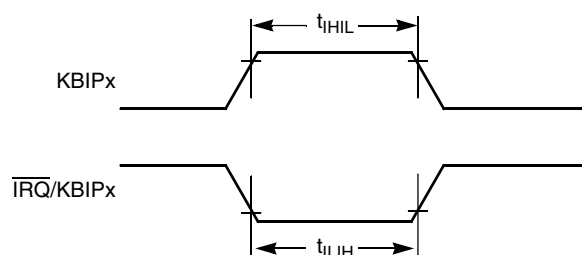


Figure 10. KBIPx timing

5.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

| C | Function | Symbol | Min | Max | Unit |
|---|--------------------------|------------|-----|-------------|-----------|
| D | External clock frequency | f_{TCLK} | 0 | $f_{Bus}/4$ | Hz |
| D | External clock period | t_{TCLK} | 4 | — | t_{cyc} |

Table continues on the next page...

Table 8. FTM input timing (continued)

| C | Function | Symbol | Min | Max | Unit |
|---|---------------------------|------------|-----|-----|-----------|
| D | External clock high time | t_{clkh} | 1.5 | — | t_{cyc} |
| D | External clock low time | t_{clkl} | 1.5 | — | t_{cyc} |
| D | Input capture pulse width | t_{ICPW} | 1.5 | — | t_{cyc} |

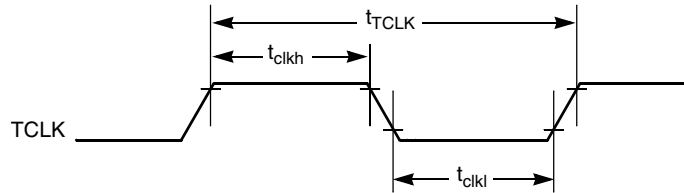


Figure 11. Timer external clock

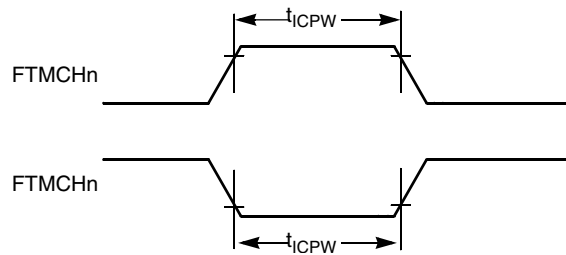


Figure 12. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal operating requirements

Table 9. Thermal operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|--------------------------|------|------|------|-------|
| T_J | Die junction temperature | -40 | 125 | °C | |
| T_A | Ambient temperature | -40 | 105 | °C | 1 |

- Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J . The simplest method to determine T_J is: $T_J = T_A + \theta_{JA} \times \text{chip power dissipation}$

5.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 10. Thermal attributes

| Board type | Symbo l | Description | 64 LQFP | 64 QFP | 44 LQFP | 32 LQFP | 32 QFN | Unit | Notes |
|-------------------|------------------|---|------------|--------|------------|------------|--------|------|-------|
| Single-layer (1S) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 71 | 61 | 75 | 86 | 97 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 53 | 47 | 53 | 57 | 33 | °C/W | 1, 3 |
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 59 | 50 | 62 | 72 | 81 | °C/W | 1, 3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 46 | 41 | 47 | 51 | 27 | °C/W | 1, 3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 35 | 32 | 34 | 33 | 12 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 20 | 23 | 20 | 24 | 1.3 | °C/W | 5 |
| — | Ψ_{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | 5 | 8 | 5 | 6 | 3 | °C/W | 6 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273 \text{ °C})$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273 \text{ °C}) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A .

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 SWD electricals

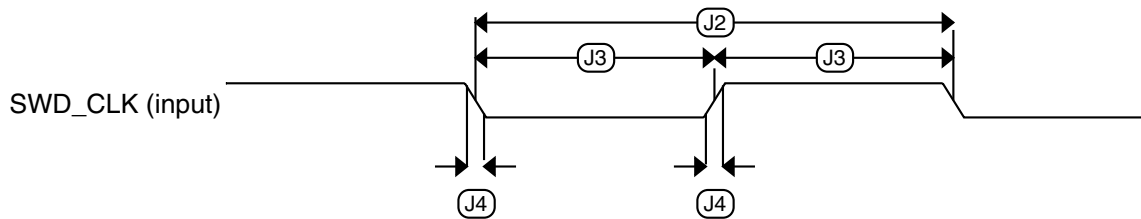
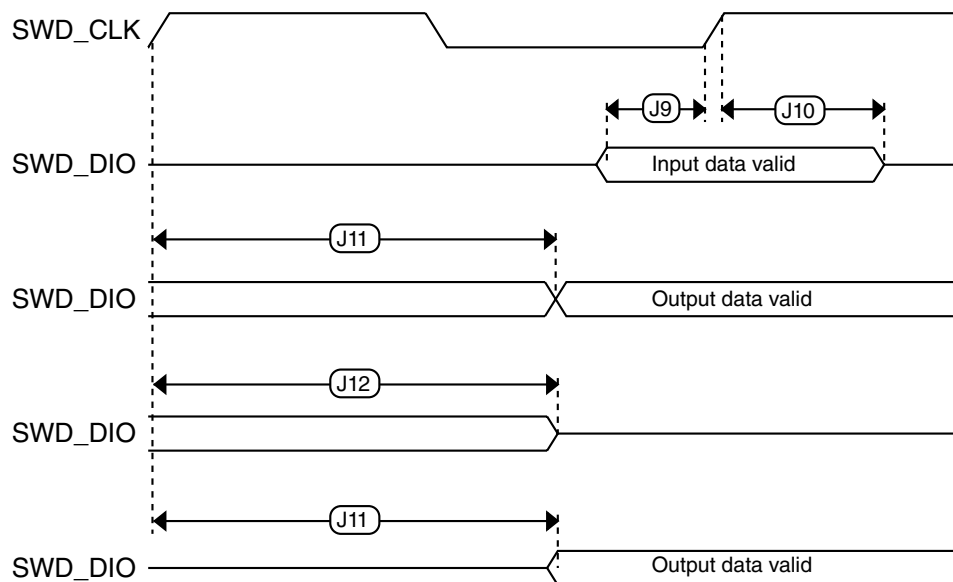
Table 11. SWD full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|--|------|------|------|
| | Operating voltage | 2.7 | 5.5 | V |
| J1 | SWD_CLK frequency of operation <ul style="list-style-type: none"> Serial wire debug | 0 | 20 | MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width <ul style="list-style-type: none"> Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 3 | — | ns |

Table continues on the next page...

Table 11. SWD full voltage range electricals (continued)

| Symbol | Description | Min. | Max. | Unit |
|--------|------------------------------------|------|------|------|
| J11 | SWD_CLK high to SWD_DIO data valid | — | 35 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

**Figure 13. Serial wire clock input timing****Figure 14. Serial wire data timing**

6.2 External oscillator (OSC) and ICS characteristics

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit | |
|-----|---|--------------------------------|------------------------|----------|----------------------|--------|---------|-----|
| 1 | C | Crystal or resonator frequency | Low range (RANGE = 0) | f_{lo} | 31.25 | 32.768 | 39.0625 | kHz |
| | C | | High range (RANGE = 1) | f_{hi} | 4 | — | 20 | MHz |

Table continues on the next page...

**Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)
(continued)**

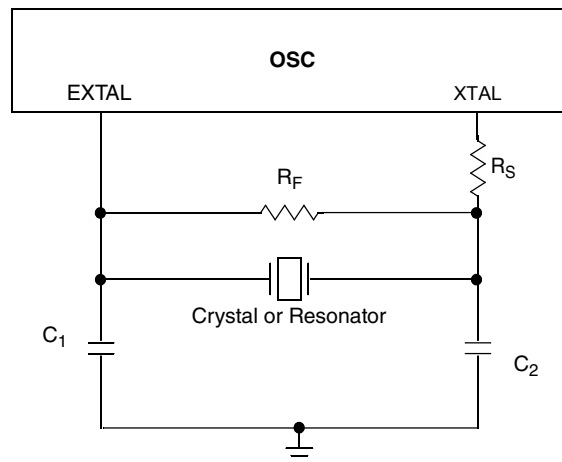
| Num | C | Characteristic | | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|--|---|-----------------------------|-----------------------|----------------------|---------|------|
| 2 | D | Load capacitors | | C1, C2 | See Note ² | | | |
| 3 | D | Feedback resistor | Low Frequency, Low-Power Mode ³ | R _F | — | — | — | MΩ |
| | | | Low Frequency, High-Gain Mode | | — | 10 | — | MΩ |
| | | | High Frequency, Low-Power Mode | | — | 1 | — | MΩ |
| | | | High Frequency, High-Gain Mode | | — | 1 | — | MΩ |
| 4 | D | Series resistor - Low Frequency | Low-Power Mode ³ | R _S ² | — | 0 | — | kΩ |
| | | | High-Gain Mode | | — | 200 | — | kΩ |
| 5 | D | Series resistor - High Frequency | Low-Power Mode ³ | R _S ² | — | 0 | — | kΩ |
| | D | Series resistor - High Frequency, High-Gain Mode | 4 MHz | | — | 0 | — | kΩ |
| | D | | 8 MHz | | — | 0 | — | kΩ |
| | D | | 16 MHz | | — | 0 | — | kΩ |
| 6 | C | Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal ^{4,5} | Low range, low power | t _{CSTL} | — | 1000 | — | ms |
| | C | | Low range, high gain | | — | 800 | — | ms |
| | C | | High range, low power | t _{CSTH} | — | 3 | — | ms |
| | C | | High range, high gain | — | 1.5 | — | ms | |
| 7 | T | Internal reference start-up time | | t _{IRST} | — | 20 | 50 | μs |
| 8 | P | Internal reference clock (IRC) frequency trim range | | f _{int_t} | 31.25 | — | 39.0625 | kHz |
| 9 | P | Internal reference clock frequency, factory trimmed | T = 25 °C, V _{DD} = 5 V | f _{int_ft} | — | 31.25 | — | kHz |
| 10 | P | DCO output frequency range | FLL reference = f _{int_t} , f _{lo} , or f _{hi} /RDIV | f _{dco} | 32 | — | 40 | MHz |
| 11 | P | Factory trimmed internal oscillator accuracy ⁶ | T = 25 °C, V _{DD} = 5 V | Δf _{int_ft} | -0.5 | — | 0.5 | % |
| 12 | C | Deviation of IRC over temperature when trimmed at T = 25 °C, V _{DD} = 5 V | Over temperature range from -40 °C to 105°C | Δf _{int_t} | -1 | — | 0.5 | % |
| | | | Over temperature range from 0 °C to 105°C | Δf _{int_t} | -0.5 | — | 0.5 | |
| 13 | C | Frequency accuracy of DCO output using factory trim value | Over temperature range from -40 °C to 105°C | Δf _{dco_ft} | -1.5 | — | 1 | % |
| | | | Over temperature range from 0 °C to 105°C | Δf _{dco_ft} | -1 | — | 1 | |

Table continues on the next page...

**Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)
(continued)**

| Num | C | Characteristic | Symbol | Min | Typical ¹ | Max | Unit |
|-----|---|---|----------------------|-----|----------------------|-----|--------------------|
| 14 | C | FLL acquisition time ^{4,7} | t_{Acquire} | — | — | 2 | ms |
| 15 | C | Long term jitter of DCO output clock (averaged over 2 ms interval) ⁸ | C_{Jitter} | — | 0.02 | 0.2 | % f_{dco} |

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. The accuracy is for factory trimmed deviation when performing trim process in NXP, however, the reflow process may cause an extra 0.5% drift at the room temperature.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

**Figure 15. Typical crystal or resonator circuit**

6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 13. Flash and EEPROM characteristics

| C | Characteristic | Symbol | Min ¹ | Typical ² | Max ³ | Unit ⁴ |
|---|---|-------------------------|------------------|----------------------|------------------|-------------------|
| D | Supply voltage for program/erase -40 °C to 105 °C | $V_{\text{prog/erase}}$ | 2.7 | — | 5.5 | V |

Table continues on the next page...

**Table 13. Flash and EEPROM characteristics
(continued)**

| C | Characteristic | Symbol | Min ¹ | Typical ² | Max ³ | Unit ⁴ |
|---|--|---------------|------------------|----------------------|------------------|-------------------|
| D | Supply voltage for read operation | V_{Read} | 2.7 | — | 5.5 | V |
| D | NVM Bus frequency | f_{NVMBUS} | 1 | — | 25 | MHz |
| D | NVM Operating frequency | f_{NVMOP} | 0.8 | 1 | 1.05 | MHz |
| D | Erase Verify All Blocks | t_{VFYALL} | — | — | 17338 | t_{cyc} |
| D | Erase Verify Flash Block | t_{RD1BLK} | — | — | 16913 | t_{cyc} |
| D | Erase Verify EEPROM Block | t_{RD1BLK} | — | — | 810 | t_{cyc} |
| D | Erase Verify Flash Section | t_{RD1SEC} | — | — | 484 | t_{cyc} |
| D | Erase Verify EEPROM Section | $t_{DRD1SEC}$ | — | — | 555 | t_{cyc} |
| D | Read Once | t_{RDONCE} | — | — | 450 | t_{cyc} |
| D | Program Flash (2 word) | t_{PGM2} | 0.12 | 0.12 | 0.29 | ms |
| D | Program Flash (4 word) | t_{PGM4} | 0.20 | 0.21 | 0.46 | ms |
| D | Program Once | $t_{PGMONCE}$ | 0.20 | 0.21 | 0.21 | ms |
| D | Program EEPROM (1 Byte) | t_{DPGM1} | 0.10 | 0.10 | 0.27 | ms |
| D | Program EEPROM (2 Byte) | t_{DPGM2} | 0.17 | 0.18 | 0.43 | ms |
| D | Program EEPROM (3 Byte) | t_{DPGM3} | 0.25 | 0.26 | 0.60 | ms |
| D | Program EEPROM (4 Byte) | t_{DPGM4} | 0.32 | 0.33 | 0.77 | ms |
| D | Erase All Blocks | t_{ERSALL} | 96.01 | 100.78 | 101.49 | ms |
| D | Erase Flash Block | t_{ERSBLK} | 95.98 | 100.75 | 101.44 | ms |
| D | Erase Flash Sector | t_{ERSPG} | 19.10 | 20.05 | 20.08 | ms |
| D | Erase EEPROM Sector | t_{DERSPG} | 4.81 | 5.05 | 20.57 | ms |
| D | Unsecure Flash | t_{UNSECU} | 96.01 | 100.78 | 101.48 | ms |
| D | Verify Backdoor Access Key | t_{VFYKEY} | — | — | 464 | t_{cyc} |
| D | Set User Margin Level | t_{MLOADU} | — | — | 407 | t_{cyc} |
| C | FLASH Program/erase endurance T_L to $T_H = -40\text{ }^\circ\text{C}$ to $105\text{ }^\circ\text{C}$ | n_{FLPE} | 10 k | 100 k | — | Cycles |
| C | EEPROM Program/erase endurance T_L to $T_H = -40\text{ }^\circ\text{C}$ to $105\text{ }^\circ\text{C}$ | n_{FLPE} | 50 k | 500 k | — | Cycles |
| C | Data retention at an average junction temperature of $T_{Javg} = 85\text{ }^\circ\text{C}$ after up to 10,000 program/erase cycles | t_{D_ret} | 15 | 100 | — | years |

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

6.4 Analog

6.4.1 ADC characteristics

Table 14. 5 V 12-bit ADC operating conditions

| Characteristic | Conditions | Symbol | Min | Typ ¹ | Max | Unit | Comment |
|--------------------------------|--|------------------|------------|------------------|------------|------------|-----------------|
| Reference potential | <ul style="list-style-type: none"> Low High | V_{REFL} | V_{SSA} | — | V_{SSA} | V | — |
| | | V_{REFH} | V_{DDA} | — | V_{DDA} | | |
| Supply voltage | Absolute | V_{DDA} | 2.7 | — | 5.5 | V | — |
| | Delta to V_{DD} ($V_{DD}-V_{DDA}$) | ΔV_{DDA} | -100 | 0 | +100 | mV | — |
| Ground voltage | Delta to V_{SS} ($V_{SS}-V_{SSA}$) | ΔV_{SSA} | -100 | 0 | +100 | mV | — |
| Input voltage | | V_{ADIN} | V_{REFL} | — | V_{REFH} | V | — |
| Input capacitance | | C_{ADIN} | — | 4.5 | 5.5 | pF | — |
| Input resistance | | R_{ADIN} | — | 3 | 5 | k Ω | — |
| Analog source resistance | 12-bit mode <ul style="list-style-type: none"> $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz | R_{AS} | — | — | 2 | k Ω | External to MCU |
| | 10-bit mode <ul style="list-style-type: none"> $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz | | — | — | 5 | | |
| | 8-bit mode (all valid f_{ADCK}) | | — | — | 10 | | |
| ADC conversion clock frequency | High speed (ADLPC=0) | f_{ADCK} | 0.4 | — | 8.0 | MHz | — |
| | Low power (ADLPC=1) | | 0.4 | — | 4.0 | | |

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

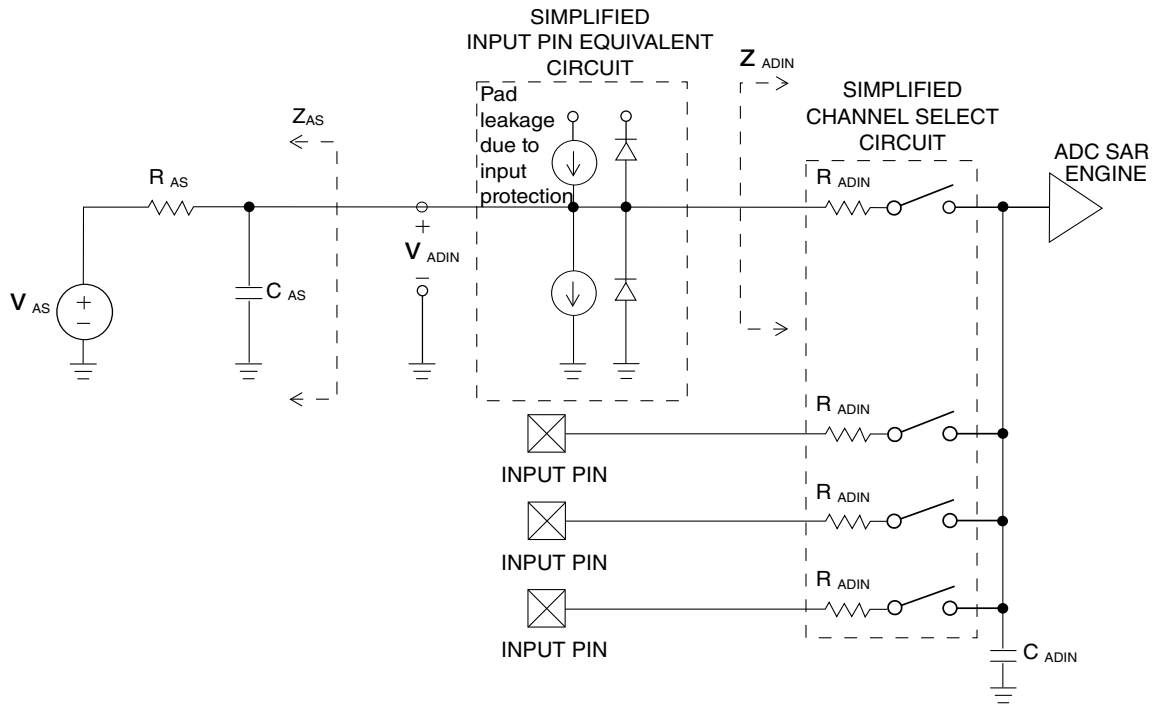


Figure 16. ADC input impedance equivalency diagram

Table 15. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Characteristic | Conditions | C | Symbol | Min | Typ ¹ | Max | Unit |
|---|-------------------------|---|-------------|-----|------------------|-----|---------------|
| Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1 | | T | I_{DDA} | — | 133 | — | μA |
| Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1 | | T | I_{DDA} | — | 218 | — | μA |
| Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1 | | T | I_{DDA} | — | 327 | — | μA |
| Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1 | | T | I_{DDA} | — | 582 | 990 | μA |
| Supply current | Stop, reset, module off | T | I_{DDA} | — | 0.011 | 1 | μA |
| ADC asynchronous clock source | High speed (ADLPC = 0) | P | f_{ADACK} | 2 | 3.3 | 5 | MHz |

Table continues on the next page...

Table 15. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Characteristic | Conditions | C | Symbol | Min | Typ ¹ | Max | Unit |
|---|---------------------------|---|--------------|-------------------|------------------|------------|------------------|
| | Low power (ADLPC = 1) | | | 1.25 | 2 | 3.3 | |
| Conversion time (including sample time) | Short sample (ADLSMP = 0) | T | t_{ADC} | — | 20 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 40 | — | |
| Sample time | Short sample (ADLSMP = 0) | T | t_{ADS} | — | 3.5 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 23.5 | — | |
| Total unadjusted Error ² | 12-bit mode ³ | T | E_{TUE} | — | ± 3.6 | — | LSB ⁴ |
| | 10-bit mode | P | | — | ± 1.5 | ± 2.0 | |
| | 8-bit mode | T | | — | ± 0.7 | ± 1.0 | |
| Differential Non-Linearity | 12-bit mode | T | DNL | — | ± 1.0 | — | LSB ⁴ |
| | 10-bit mode ⁵ | P | | — | ± 0.25 | ± 0.5 | |
| | 8-bit mode ⁵ | T | | — | ± 0.15 | ± 0.25 | |
| Integral Non-Linearity | 12-bit mode ³ | T | INL | — | ± 1.0 | — | LSB ⁴ |
| | 10-bit mode | T | | — | ± 0.3 | ± 0.5 | |
| | 8-bit mode | T | | — | ± 0.15 | ± 0.25 | |
| Zero-scale error ⁶ | 12-bit mode | C | E_{ZS} | — | ± 2.0 | — | LSB ⁴ |
| | 10-bit mode | P | | — | ± 0.25 | ± 1.0 | |
| | 8-bit mode | T | | — | ± 0.65 | ± 1.0 | |
| Full-scale error ⁷ | 12-bit mode | T | E_{FS} | — | ± 2.5 | — | LSB ⁴ |
| | 10-bit mode | T | | — | ± 0.5 | ± 1.0 | |
| | 8-bit mode | T | | — | ± 0.5 | ± 1.0 | |
| Quantization error | ≤ 12 bit modes | D | E_Q | — | — | ± 0.5 | LSB ⁴ |
| Input leakage error ⁸ | all modes | D | E_{IL} | $I_{in} * R_{AS}$ | | | mV |
| Temp sensor slope | -40 °C–25 °C | D | m | — | 3.266 | — | mV/°C |
| | 25 °C–125 °C | | | — | 3.638 | — | |
| Temp sensor voltage | 25 °C | D | V_{TEMP25} | — | 1.396 | — | V |

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3. This parameter is valid for the temperature range of 25 °C to 50 °C.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
6. $V_{ADIN} = V_{SSA}$
7. $V_{ADIN} = V_{DDA}$
8. I_{in} = leakage current (refer to DC characteristics)

6.4.2 Analog comparator (ACMP) electricals

Table 16. Comparator electrical specifications

| C | Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---------------------------------------|---------------------|----------------|---------|-----------|---------------|
| D | Supply voltage | V_{DDA} | 2.7 | — | 5.5 | V |
| T | Supply current (Operation mode) | I_{DDA} | — | 10 | 20 | μA |
| D | Analog input voltage | V_{AIN} | $V_{SS} - 0.3$ | — | V_{DDA} | V |
| P | Analog input offset voltage | V_{AIO} | — | — | 40 | mV |
| C | Analog comparator hysteresis (HYST=0) | V_H | — | 15 | 20 | mV |
| C | Analog comparator hysteresis (HYST=1) | V_H | — | 20 | 30 | mV |
| T | Supply current (Off mode) | $I_{DDA\text{OFF}}$ | — | 60 | — | nA |
| C | Propagation Delay | t_D | — | 0.4 | 1 | μs |

6.5 Communication interfaces

6.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 80% V_{DD} , unless noted, and 25 pF load on all SPI pins. All timing assumes high-drive strength is enabled for SPI output pins.

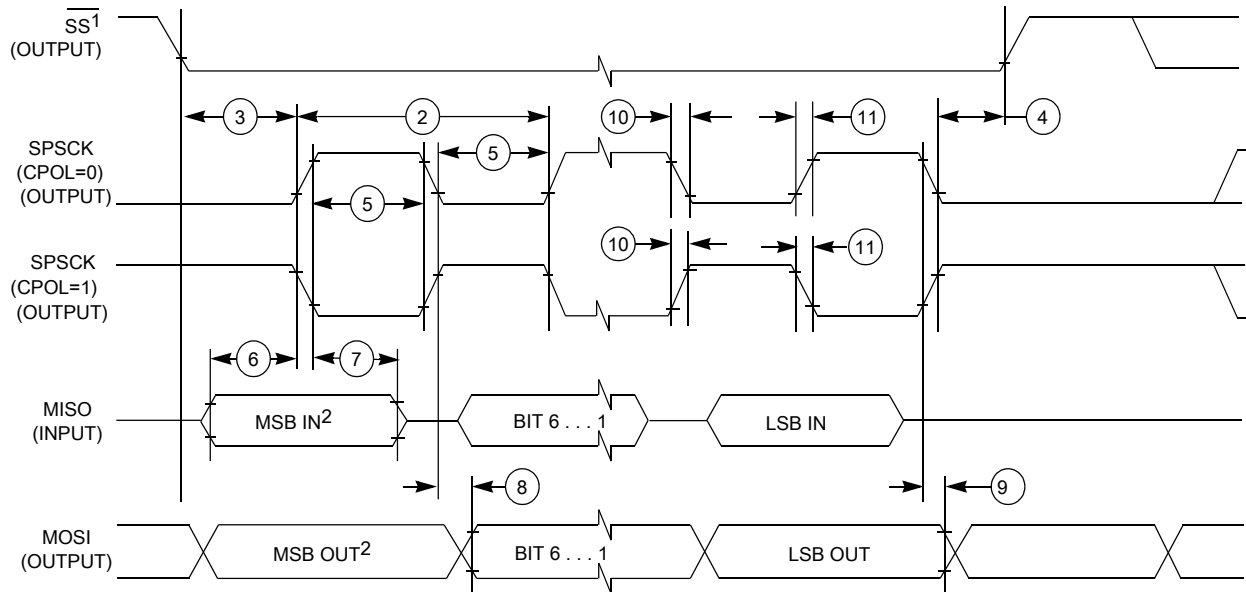
Table 17. SPI master mode timing

| Nu m. | Symbol | Description | Min. | Max. | Unit | Comment |
|-------|--------------|--------------------------------|--------------------|-----------------------|-------------|----------------------------|
| 1 | f_{op} | Frequency of operation | $f_{Bus}/2048$ | $f_{Bus}/2$ | Hz | f_{Bus} is the bus clock |
| 2 | t_{SPSCK} | SPSCK period | $2 \times t_{Bus}$ | $2048 \times t_{Bus}$ | ns | $t_{Bus} = 1/f_{Bus}$ |
| 3 | t_{Lead} | Enable lead time | 1/2 | — | t_{SPSCK} | — |
| 4 | t_{Lag} | Enable lag time | 1/2 | — | t_{SPSCK} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{Bus} - 30$ | $1024 \times t_{Bus}$ | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 8 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 8 | — | ns | — |
| 8 | t_v | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 9 | t_{HO} | Data hold time (outputs) | 20 | — | ns | — |
| 10 | t_{RI} | Rise time input | — | $t_{Bus} - 25$ | ns | — |

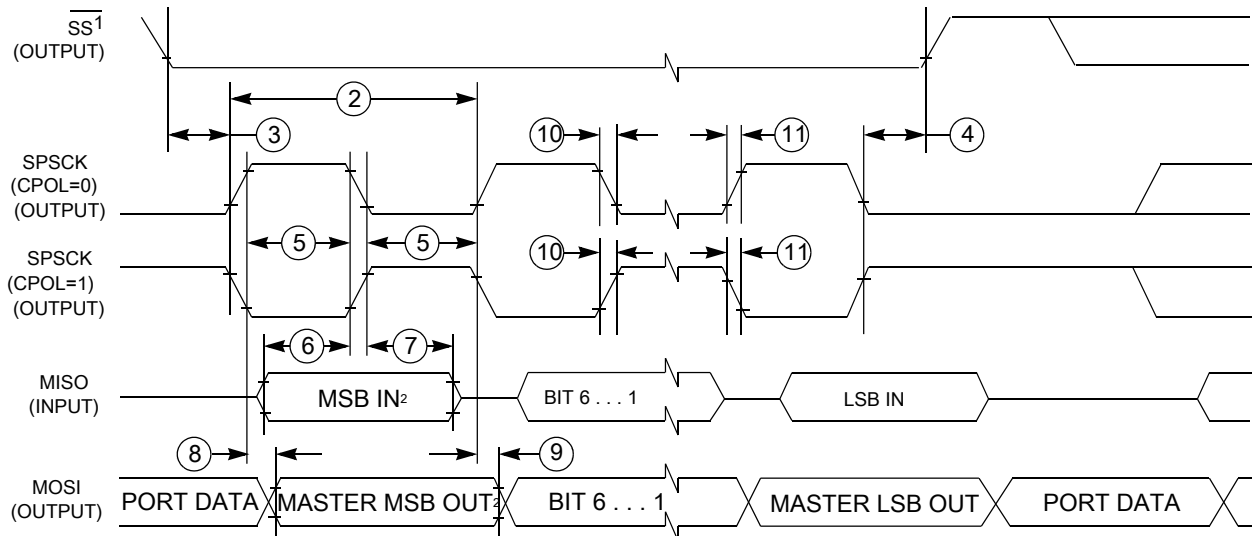
Table continues on the next page...

Table 17. SPI master mode timing (continued)

| Nu m. | Symbol | Description | Min. | Max. | Unit | Comment |
|-------|----------|------------------|------|------|------|---------|
| | t_{FI} | Fall time input | | | | |
| 11 | t_{RO} | Rise time output | — | 25 | ns | — |
| | t_{FO} | Fall time output | | | | |



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

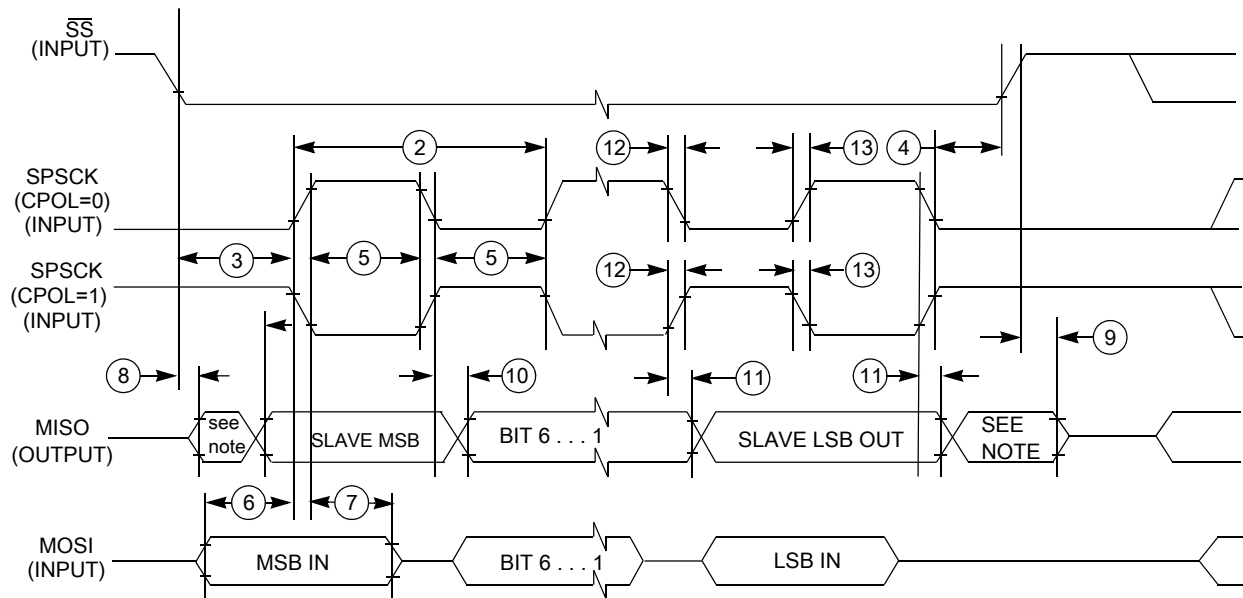
Figure 17. SPI master mode timing (CPHA=0)

1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 18. SPI slave mode timing

| Nu m. | Symbol | Description | Min. | Max. | Unit | Comment |
|-------|--------------|--------------------------------|--------------------|----------------|-----------|---|
| 1 | f_{op} | Frequency of operation | 0 | $f_{BUS}/4$ | Hz | f_{BUS} is the bus clock as defined in Control timing . |
| 2 | t_{SPSCK} | SPSCK period | $4 \times t_{BUS}$ | — | ns | $t_{BUS} = 1/f_{BUS}$ |
| 3 | t_{Lead} | Enable lead time | 1 | — | t_{BUS} | — |
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{BUS} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{BUS} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 15 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 25 | — | ns | — |
| 8 | t_a | Slave access time | — | t_{BUS} | ns | Time to data active from high-impedance state |
| 9 | t_{dis} | Slave MISO disable time | — | t_{BUS} | ns | Hold time to high-impedance state |
| 10 | t_v | Data valid (after SPSCK edge) | — | 25 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} | Rise time input | — | $t_{BUS} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 13 | t_{RO} | Rise time output | — | 25 | ns | — |
| | t_{FO} | Fall time output | | | | |



NOTE: Not defined

Figure 19. SPI slave mode timing (CPHA = 0)

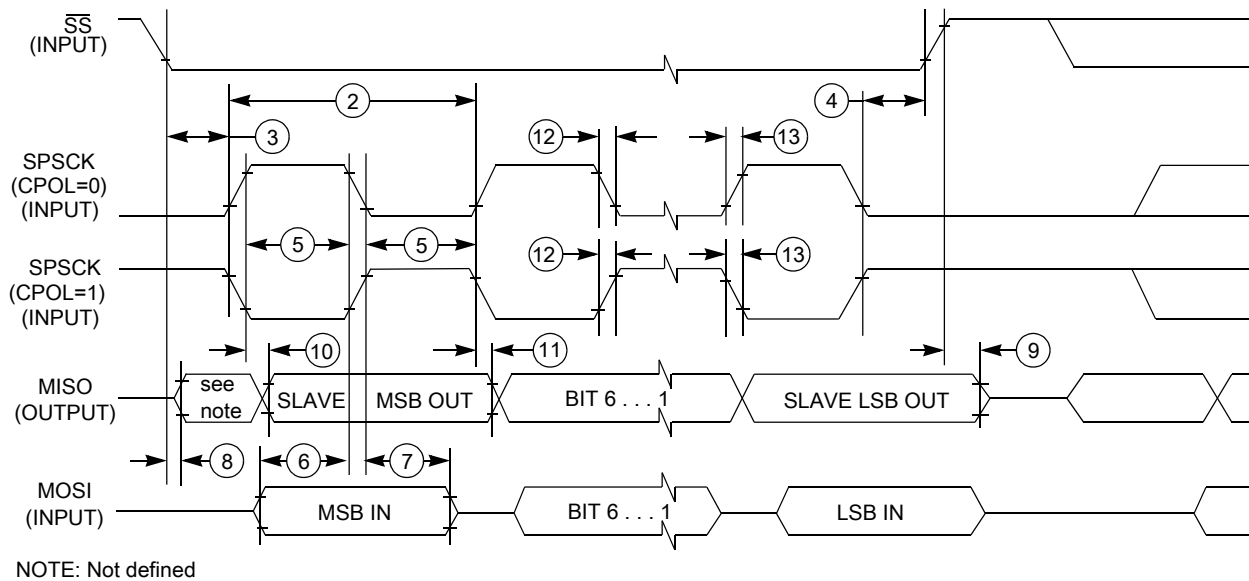


Figure 20. SPI slave mode timing (CPHA=1)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 32-pin LQFP | 98ASH70029A |
| 32-pin QFN | 98ASA00473D |
| 44-pin LQFP | 98ASS23225W |
| 64-pin QFP | 98ASB42844B |
| 64-pin LQFP | 98ASS23234W |

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 19. Pin availability by package pin-count

| Pin Number | | | Lowest Priority <-- --> Highest | | | | |
|-----------------|---------|-----------------|---------------------------------|----------|-----------|-----------|--------------------|
| 64-QFP/ LQFP | 44-LQFP | 32- LQFP/QFN | Port Pin | Alt 1 | Alt 2 | Alt 3 | Alt 4 |
| 1 | 1 | 1 | PTD1 ¹ | KBI1_P1 | FTM2_CH3 | SPI1_MOSI | — |
| 2 | 2 | 2 | PTD0 ¹ | KBI1_P0 | FTM2_CH2 | SPI1_SCK | — |
| 3 | — | — | PTH7 | — | — | — | — |
| 4 | — | — | PTH6 | — | — | — | — |
| 5 | 3 | — | PTE7 | — | FTM2_CLK | — | FTM1_CH1 |
| 6 | 4 | — | PTH2 | — | BUSOUT | — | FTM1_CH0 |
| 7 | 5 | 3 | — | — | — | — | VDD |
| 8 | 6 | 4 | — | — | — | VDDA | VREFH ² |
| 9 | 7 | 5 | — | — | — | — | VREFL |
| 10 | 8 | 6 | — | — | — | VSSA | VSS ³ |
| 11 | 9 | 7 | PTB7 | — | I2C0_SCL | — | EXTAL |
| 12 | 10 | 8 | PTB6 | — | I2C0_SDA | — | XTAL |
| 13 | 11 | — | — | — | — | — | VSS |
| 14 | — | — | PTH1 ¹ | — | FTM2_CH1 | — | — |
| 15 | — | — | PTH0 ¹ | — | FTM2_CH0 | — | — |
| 16 | — | — | PTE6 | — | — | — | — |
| 17 | — | — | PTE5 | — | — | — | — |
| 18 | 12 | 9 | PTB5 ¹ | FTM2_CH5 | SPI0_PCS0 | ACMP1_OUT | — |
| 19 | 13 | 10 | PTB4 ¹ | FTM2_CH4 | SPI0_MISO | NMI | ACMP1_IN2 |
| 20 | 14 | 11 | PTC3 | FTM2_CH3 | — | — | ADC0_SE11 |
| 21 | 15 | 12 | PTC2 | FTM2_CH2 | — | — | ADC0_SE10 |
| 22 | 16 | — | PTD7 | KBI1_P7 | UART2_TX | — | — |
| 23 | 17 | — | PTD6 | KBI1_P6 | UART2_RX | — | — |
| 24 | 18 | — | PTD5 | KBI1_P5 | — | — | — |
| 25 | 19 | 13 | PTC1 | — | FTM2_CH1 | — | ADC0_SE9 |
| 26 | 20 | 14 | PTC0 | — | FTM2_CH0 | — | ADC0_SE8 |
| 27 | — | — | PTF7 | — | — | — | ADC0_SE15 |

Table continues on the next page...

Table 19. Pin availability by package pin-count (continued)

| Pin Number | | | Lowest Priority <-- --> Highest | | | | |
|-----------------|---------|-----------------|---------------------------------|---------|-----------|-----------|-----------|
| 64-QFP/ LQFP | 44-LQFP | 32- LQFP/QFN | Port Pin | Alt 1 | Alt 2 | Alt 3 | Alt 4 |
| 28 | — | — | PTF6 | — | — | — | ADC0_SE14 |
| 29 | — | — | PTF5 | — | — | — | ADC0_SE13 |
| 30 | — | — | PTF4 | — | — | — | ADC0_SE12 |
| 31 | 21 | 15 | PTB3 | KBI0_P7 | SPI0_MOSI | FTM0_CH1 | ADC0_SE7 |
| 32 | 22 | 16 | PTB2 | KBI0_P6 | SPI0_SCK | FTM0_CH0 | ADC0_SE6 |
| 33 | 23 | 17 | PTB1 | KBI0_P5 | UART0_TX | — | ADC0_SE5 |
| 34 | 24 | 18 | PTB0 | KBI0_P4 | UART0_RX | — | ADC0_SE4 |
| 35 | — | — | PTF3 | — | — | — | — |
| 36 | — | — | PTF2 | — | — | — | — |
| 37 | 25 | 19 | PTA7 | — | FTM2_FLT2 | ACMP1_IN1 | ADC0_SE3 |
| 38 | 26 | 20 | PTA6 | — | FTM2_FLT1 | ACMP1_IN0 | ADC0_SE2 |
| 39 | — | — | PTE4 | — | — | — | — |
| 40 | 27 | — | — | — | — | — | VSS |
| 41 | 28 | — | — | — | — | — | VDD |
| 42 | — | — | PTF1 | — | — | — | — |
| 43 | — | — | PTF0 | — | — | — | — |
| 44 | 29 | — | PTD4 | KBI1_P4 | — | — | — |
| 45 | 30 | 21 | PTD3 | KBI1_P3 | SPI1_PCS0 | — | — |
| 46 | 31 | 22 | PTD2 | KBI1_P2 | SPI1_MISO | — | — |
| 47 | 32 | 23 | PTA3 ⁴ | KBI0_P3 | UART0_TX | I2C0_SCL | — |
| 48 | 33 | 24 | PTA2 ⁴ | KBI0_P2 | UART0_RX | I2C0_SDA | — |
| 49 | 34 | 25 | PTA1 | KBI0_P1 | FTM0_CH1 | ACMP0_IN1 | ADC0_SE1 |
| 50 | 35 | 26 | PTA0 | KBI0_P0 | FTM0_CH0 | ACMP0_IN0 | ADC0_SE0 |
| 51 | 36 | 27 | PTC7 | — | UART1_TX | — | — |
| 52 | 37 | 28 | PTC6 | — | UART1_RX | — | — |
| 53 | — | — | PTE3 | — | SPI0_PCS0 | — | — |
| 54 | 38 | — | PTE2 | — | SPI0_MISO | — | — |
| 55 | — | — | PTG3 | — | — | — | — |
| 56 | — | — | PTG2 | — | — | — | — |
| 57 | — | — | PTG1 | — | — | — | — |
| 58 | — | — | PTG0 | — | — | — | — |
| 59 | 39 | — | PTE1 ¹ | — | SPI0_MOSI | — | — |
| 60 | 40 | — | PTE0 ¹ | — | SPI0_SCK | FTM1_CLK | — |
| 61 | 41 | 29 | PTC5 | — | FTM1_CH1 | — | RTCO |
| 62 | 42 | 30 | PTC4 | RTCO | FTM1_CH0 | ACMP0_IN2 | SWD_CLK |
| 63 | 43 | 31 | PTA5 | IRQ | FTM0_CLK | — | RESET |
| 64 | 44 | 32 | PTA4 | — | ACMP0_OUT | — | SWD_DIO |

1. This is a high-current drive pin when operated as output.

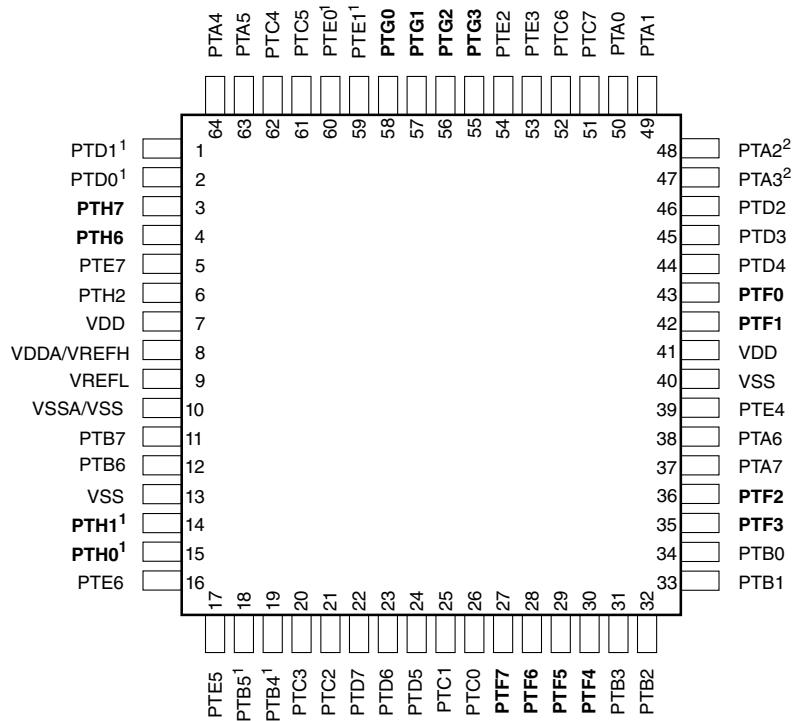
Pinout

2. VREFH and VDDA are internally connected.
3. VSSA and VSS are internally connected.
4. This is a true open-drain pin when operated as output.

Note

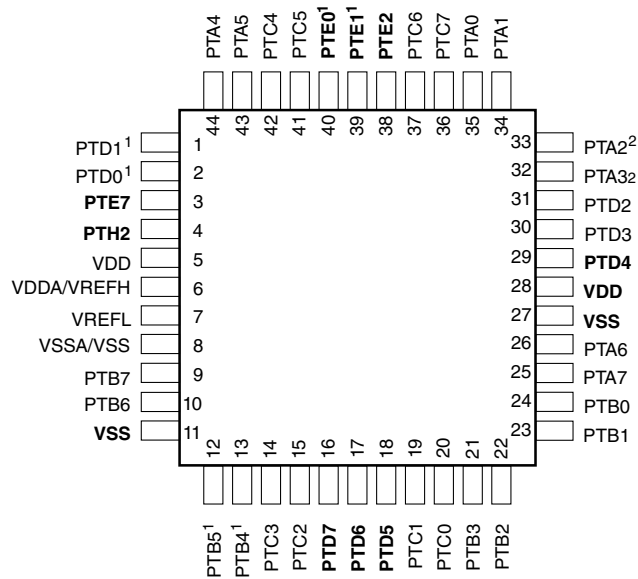
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. [Table 19](#) illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment



Pins in **bold** are not available on less pin-count packages.
 1. High source/sink current pins
 2. True open drain pins

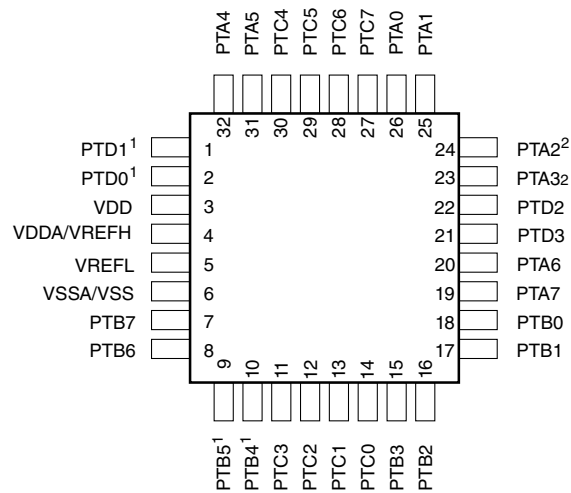
Figure 21. 64-pin QFP/LQFP packages



Pins in **bold** are not available on less pin-count packages.

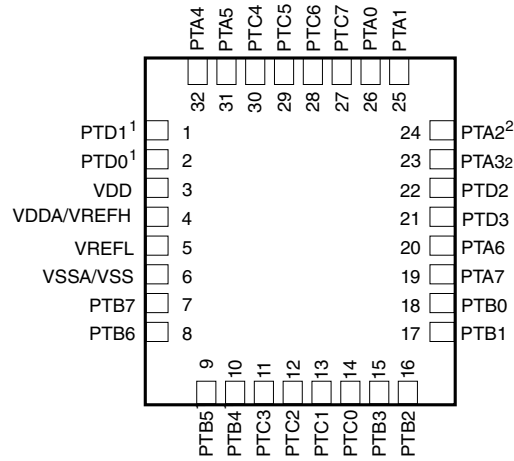
1. High source/sink current pins
2. True open drain pins

Figure 22. 44-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 23. 32-pin LQFP package



- 1. High source/sink current pins
- 2. True open drain pins

Figure 24. 32-pin QFN package

9 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

| Rev. No. | Date | Substantial Changes |
|----------|---------|---|
| 2 | 3/2014 | Initial public release. |
| 3 | 10/2014 | <ul style="list-style-type: none"> • Added new package of 32-pin QFN information • Updated pin-out • Updated key features of UART, KBI and ADC in the front page • Added a note to the Max. in Supply current characteristics • Updated footnote $f_{OSC} = 10$ MHz (crystal) in EMC radiated emissions operating behaviors • Added a new section of Thermal operating requirements • Updated NVM specifications • Added reference potential in ADC characteristics • Updated to "All timing assumes high-drive strength is enabled for SPI output pins." in SPI switching specifications |
| 4 | 07/2016 | <ul style="list-style-type: none"> • Updated the Typical value of E_{TUE} in 12-bit mode and added a note to the 12-bit mode of E_{TUE} and INL in the ADC characteristics. |
| 5 | 01/2019 | <ul style="list-style-type: none"> • Added a footnote of "Max power supply ramp rate is 500 V/ms." to Operating voltage in the DC characteristics. • Added a footnote to the Δf_{int_ft} in the External oscillator (OSC) and ICS characteristics |
| 6 | 12/2019 | <ul style="list-style-type: none"> • Updated the footnote to the Operating voltage in the DC characteristics. |

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