NCP1216, NCP1216A

PWM Current-Mode Controller for High-Power Universal Off-Line Supplies

Housed in a SOIC−8 or PDIP−7 package, the NCP1216 represents an enhanced version of NCP1200 based controllers. Due to its high drive capability, NCP1216 drives large gate−charge MOSFETs, which together with internal ramp compensation and built−in frequency jittering, ease the design of modern AC−DC adapters.

With an internal structure operating at different fixed frequencies, the controller supplies itself from the high−voltage rail, avoiding the need of an auxiliary winding. This feature naturally eases the designer task in some particular applications, e.g. battery chargers or TV sets. Current−mode control also provides an excellent input audio susceptibility and inherent pulse−by−pulse control. Internal ramp compensation easily prevents sub−harmonic oscillations from taking place in continuous conduction mode designs.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so−called skip cycle mode and provides excellent efficiency at light loads. Because this occurs at a user adjustable low peak current, no acoustic noise takes place.

The NCP1216 features an efficient protective circuitry, which in presence of an over current condition disables the output pulses while the device enters a safe burst mode, trying to restart. Once the default has gone, the device auto−recovers.

Features

- No Auxiliary Winding Operation
- Current−Mode Control with Adjustable Skip−Cycle Capability
- Internal Ramp Compensation
- Limited Duty Cycle to 50% (NCP1216A Only)
- Internal 1.0 ms Soft−Start (NCP1216A Only)
- Built−In Frequency Jittering for Better EMI Signature
- Auto−Recovery Internal Output Short−Circuit Protection
- Extremely Low No−Load Standby Power
- 500 mA Peak Current Capability
- Fixed Frequency Versions at 65 kHz, 100 kHz, 133 kHz
- Internal Temperature Shutdown
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient and AC Analysis
- Pin−to−Pin Compatible with NCP1200 Series
- These are Pb−Free and Halide−Free Devices

Typical Applications

- High Power AC−DC Converters for TVs, Set−Top Boxes, etc.
- Offline Adapters for Notebooks
- Telecom DC−DC Converters
- All Power Supplies

ON Semiconductor®

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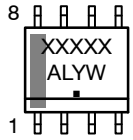
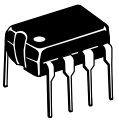
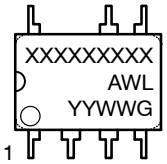
MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751



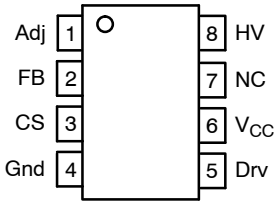


PDIP−7
P SUFFIX
CASE 626B



XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

PIN CONNECTIONS



DEVICE MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 16 of this data sheet.

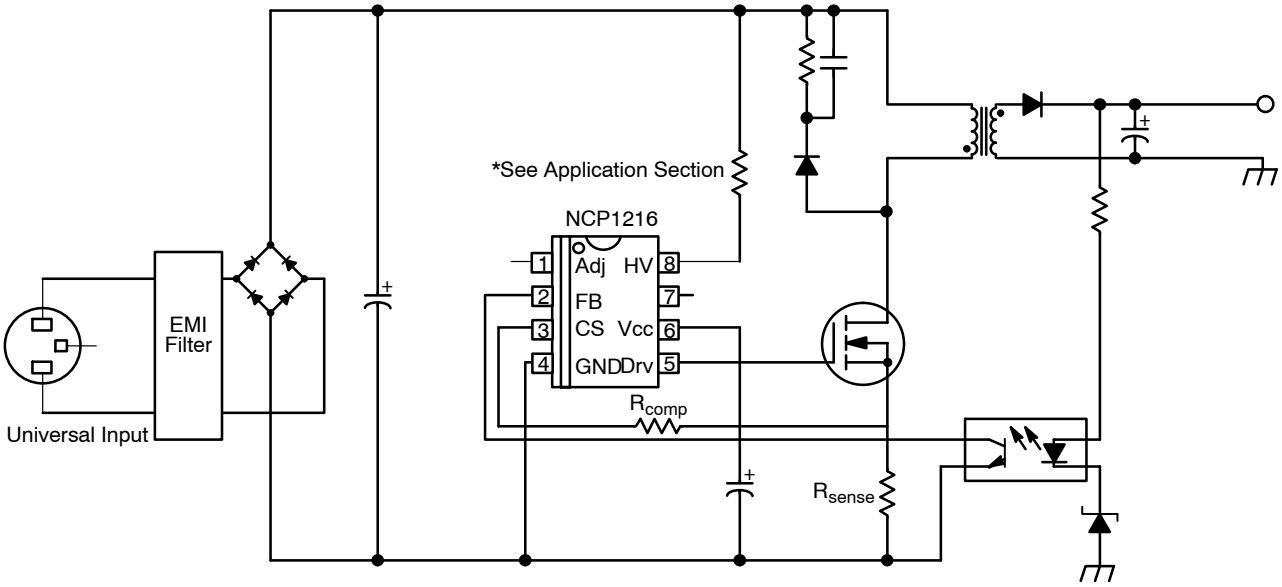
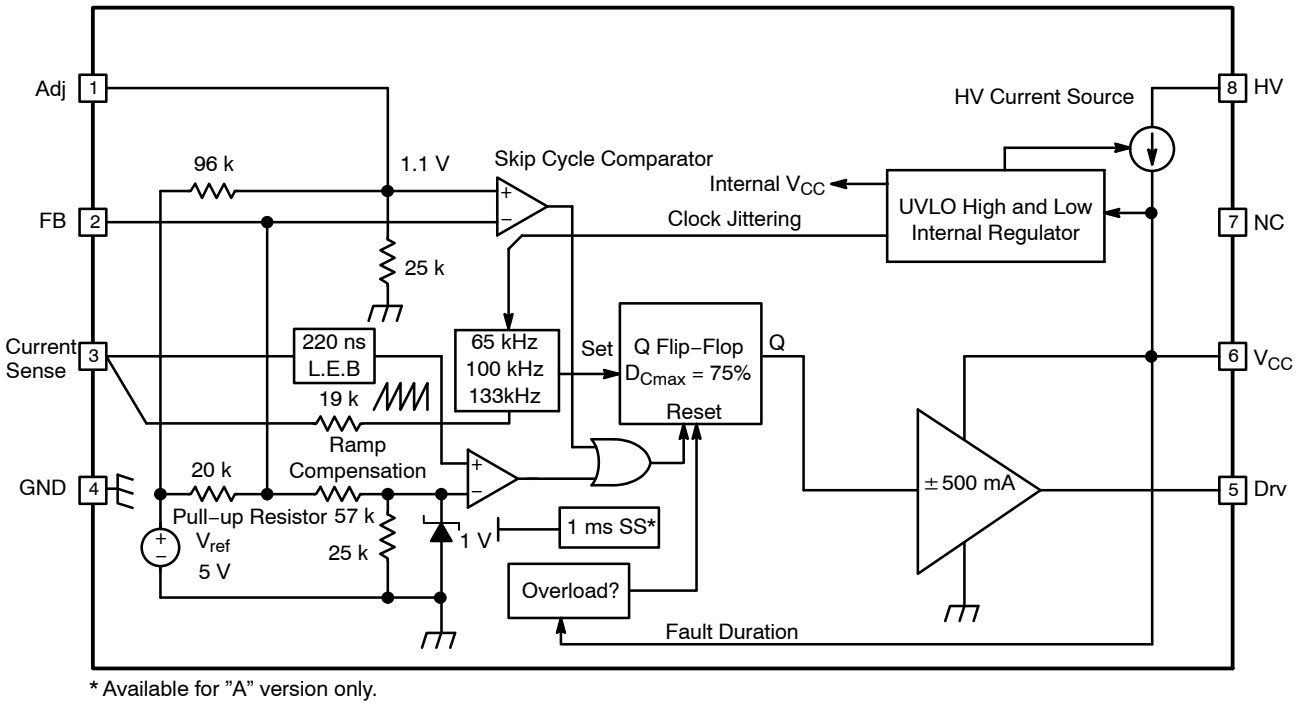


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	Adj	Adjust the Skipping Peak Current	This pin lets you adjust the level at which the cycle skipping process takes place. Shorting this pin to ground, permanently disables the skip cycle feature.
2	FB	Sets the Peak Current Setpoint	By connecting an Optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand.
3	CS	Current Sense Input	This pin senses the primary current and routes it to the internal comparator via an L.E.B. By inserting a resistor in series with the pin, you control the amount of ramp compensation you need.
4	GND	IC Ground	–
5	Drv	Driving Pulses	The driver's output to an external MOSFET.
6	V_{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 22 μF.
7	NC	–	This un−connected pin ensures adequate creepage distance.
8	HV	Generates the V_{CC} from the Line	Connected to the high−voltage rail, this pin injects a constant current into the V_{CC} bulk capacitor.



* Available for "A" version only.

Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage, V_{CC} Pin	V_{CC}	16	V
Maximum Voltage on Low Power Pins (except Pin 8 and Pin 6)		−0.3 to 10	V
Maximum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) Decoupled to Ground with 10 μF		500	V
Maximum Voltage on Pin 8 (HV), Pin 6 (V_{CC}) Grounded		450	V
Minimum Operating Voltage on Pin 8 (HV)		28	V
Maximum Current into all Pins except V_{CC} (Pin 6) and HV (Pin 8) when 10 V ESD Diodes are Activated		5.0	mA
Thermal Resistance Junction−to−Air, PDIP−7 Version Thermal Resistance Junction−to−Air, SOIC−8 Version	$R_{\theta J-A}$ $R_{\theta J-A}$	100 178	°C/W
Maximum Junction Temperature	T_{JMAX}	150	°C
Temperature Shutdown	TSD	155	°C
Hysteresis in Shutdown		30	°C
Storage Temperature Range		−60 to +150	°C
ESD Capability, HBM Model (All Pins except V_{CC} and HV)		2.0	kV
ESD Capability, Machine Model		200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection rated using the following tests:
   Human Body Model (HBM) 2000 V per JEDEC Standard JESD22, Method A114E.
   Machine Model (MM) 200 V per JEDEC Standard JESD22, Method A115A.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Maximum T_J = 150°C, V_{CC} = 11 V unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
DYNAMIC SELF−SUPPLY						
V_{CC} Increasing Level at which the Current Source Turns Off	6	VCC_{OFF}	11.2	12.2	13.4 (Note 1)	V
V_{CC} Decreasing Level at which the Current Source Turns On	6	VCC_{ON}	9.2	10.0	11.0 (Note 1)	V
V_{CC} Decreasing Level at which the Latchoff Phase Ends	6	VCC_{latch}		5.6		V
Internal IC Consumption, Latchoff Phase, V_{CC} = 6.0 V NCP1216 NCP1216A	6	I_{CC3}		250 320		μA
Internal IC Consumption, No Output Load on Pin 5, F_{SW} = 65 kHz 0°C ≤ T_J ≤ +125°C −40°C ≤ T_J ≤ +125°C	6	I_{CC1}		990	 1110 1245	μA
Internal IC Consumption, No Output Load on Pin 5, F_{SW} = 100 kHz 0°C ≤ T_J ≤ +125°C −40°C ≤ T_J ≤ +125°C	6	I_{CC1}		1025	 1180 1285	μA
Internal IC Consumption, No Output Load on Pin 5, F_{SW} = 133 kHz 0°C ≤ T_J ≤ +125°C −40°C ≤ T_J ≤ +125°C	6	I_{CC1}		1060	 1200 1290	μA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 65 kHz 0°C ≤ T_J ≤ +125°C −40°C ≤ T_J ≤ +125°C	6	I_{CC2}		1.7	 2.0 2.0	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 100 kHz 0°C ≤ T_J ≤ +125°C −40°C ≤ T_J ≤ +125°C	6	I_{CC2}		2.1	 2.4 2.55	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, F_{SW} = 133 kHz 0°C ≤ T_J ≤ +125°C −40°C ≤ T_J ≤ +125°C	6	I_{CC2}		2.4	 2.9 3.0	mA
INTERNAL STARTUP CURRENT SOURCE (T_J > 0°C)						
High−voltage Current Source, V_{CC} = 10 V	8	IC1	4.9 (Note 2)	8.0	11	mA
High−voltage Current Source, V_{CC} = 0 V	8	IC2		9.0		mA
DRIVE OUTPUT						
Output Voltage Rise−time @ C_L = 1.0 nF, 10−90% of a 12 V Output Signal	5	T_r		60		ns
Output Voltage Fall−time @ C_L = 1.0 nF, 10−90% of a 12 V Output Signal	5	T_f		20		ns
Source Resistance	5	R_{OH}	15	20	35	Ω
Sink Resistance	5	R_{OL}	5.0	10	18	Ω
CURRENT COMPARATOR (Pin 5 Unloaded)						
Input Bias Current @ 1.0 V Input Level on Pin 3	3	I_{IB}		0.02		μA
Maximum Internal Current Setpoint	3	I_{Limit}	0.93	1.08	1.14	V
Default Internal Current Setpoint for Skip Cycle Operation	3	I_{Lskip}		330		mV
Propagation Delay from Current Detection to Gate OFF State	3	T_{DEL}		80	130	ns
Leading Edge Blanking Duration	3	T_{LEB}		220		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. VCC_{OFF} and VCC_{ON} min−max always ensure an hysteresis of 2.0 V.
2. Minimum value for T_J = 125°C.

ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Maximum T_J = 150°C, V_{CC} = 11 V unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
INTERNAL OSCILLATOR (V_{CC} = 11 V, Pin 5 Loaded by 1.0 kΩ)						
Oscillation Frequency, 65 kHz Version 0°C ≤ T_J ≤ +125°C −40°C ≤ T_J ≤ +125°C		f_{OSC}	 58.5 57	 65 65	 71.5 75	kHz
Oscillation Frequency, 100 kHz Version 0°C ≤ T_J ≤ +125°C −40°C ≤ T_J ≤ +125°C		f_{OSC}	 90 86	 100 100	 110 120	kHz
Oscillation Frequency, 133 kHz Version 0°C ≤ T_J ≤ +125°C −40°C ≤ T_J ≤ +125°C		f_{OSC}	 120 110	 133 133	 146 160	kHz
Built−in Frequency Jittering in Percentage of f_{OSC}		f_{jitter}		±4.0		%
Maximum Duty−Cycle NCP1216 NCP1216A		D_{max}	 69 42	 75 46.5	 81 50	%
FEEDBACK SECTION (V_{CC} = 11 V, Pin 5 Loaded by 1.0 kΩ)						
Internal Pullup Resistor	2	R_{up}		20		kΩ
Pin 2 (FB) to Internal Current Setpoint Division Ratio	−	I_{ratio}		3.3		
SKIP CYCLE GENERATION						
Default Skip Mode Level	1	V_{skip}	0.9	1.1	1.26	V
Pin 1 Internal Output Impedance	1	Z_{out}		25		kΩ
INTERNAL RAMP COMPENSATION						
Internal Ramp Level @ 25°C (Note 3)	3	V_{ramp}	2.6	2.9	3.2	V
Internal Ramp Resistance to C_S Pin	3	R_{ramp}		19		kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. A 1.0 MΩ resistor is connected to the ground for the measurement.

TYPICAL CHARACTERISTICS

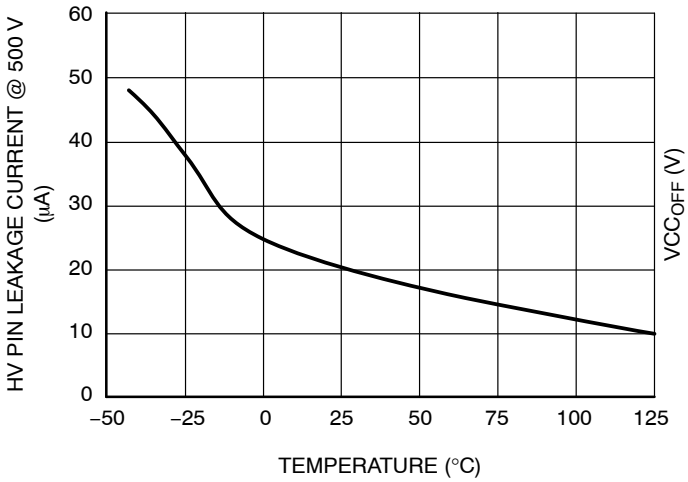


Figure 3. High Voltage Pin Leakage Current vs. Temperature

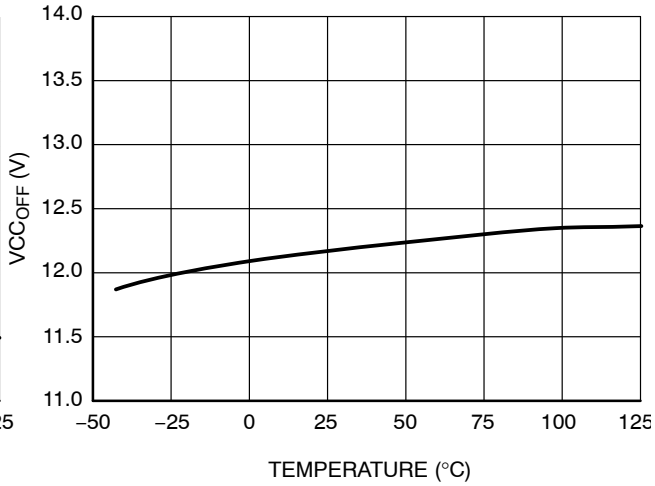


Figure 4. VCC_{OFF} vs. Temperature

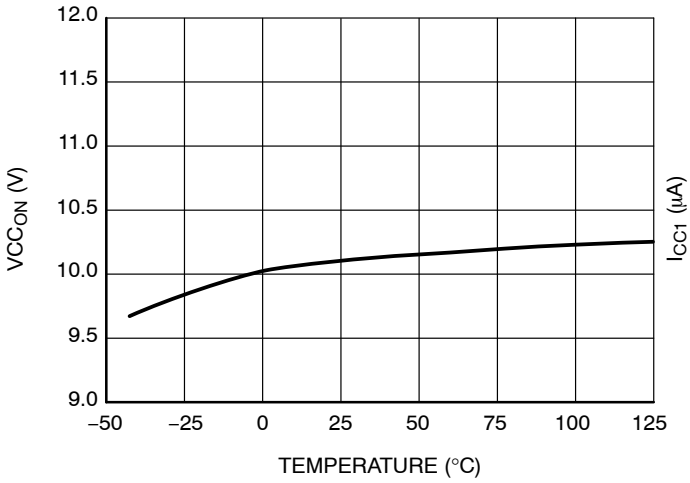


Figure 5. VCC_{ON} vs. Temperature

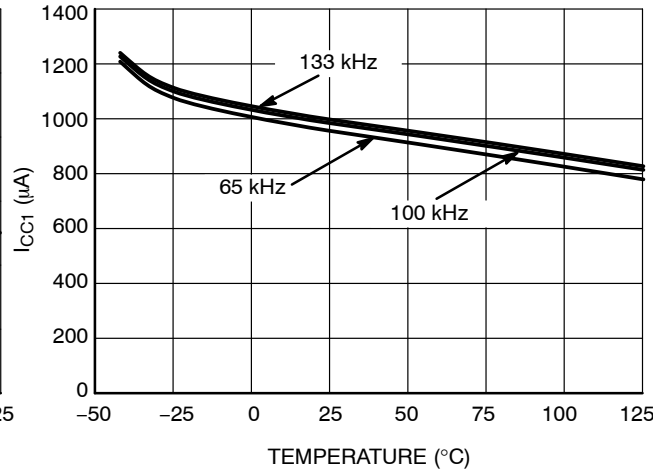


Figure 6. I_{CC1} (@ V_{CC} = 11 V) vs. Temperature

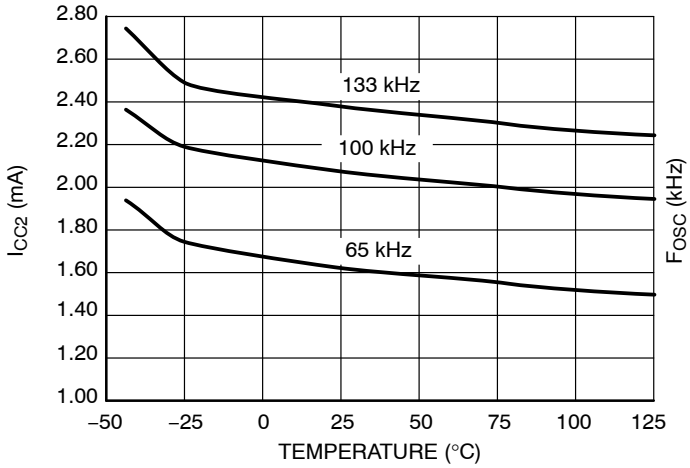


Figure 7. I_{CC2} vs. Temperature

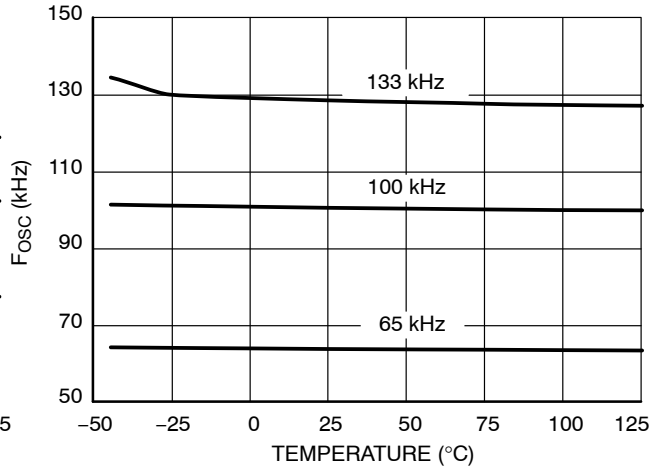


Figure 8. Switching Frequency vs. Temperature

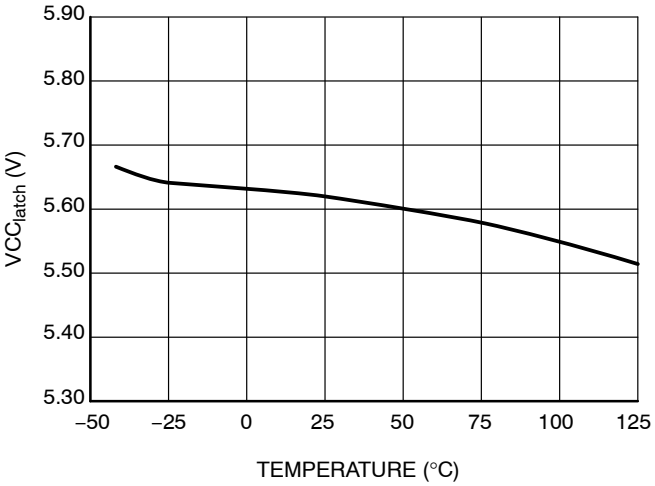


Figure 9. VCC_{latch} vs. Temperature

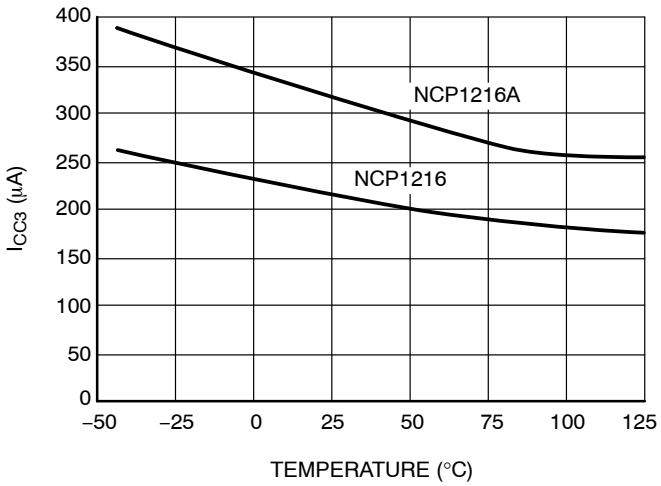


Figure 10. I_{CC3} vs. Temperature

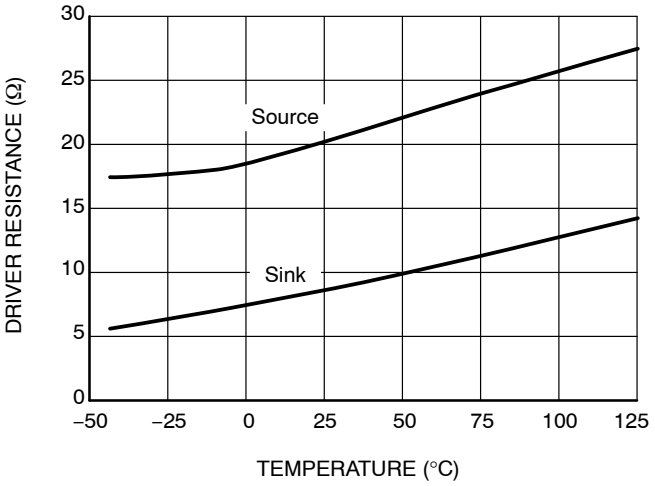


Figure 11. Drive Sink and Source Resistance vs. Temperature

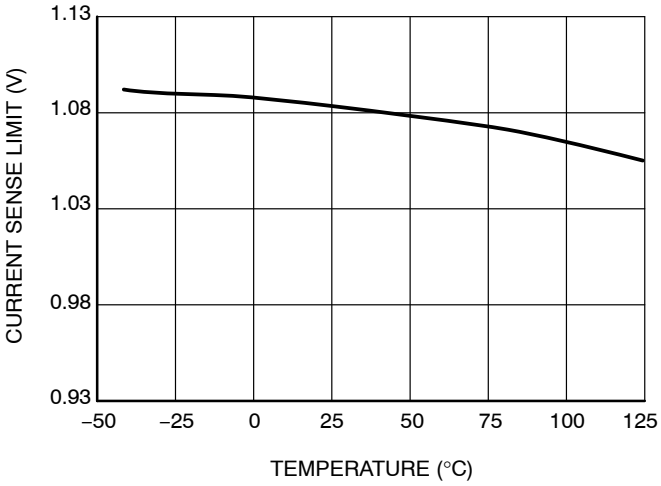


Figure 12. Current Sense Limit vs. Temperature

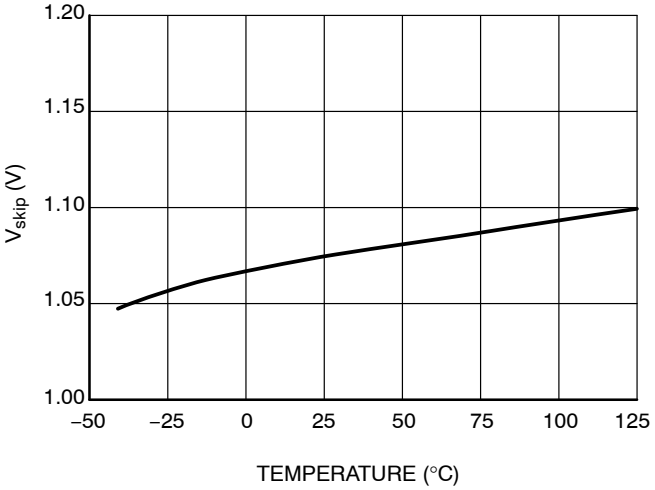


Figure 13. V_{skip} vs. Temperature

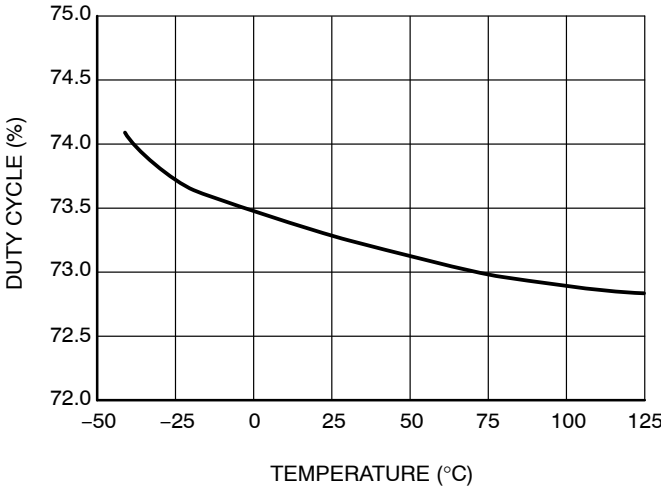


Figure 14. NCP1216 Max Duty−Cycle vs. Temperature

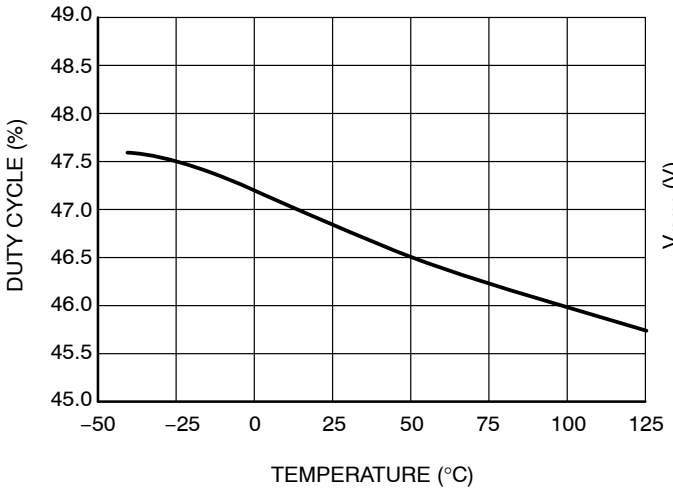


Figure 15. NCP1216A Max Duty−Cycle vs. Temperature

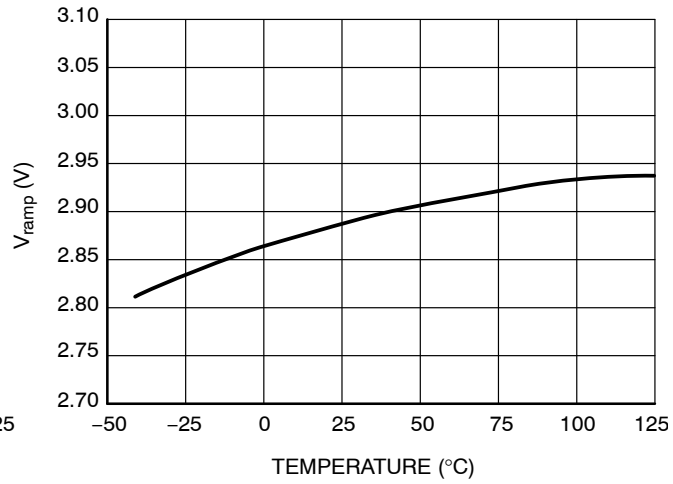


Figure 16. V_{ramp} vs. Temperature

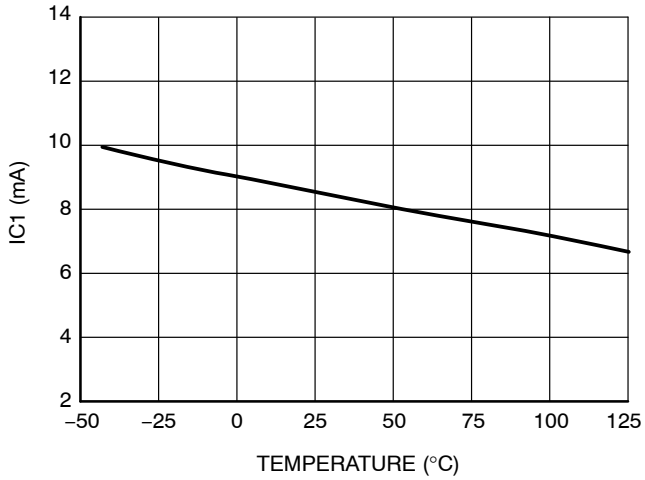


Figure 17. High Voltage Current Source (@ V_{CC} = 10 V) vs. Temperature

APPLICATION INFORMATION

Introduction

The NCP1216 implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part count is the key parameter, particularly in low−cost AC−DC adapters, TV power supplies etc. Due to its high−performance High−Voltage technology, the NCP1216 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low−pass filter and self−supply. This later point emphasizes the fact that ON Semiconductor's NCP1216 does NOT need an auxiliary winding to operate: the product is naturally supplied from the high−voltage rail and delivers a V_{CC} to the IC. This system is called the Dynamic Self−Supply (DSS):

Dynamic Self−Supply (DSS): Due to its Very High Voltage Integrated Circuit (VHVIC) technology, ON Semiconductor's NCP1216 allows for a direct pin connection to the high−voltage DC rail. A dynamic current source charges up a capacitor and thus provides a fully independent V_{CC} level to the NCP1216. As a result, there is no need for an auxiliary winding whose management is always a problem in variable output voltage designs (e.g. battery chargers).

Adjustable Skip Cycle Level: By offering the ability to tailor the level at which the skip cycle takes place, the designer can make sure that the skip operation only occurs at low peak current. This point guarantees a noise−free operation with cheap transformers. Skip cycle offers a proven mean to reduce the standby power in no or light loads situations.

Internal Frequency Dithering for Improved EMI Signature: By modulating the internal switching frequency with the DSS V_{CC} ripple, natural energy spread appears and softens the controller's EMI signature.

Wide Switching − Frequency Offered with Different Options (65 kHz − 100 kHz − 133 kHz): Depending on the application, the designer can pick up the right device to help reducing magnetics or improve the EMI signature before reaching the 150 kHz starting point.

Ramp Compensation: By inserting a resistor between the Current Sense (CS) pin and the actual sense resistor, it becomes possible to inject a given amount of ramp compensation since the internal sawtooth clock is routed to the CS pin. Sub−harmonic oscillations in Continuous Conduction Mode (CCM) can thus be compensated via a single resistor.

Over Current Protection (OCP): By continuously monitoring the FB line activity, NCP1216 enters burst mode as soon as the power supply undergoes an overload. The device enters a safe low power operation, which prevents from any lethal thermal runaway. As soon as the default disappears, the power supply resumes operation. Unlike other controllers, overload detection is performed independently of any auxiliary winding level. In presence of a bad coupling between both power and auxiliary windings, the short circuit detection can be severely affected. The DSS naturally shields you against these troubles.

Wide Duty−Cycle Operation: Wide mains operation requires a large duty−cycle excursion. The NCP1216 can go up to 75% typically. For Continuous Conduction Mode (CCM) applications, the internal ramp compensation lets you fight against sub−harmonic oscillations.

Low Standby Power: If SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping unnecessary switching cycles, the NCP1216 drastically reduces the power wasted during light load conditions. In no−load conditions, the NPC1216 allows the total standby power to easily reach next International Energy Agency (IEA) recommendations.

No Acoustic Noise While Operating: Instead of skipping cycles at high peak currents, the NCP1216 waits until the peak current demand falls below a user−adjustable 1/3 of the maximum limit. As a result, cycle skipping can take place without having a singing transformer, one can thus select cheap magnetic components free of noise problems.

External MOSFET Connection: By leaving the external MOSFET external to the IC, you can select avalanche proof devices, which in certain cases (e.g. low output powers), let you work without an active clamping network. Also, by controlling the MOSFET gate signal flow; you have an option to slow down the device commutation, therefore reducing the amount of ElectroMagnetic Interference (EMI).

SPICE Model: A dedicated model to run transient cycle−by−cycle simulations is available but also an averaged version to help you closing the loop. Ready−to−use templates can be downloaded in OrCAD's PSpice and INTUSOFT's IsSpice from ON Semiconductor web site, in the NCP1216 related section.

Dynamic Self−Supply

The DSS principle is based on the charge/discharge of the V_{CC} bulk capacitor from a low level up to a higher level. We can easily describe the current source operation with a bunch of simple logical equations:

POWER−ON: If V_{CC} < VCC_{OFF} then the Current Source is ON, no output pulses

If V_{CC} decreasing > VCC_{ON} then the Current Source is OFF, output is pulsing

If V_{CC} increasing < VCC_{OFF} then the Current Source is ON, output is pulsing

Typical values are: VCC_{OFF} = 12.2 V, VCC_{ON} = 10 V

To better understand the operational principle, Figure 18 offers the necessary light:

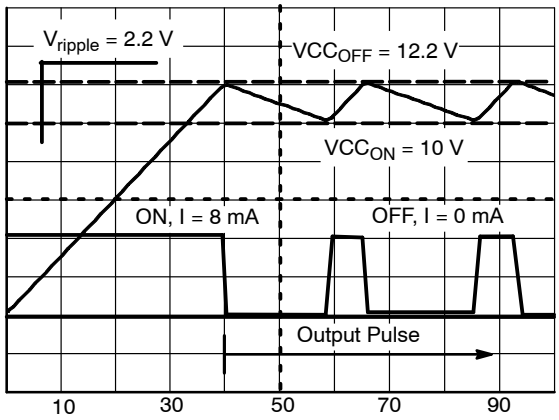


Figure 18. The Charge/Discharge Cycle Over a 10 μF V_{CC} Capacitor

The DSS behavior actually depends on the internal IC consumption and the MOSFET's gate charge Q_g. If we select a 600 V 10 A MOSFET featuring a 30 nC Q_g, then we can compute the resulting average consumption supported by the DSS which is:

$$I_{total} \approx F_{sw} \times Q_g + I_{CC1}. \quad \text{(eq. 1)}$$

The total IC heat dissipation incurred by the DSS only is given by:

$$I_{total} \times V_{pin8}. \quad \text{(eq. 2)}$$

Suppose that we select the NCP1216P065 with the above MOSFET, the total current is

$$(30\ n \times 65\ k) + 900\ \mu = 2.9\ mA. \quad \text{(eq. 3)}$$

Supplied from a 350 VDC rail (250 VAC), the heat dissipated by the circuit would then be:

$$350\ V \times 2.9\ mA = 1\ W \quad \text{(eq. 4)}$$

As you can see, it exists a tradeoff where the dissipation capability of the NCP1216 fixes the maximum Q_g that the circuit can drive, keeping its dissipation below a given target. Please see the "Power Dissipation" section for a complete design example and discover how a resistor can help to heal the NCP1216 heat equation.

Application note AND8069/D details tricks to widen the NCP1216 driving implementation, in particular for large Q_g MOSFETs. This document can be downloaded at www.onsemi.com/pub/Collateral/AND8069−D.PDF.

Ramp Compensation

Ramp compensation is a known mean to cure sub−harmonic oscillations. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−cycle greater than 50%. To lower the current loop gain, one usually injects between 50% and 100% of the inductor down−slope. Figure 19 depicts how internally the ramp is generated:

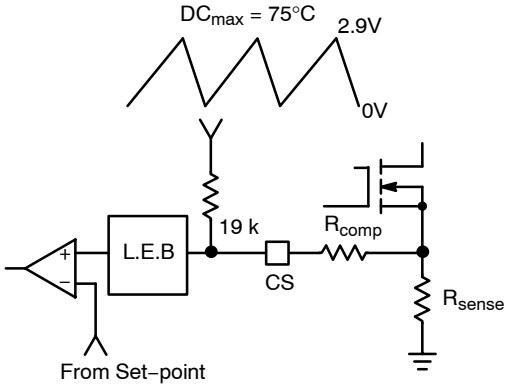


Figure 19. Inserting a Resistor in Series with the Current Sense Information brings Ramp Compensation

In the NCP1216, the ramp features a swing of 2.9 V with a Duty cycle max at 75%. Over a 65 kHz frequency, it corresponds to a

$$\frac{2.9}{0.75} \times 65\ kHz = 251\ mV/\mu s\ ramp. \quad \text{(eq. 5)}$$

In our FLYBACK design, let's suppose that our primary inductance L_p is 350 μH, delivering 12 V with a Np : Ns ratio of 1:0.1. The OFF time primary current slope is thus given by:

$$\frac{V_{out} + V_f}{L_p} \times \frac{N_p}{N_s} = 371\ mA/\mu s\ or 37\ mV/\mu s \quad \text{(eq. 6)}$$

when projected over an R_{sense} of 0.1 Ω, for instance. If we select 75% of the down−slope as the required amount of ramp compensation, then we shall inject 27 mV/μs. Our internal compensation being of 251 mV/μs, the divider ratio (divratio) between R_{comp} and the 19 kΩ is 0.107. A few lines of algebra to determine R_{comp}:

$$\frac{19\ k \times divratio}{1 - divratio} = 2.37\ k\Omega \quad \text{(eq. 7)}$$

Frequency Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. NCP1216 offers a ±4% deviation of

the nominal switching frequency whose sweep is synchronized with the V_{CC} ripple. For instance, with a 2.2 V peak−to−peak ripple, the NCP1216P065 frequency will equal 65 kHz in the middle of the ripple and will increase as V_{CC} rises or decrease as V_{CC} ramps down. Figure 20 portrays the behavior we have adopted:

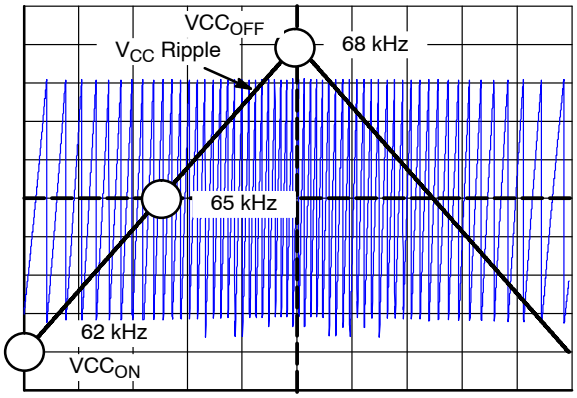


Figure 20. V_{CC} Ripple is Used to Introduce a Frequency Jittering on the Internal Oscillator Sawtooth

Skipping Cycle Mode

The NCP1216 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so−called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 22). Suppose we have the following component values:

L_p, primary inductance = 350 μH

F_{sw}, switching frequency = 65 kHz

I_p skip = 600 mA (or 333 mV / R_{sense})

The theoretical power transfer is therefore:

$$\frac{1}{2} \times L_p \times I_p^2 \times F_{sw} = 4\ W. \quad \text{(eq. 8)}$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is:

$$4 \times 0.1 = 400\ mW. \quad \text{(eq. 9)}$$

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:

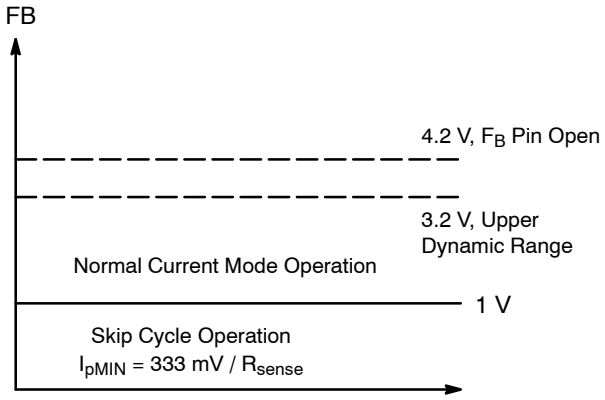


Figure 21.

When FB is above the skip cycle threshold (1.0 V by default), the peak current cannot exceed 1.0 V/R_{sense}. When the IC enters the skip cycle mode, the peak current cannot go below V_{pin1} / 3.3. The user still has the flexibility to alter this 1.0 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level. Grounding pin 1 permanently invalidates the skip cycle operation.

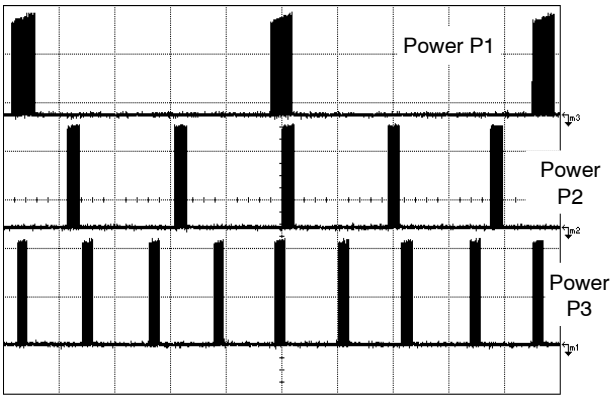


Figure 22. Output Pulses at Various Power Levels (X = 5 μs/div) P1 < P2 < P3

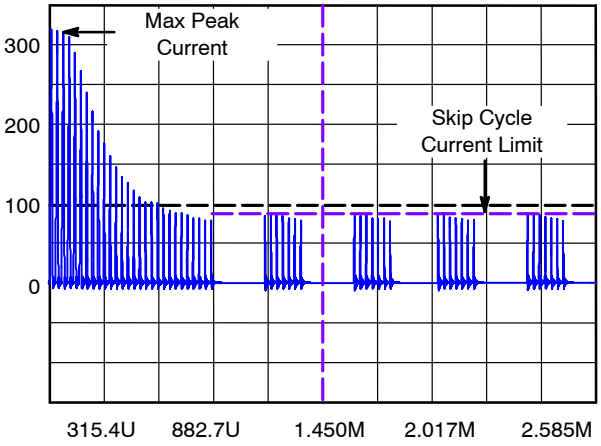


Figure 23. The Skip Cycle Takes Place at Low Peak Currents which Guarantees Noise Free Operation

Non−Latching Shutdown

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the Adj pin 1 level, the output pulses are disabled as long as FB is pulled below pin 1. As soon as FB is relaxed, the IC resumes its operation. Figure 24 depicts the application example:

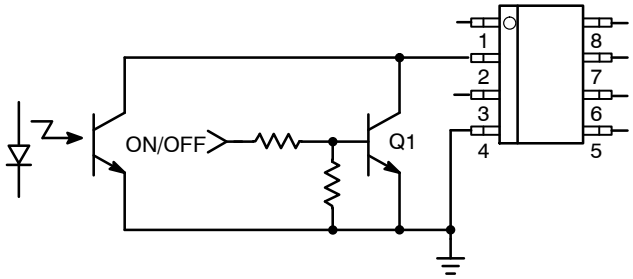


Figure 24. Another Way of Shutting Down the IC without a Definitive Latchoff State

A full latching shutdown, including overtemperature protection, is described in application note AND8069/D.

Power Dissipation

The NCP1216 is directly supplied from the DC rail through the internal DSS circuitry. The current flowing through the DSS is therefore the direct image of the NCP1216 current consumption. The total power dissipation can be evaluated using:

$$(V_{HVDC} - 11\ V) \times I_{CC2} \qquad \text{(eq. 10)}$$

which is, as we saw, directly related to the MOSFET Q_g. If we operate the device on a 90−250 VAC rail, the maximum rectified voltage can go up to 350 VDC. However, as the characterization curves show, the current consumption drops at a higher junction temperature, which quickly occurs due to the DSS operation. In our example, at $T_{ambient}$ = 50°C, I_{CC2} is measured to be 2.9 mA with a 10 A / 600 V MOSFET. As a result, the NCP1216 will dissipate from a 250 VAC network,

$$350\ V \times 2.9\ mA@T_A = 50^{\circ}C = 1\ W \qquad \text{(eq. 11)}$$

The PDIP−7 package offers a junction−to−ambient thermal resistance $R_{\theta J-A}$ of 100°C/W. Adding some copper area around the PCB footprint will help decreasing this number: 12 mm x 12 mm to drop $R_{\theta J-A}$ down to 75°C/W with 35 μ copper thickness (1 oz.) or 6.5 mm x 6.5 mm with 70 μ copper thickness (2 oz.). For a SOIC−8, the original 178°C/W will drop to 100°C/W with the same amount of copper. With this later PDIP−7 number, we can compute the maximum power dissipation that the package accepts at an ambient of 50°C:

$$P_{max} = \frac{T_{Jmax} - T_{Amax}}{R_{\theta J - A}} = 1\ W \qquad \text{(eq. 12)}$$

which barely matches our previous budget. Several solutions exist to help improving the situation:

1. Insert a Resistor in Series with Pin 8: This resistor will take a part of the heat normally dissipated by the NCP1216. Calculations of this resistor imply that V_{pin8} does not drop below 30 V in the lowest mains conditions. Therefore, R_{drop} can be selected with:

$$R_{drop} \leq \frac{V_{bulkmin} - 50\ V}{8\ mA} \qquad \text{(eq. 13)}$$

In our case, V_{bulk} minimum is 120 VDC, which leads to a dropping resistor of 8.7 kΩ. With the above example in mind, the DSS will exhibit a duty−cycle of:

$$2.9\ mA/8\ mA = 36\% \qquad \text{(eq. 14)}$$

By inserting the 8.7 kΩ resistor, we drop

$$8.7\ k\Omega * 8\ mA = 69.6\ V \qquad \text{(eq. 15)}$$

during the DSS activation. The power dissipated by the NCP1216 is therefore:

$$P_{instant} * DSS_{duty-cycle} = (350 - 69) * 8\ m * 0.36 = 800\ mW \qquad \text{(eq. 16)}$$

We can pass the limit and the resistor will dissipate

$$1\ W - 800\ mW = 200\ mW \qquad \text{(eq. 17)}$$

or

$$P_{drop} = \frac{69^2}{8.7\ k} * 0.36 \qquad \text{(eq. 18)}$$

2. Select a MOSFET with a Lower Q_g: Certain MOSFETs exhibit different total gate charges depending on the technology they use. Careful selection of this component can help to significantly decrease the dissipated heat.

3. Implement Figure 3, from AN8069/D, Solution: This is another possible option to keep the DSS functionality (good short−circuit protection and EMI jittering) while driving any types of MOSFETs. This solution is recommended when the designer plans to use SOIC−8 controllers.

4. Connect an Auxiliary Winding: If the mains conditions are such that you simply can't match the maximum power dissipation, then you need to connect an auxiliary winding to permanently disconnect the startup source.

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short−circuit protection. A short−circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the Optocoupler LED. As a result, the FB pin level is pulled up to 4.2 V, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken Optocoupler. To account for this situation, NCP1216 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty−cycle. The system auto−recovers when the fault condition disappears.

During the startup phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time−out used by this IC works with the V_{CC} decoupling capacitor: as soon as the V_{CC} decreases from the VCC_{OFF} level (typically 12.2 V) the device internally watches for an overload current situation. If this condition is still present when the VCC_{ON} level is reached, the controller stops the driving pulses, prevents the self−supply current source to restart and puts all the circuitry in standby, consuming as little as 350 μA typical (I_{CC3} parameter). As a result, the V_{CC} level slowly discharges toward 0 V. When this level crosses 5.6 V typical, the controller enters a new startup phase by turning the current source on: V_{CC} rises toward 12.2 V and again delivers output pulses at the VCC_{OFF} crossing point. If the fault condition has been removed before VCC_{ON} approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 25 shows the evolution of the signals in presence of a fault.

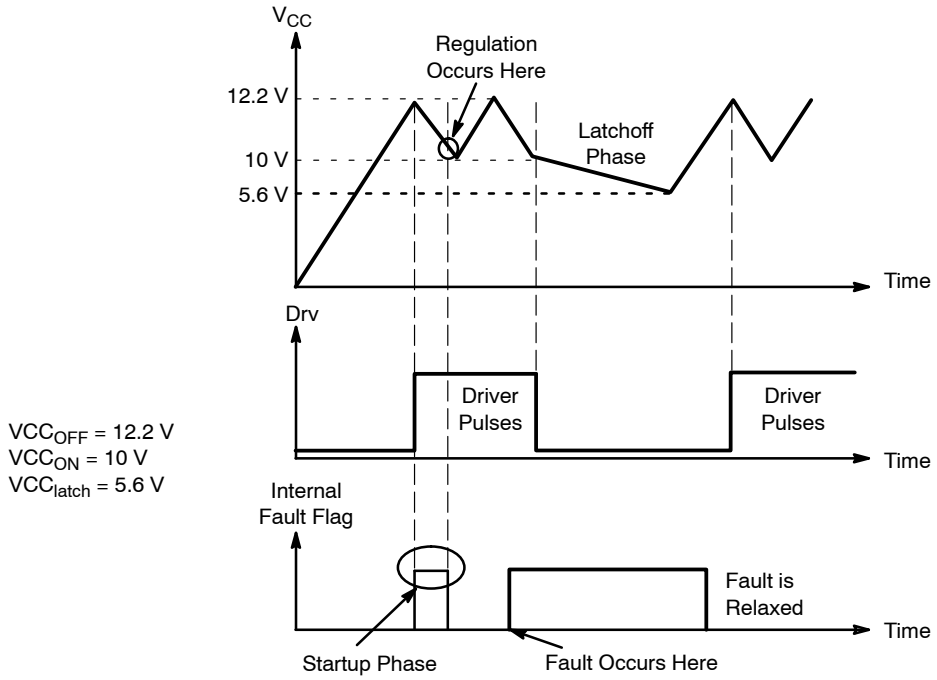


Figure 25.

If the fault is relaxed during the V_{CC} natural fall down sequence, the IC automatically resumes.

If the fault still persists when V_{CC} reached VCC_{ON}, then the controller cuts everything off until recovery.

Calculating the VCC Capacitor

As the above section describes, the fall down sequence depends upon the V_{CC} level: how long does it take for the V_{CC} line to go from 12.2 V to 10 V. The required time

depends on the startup sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 12.2 V to 10 V, otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6ms. Therefore a V_{CC} fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 2.9 mA, we can calculate the required capacitor using the following formula:

$$\Delta t = \frac{\Delta V \cdot C}{i} \qquad \text{(eq. 19)}$$

with ΔV = 2.2 V. Then for a wanted Δt of 30 ms, C equals 39.5 µF or a 68 µF for a standard value (including ±20% dispersions). When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to 350 µA typical. This happens at V_{CC} = 10 V and it remains stuck until V_{CC} reaches 5.6 V: we are in latchoff phase. Again, using the selected 68 µF and 350 µA current consumption, this latchoff phase lasts: 780 ms.

Protecting the Controller Against Negative Spikes

As with any controller built upon a CMOS technology, it is the designer's duty to avoid the presence of negative spikes on sensitive pins. Negative signals have the bad habit to forward bias the controller substrate and induce erratic behaviors. Sometimes, the injection can be so strong that internal parasitic SCRs are triggered, engendering irremediable damages to the IC if a low impedance path is offered between V_{CC} and GND. If the current sense pin is often the seat of such spurious signals, the high−voltage pin can also be the source of problems in certain circumstances. During the turn−off sequence, e.g. when the user unplugs the power supply, the controller is still fed by its V_{CC} capacitor and keeps activating the MOSFET ON and OFF with a peak current limited by R_{sense}. Unfortunately, if the quality coefficient Q of the resonating network formed by L_p and C_{bulk} is low (e.g. the MOSFET R_{dson} + R_{sense} are small), conditions are met to make the circuit resonate and thus negatively bias the controller. Since we are talking about ms pulses, the amount of injected charge, (Q = I * t), immediately latches the controller that brutally discharges its V_{CC} capacitor. If this V_{CC} capacitor is of sufficient value, its stored energy damages the controller. Figure 26 depicts a typical negative shot occurring on the HV pin where the brutal V_{CC} discharge testifies for latchup.

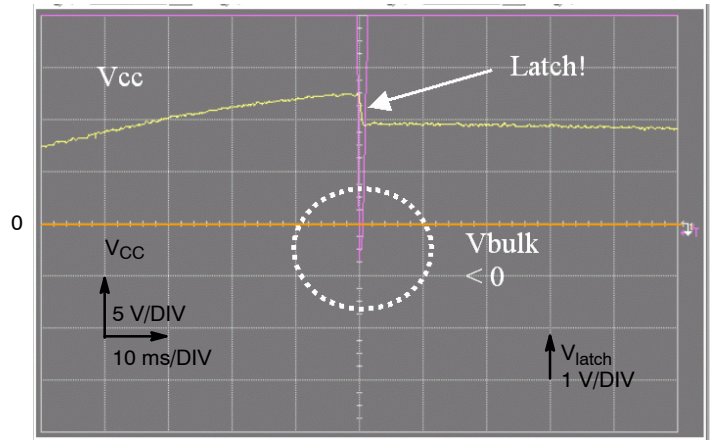


Figure 26. A Negative Spike Takes Place on the Bulk Capacitor at the Switch−off Sequence

Simple and inexpensive cures exist to prevent from internal parasitic SCR activation. One of them consists in inserting a resistor in series with the high−voltage pin to keep the negative current to the lowest when the bulk becomes negative (Figure 27). Please note that the negative spike is clamped to (−2 * V_f) due to the diode bridge. Also, the power dissipation of this resistor is extremely small since it only heats up during the startup sequence.

Another option (Figure 28) consists in wiring a diode from V_{CC} to the bulk capacitor to force V_{CC} to reach VCC_{ON} sooner and thus stops the switching activity before the bulk capacitor gets deeply discharged. For security reasons, two diodes can be connected in series.

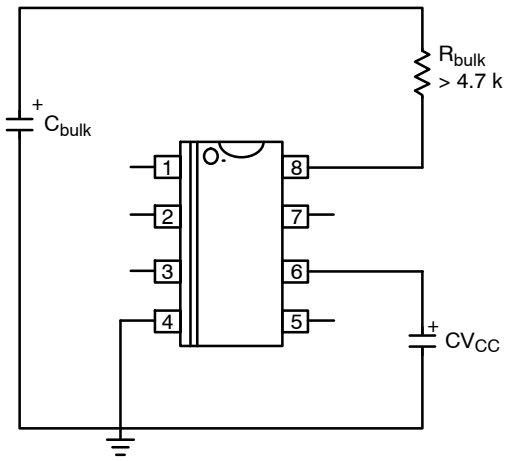


Figure 27.

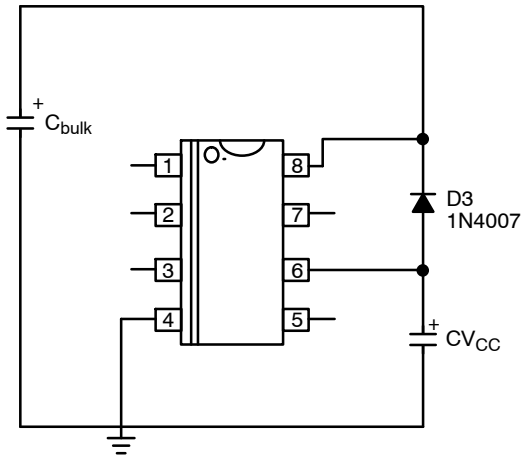


Figure 28.

A simple resistor in series avoids any latchup in the controller or one diode forces V_{CC} to reach V_{CCON} sooner.

Soft−Start − NCP1216A only

The NCP1216A features an internal 1.0 ms soft−start activated during the power on sequence (PON). As soon as V_{CC} reaches V_{CCOFF}, the peak current is gradually increased from nearly zero up to the maximum clamping level (e.g. 1.0 V). This situation lasts during 1ms and further to that time period, the peak current limit is blocked to 1.0 V until the supply enters regulation. The soft−start is also activated during the over current burst (OCP) sequence. Every restart attempt is followed by a soft−start activation. Generally speaking, the soft−start will be activated when V_{CC} ramps up either from zero (fresh power−on sequence) or 5.6 V, the latchoff voltage occurring during OCP. Figure 29 portrays the soft−start behavior. The time scales are purposely shifted to offer a better zoom portion.

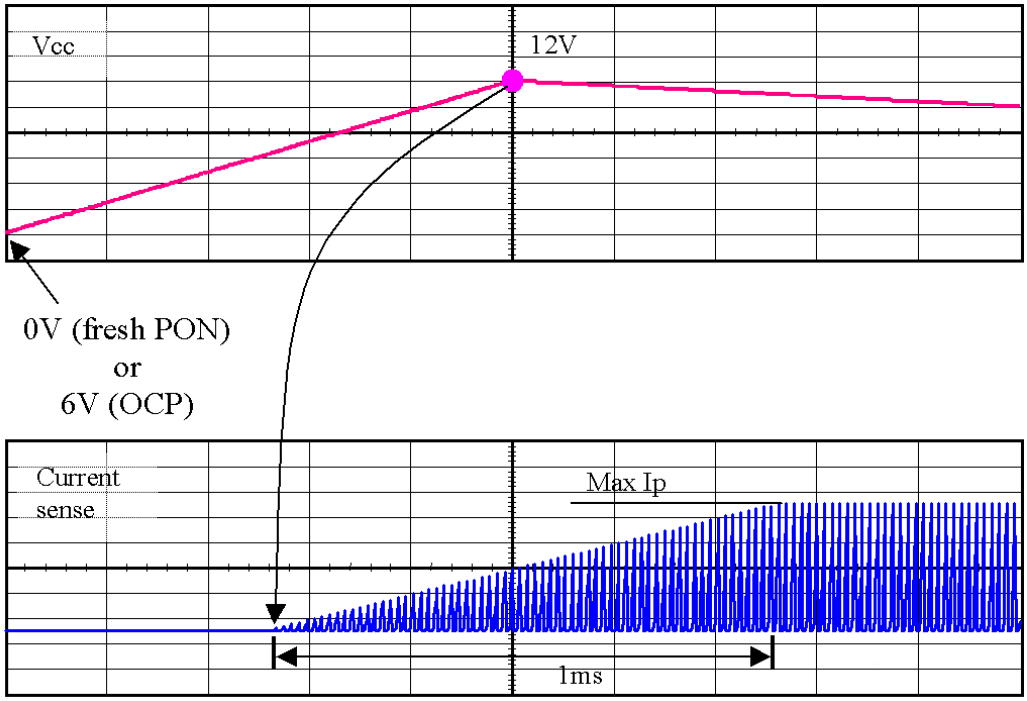


Figure 29. Soft−start is activated during a startup sequence or an OCP condition

ORDERING INFORMATION

Device	Version	Marking	Package	Shipping†
NCP1216D65R2G	65 kHz	16D06	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1216D100R2G	100 kHz	16D10	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1216D133R2G	133 kHz	16D13	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1216P65G	65 kHz	P1216P065	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1216P100G	100 kHz	P1216P100	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1216P133G	133 kHz	P1216P133	PDIP−7 (Pb−Free)	50 Units/ Rail
NCP1216AD65R2G	65 kHz	16A06	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1216AD100R2G	100 kHz	16A10	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1216AD133R2G	133 kHz	16A13	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1216AP65G	65 kHz	1216AP06	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1216AP100G	100 kHz	P1216AP10	PDIP−7 (Pb−Free)	50 Units / Rail
NCP1216AP133G	133 kHz	P1216AP13	PDIP−7 (Pb−Free)	50 Units / Rail

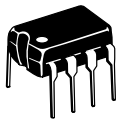
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

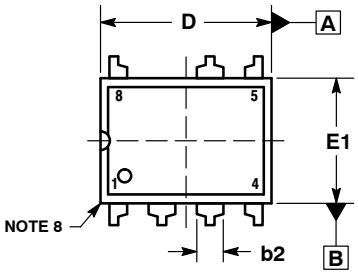
ON Semiconductor®

PDIP−7 (PDIP−8 LESS PIN 7)
CASE 626B
ISSUE D

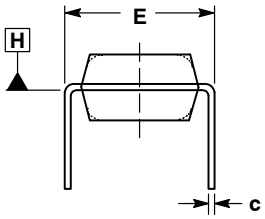
DATE 22 APR 2015



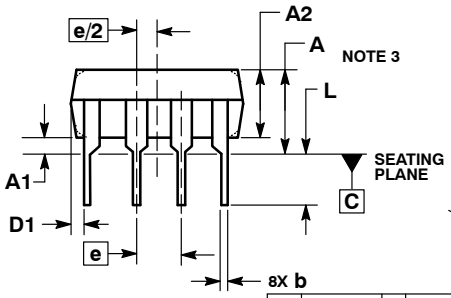
SCALE 1:1



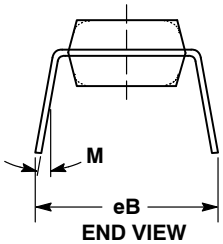
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



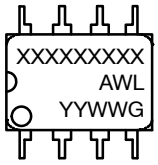
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. NOT USED
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98AON12198D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP−7 (PDIP−8 LESS PIN 7)	PAGE 1 OF 1

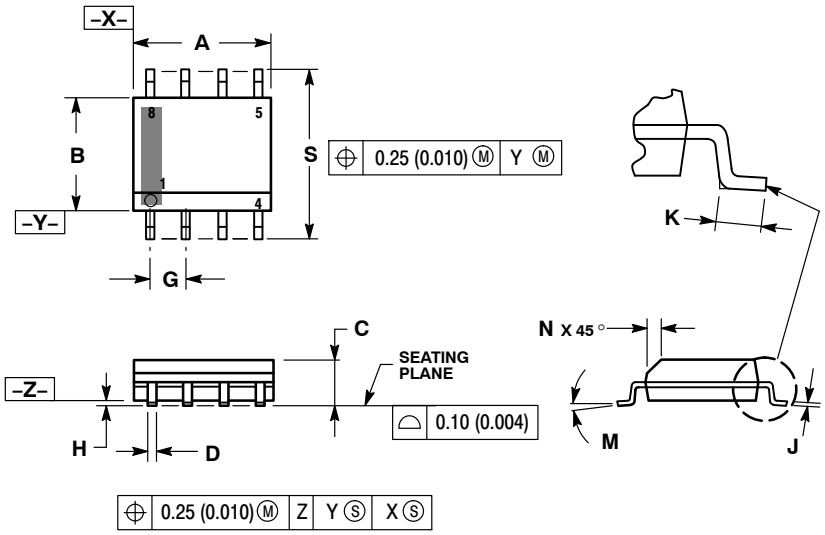
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

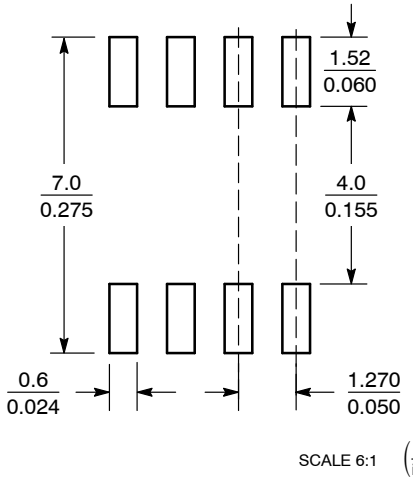
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

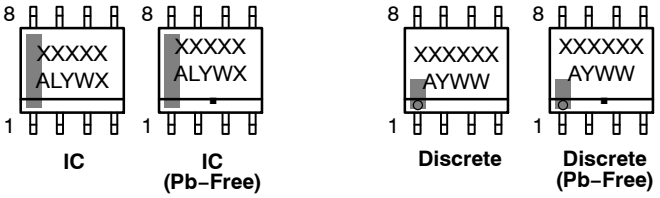
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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