eSP270D

USB 2.0 Camera Bridge Controller

BRIEF DATASHEET

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1. Introduction

eSP270D is a USB 2.0 High-speed (HS) and Full-speed (FS) compatible PC camera controller with three LDOs & a eXTAL build-in. These built-in LDOs & eXTAL can support power & system clock for CIS module and bridge chip itself. That's why eSP270D can meet the requirement in lower system BOM cost and small form factor.

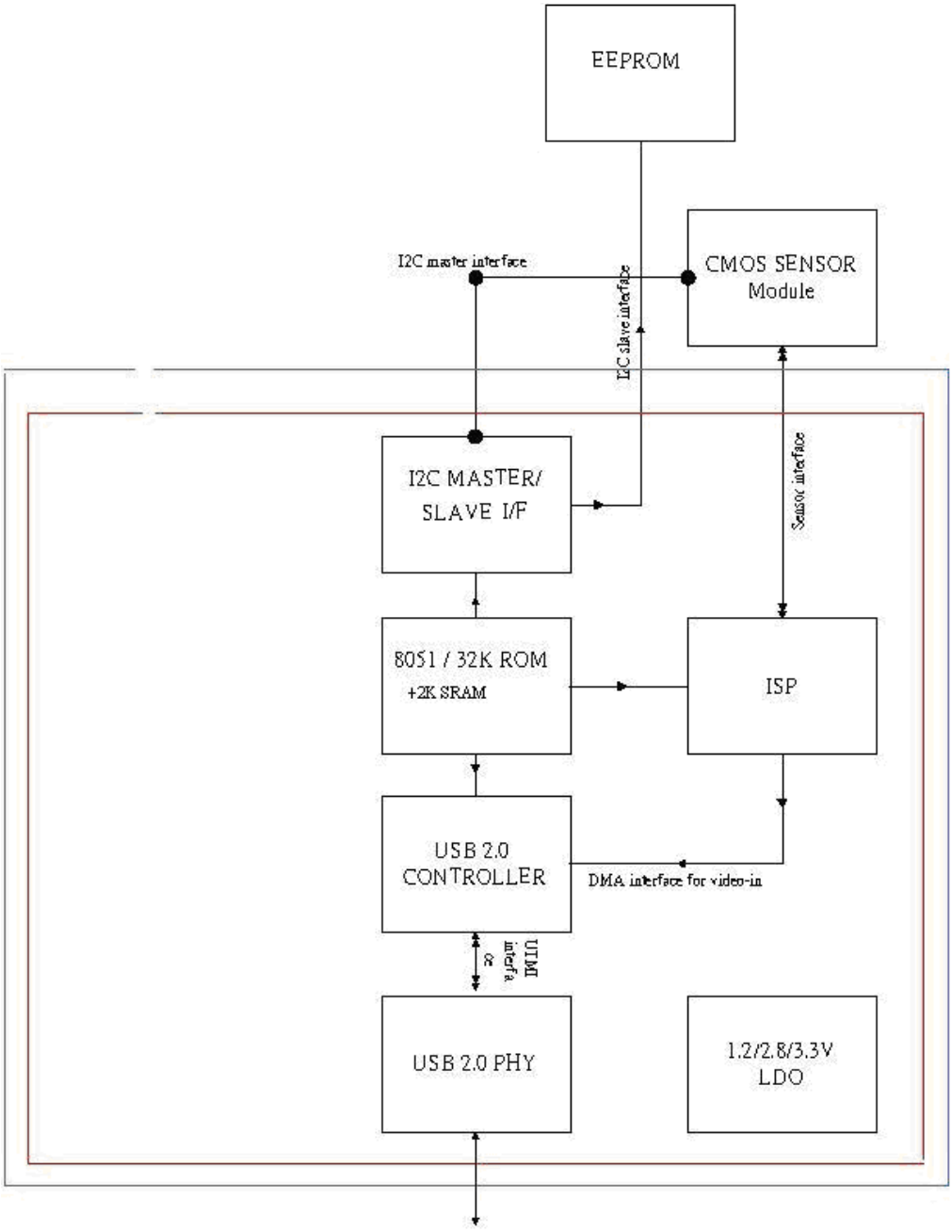


Figure 1 eSP270D Block Diagram

2. Features

- CMOS Sensor Module Interface
  - Input: 8-bit YUV422/JPEG
  - Resolution: Supports up to 8M CMOS Sensor (YUV & JPEG input)
  - Support encoded JPEG stream via bypass mode
- USB 2.0 high-speed and full-speed compatible
  - UVC 1.1
  - Support Isochronous endpoint (video, 24MB/s max.)
  - Support remote wakeup from USB event
- Embedded 8051 with 32KB mask ROM, and 2KB SRAM
  - Up to 48MHz
  - F/W upgrade to EEPROM via USB
  - Sensor support: mask ROM 2(eSP270D2) GC0307/GC0308/GC0309/GC0329/OV7670
  - Sensor support: mask ROM 3(eSP270D3) GC0307/BF3603/BF3703/BG0328/SP0838
- Control Interface
  - Support I2C master for CIS/EEPROM control
  - Support I2C slave by external HOST
- ISP functions
  - Brightness, Contrast for luminance
  - Hue, Saturation, Gain and Offset for chroma
  - Window cropping
  - Downsampling
- Single 5V power supply
  - Built-in 1.2V/3.3V LDO for core/peripheral power
  - Built-in 2.8V LDO for CIS
  - Lower power consumption: < 50mA when operation and <330uA when suspend
- Certified by Microsoft WHQL & USB-IF
- Support platforms: Window XP SP2,Window XP 64,Vista 32,Vista 64,Window 7,Windows 8,Mac and Linux with UVC driver
- Package
  - 32-QFN (4mm x 4mm eSP270Dx)

3. Pin Assignments

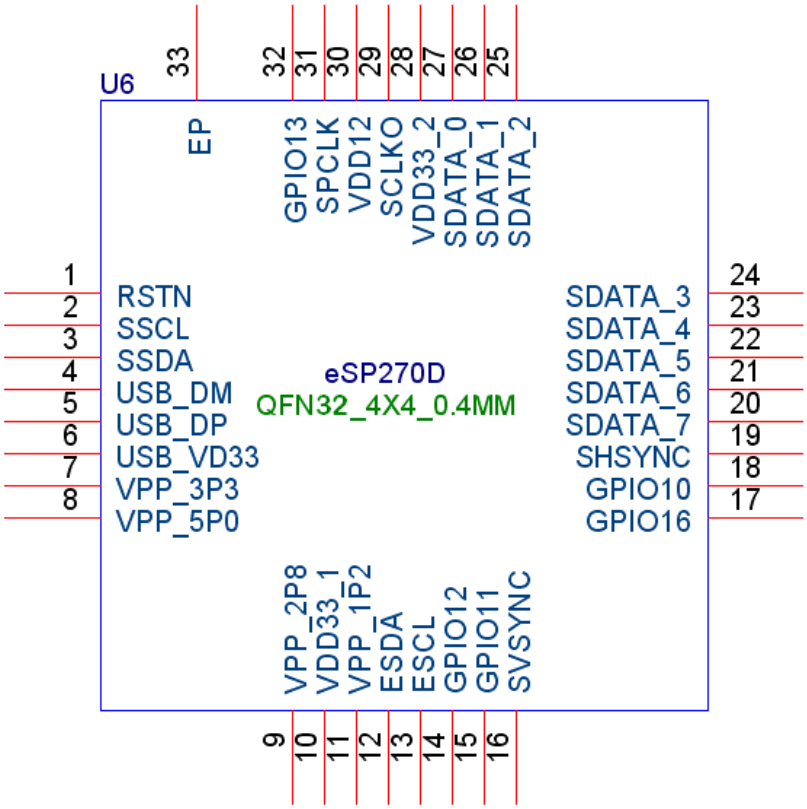


Figure 3 eSP270D Pin Assignments in 32-QFN

4. Pin Description

32-QFN eSP270D Pin Description

Pin	Pin Name	Function Description	Type	Pin	Pin Name	Function Description	Type
1	RSTN	reset, low active	IN	17	GPIO1_6	GPIO, LED indicator ctrl.	I/O
2	SSCL	I2c interface to sensor, clock	I/O	18	GPIO1_0	GPIO, snap shoot Button detection	I/O
3	SSDA	I2c interface to sensor, data	I/O	19	SHSYNC	HSYNC from sensor, to qualify the image frame	IN
4	USB_DM	USB interface, PHI negative pin	I/O	20	SDATA_7	DATA from sensor, bit7, most bit	IN
5	USB_DP	USB interface, PHI positive pin	I/O	21	SDATA_6	DATA from sensor, bit6	IN
6	USB_VD33	USB interface, Power 3.3v input	PWR	22	SDATA_5	DATA from sensor, bit5	IN
7	VPP_3P3	LDO Output, Power 3.3v out	PWR	23	SDATA_4	DATA from sensor, bit4	IN
8	VPP_5P0	LDO Input, Power 5v in	PWR	24	SDATA_3	DATA from sensor, bit3	IN
9	VPP_2P8	LDO Output, Power 2.8v out	PWR	25	SDATA_2	DATA from sensor, bit2	IN
10	VDD33	Power 3.3v in	PWR	26	SDATA_1	DATA from sensor, bit1	IN
11	VPP_1P2	LDO Output, Power 1.2v out	PWR	27	SDATA_0	DATA from sensor, bit0, last bit	IN
12	ESDA	i2c interface to EEPROM, data	I/O	28	VDD33	Power 3.3v in	PWR
13	ESCL	i2c interface to EEPROM, clock	I/O	29	SCLKO	clock output for sensor	OUT
14	GPIO1_2	GPIO, sensor reset output	I/O	30	VDD12	Power 1.2v in	PWR
15	GPIO1_1	GPIO, sensor PWDN output, default low for mask ROM 50Hz filter setting	I/O	31	SPCLK	pixel clock from sensor	IN
16	SVSYNC	VSYNC from sensor, to qualify the image frame	IN	32	GPIO1_3	GPIO, EEPROM WP ctrl.	I/O

Note: the EP(mask Exposed PAD) have to be connected Ground

Table 2: eSP270D Pin Description (32-QFN)

5. Electrical Characteristics

Absolute Maximum Ratings

Absolute Maximum Ratings						
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VPP_5P0	Supply voltage		-0.3	5.0	5.5	V
VD33P , VPP_3P3	Supply voltage		-0.3	3.3	4.0	V
VD12P, VPP_1P2	Supply voltage		-0.3	1.2	1.4	
V_{IN}	DC TTL input voltage		-0.3		DVDD+0.3	V
V_{OUT}	DC output voltage		-0.3		DVDD+0.3	V
T_{AMB}	Ambient temperature when voltage applied		-25		85	℃
T_{STG}	Storage temperature		-40		125	℃
ESD	ESD rating		MM=200 , HBM=2000			V

Recommend Operations

Recommend Operations						
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VPP_5P0	Supply voltage		4.75	5.0	5.25	V
VD33P , VPP_3P3	Supply voltage		3.1	3.3	3.6	V
VD12P, VPP_1P2	Supply Voltage		1.14	1.2	1.26	V
T_A	Operation temperature		0		70	℃
IDD	Supply current			50		mA

IO Pad Electrical Characteristics

(VDD=3.3V, Ta=25°C, unless otherwise noted)

IO PAD Electrical Characteristics						
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}		2.4 IOH=4,8,12mA			V
Output Low Voltage	V_{OL}				0.4 IOL=4,8,12mA	V

IOH and IOL are controlled by register.

6. Application Circuit

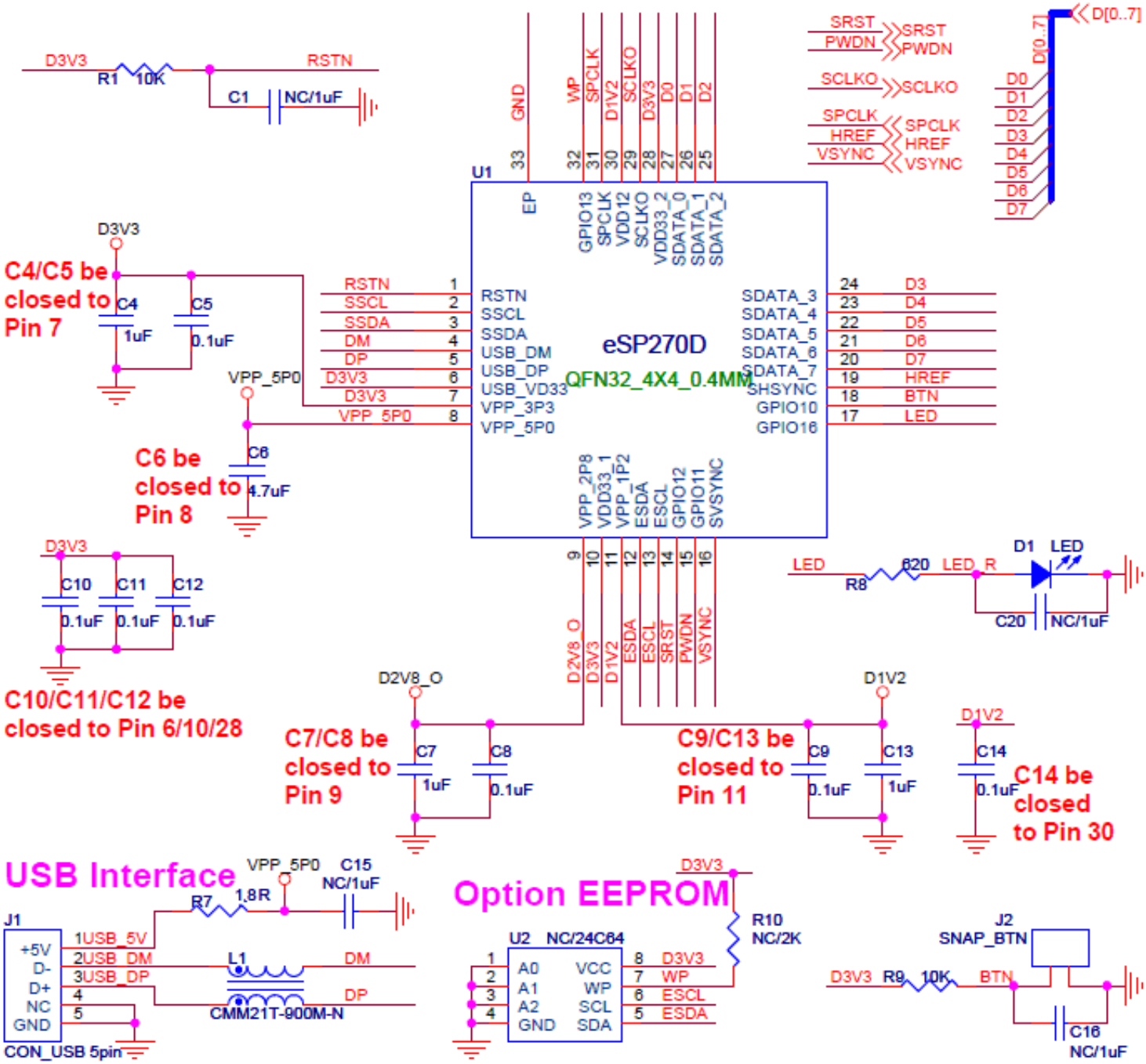
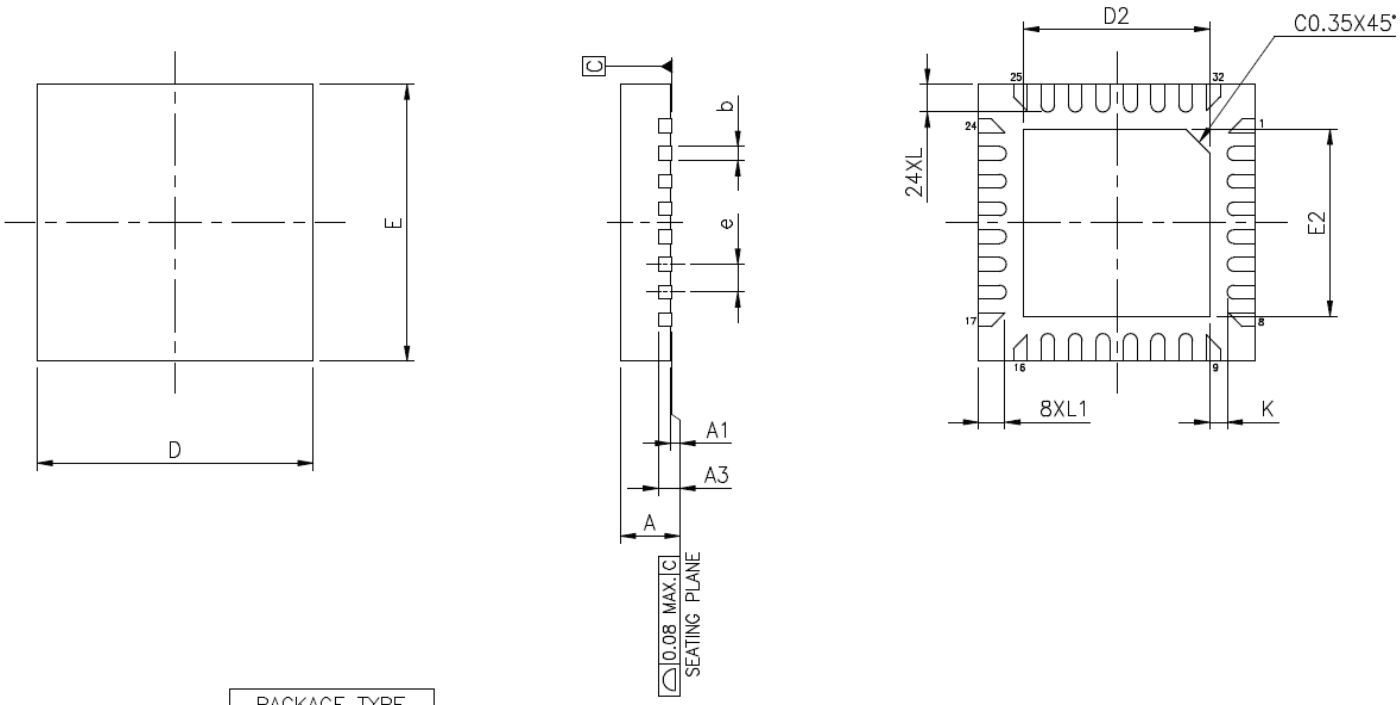


Figure 5 eSP270D Schematic(32-QFN)

7. Package Information



	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	VQFN(Y432)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	4.00 BSC		
E	4.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
L1	0.332	0.382	0.432
K	0.20	—	—

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
114X114 MIL	2.60	2.70	2.75	2.60	2.70	2.75	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 7 eSP270D Package Drawing (32-QFN)