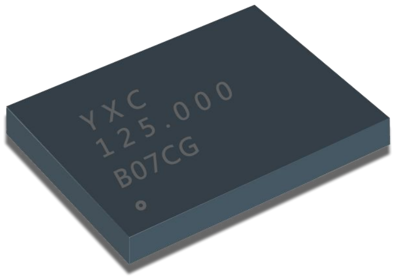
YSO8009MR



Features:

- Any frequency between 115 MHz and 137 MHz accurate to 6 decimal places
- 100% pin-to-pin drop-in replacement to quartz-based XO
- Excellent total frequency stability as low as ±20 ppm
- Operating temperature from -40°C to 85°C.
- Low power consumption of 4.9 mA typical at 1.8V
- Standby mode for longer battery life. Fast startup time of 5 ms
- LVCMOS/HCMOS compatible output
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm

Applications:

- Ideal for GPON/GPON, network switches, routers. servers, embedded systems
- Ideal for Ethernet, PCI-E, DDR, etc.

Electrical Specifications

Table 1. Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	115	–	137	MHz	
Frequency Stability and Aging						
Frequency Stability	F_stab	-20	–	+20	ppm	Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load.
		-25	–	+25	ppm	
		-50	–	+50	ppm	
Operating Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage and Current Consumption						
Supply Voltage	Vdd	1.62	1.8	1.98	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
		2.25	–	3.63	V	
Current Consumption	Idd	–	6.2	7.5	mA	No load condition, f = 125 MHz, Vdd = 2.8V, 3.0V, 3.3V or 2.25 to 3.63V
		–	5.5	6.4	mA	No load condition, f = 125 MHz, Vdd = 2.5V
		–	4.9	5.6	mA	No load condition, f = 125 MHz, Vdd = 1.8V
OE Disable Current	I_OD	–	–	4.2	mA	Vdd = 2.5V to 3.3V, OE = GND, Output in high-Z state
		–	–	4.0	mA	Vdd = 1.8V, OE = GND, Output in high-Z state
Standby Current	I_std	–	2.6	4.3	µA	$\overline{ST}$ = GND, Vdd = 2.8V to 3.3V, Output is weakly pulled down
		–	1.4	2.5	µA	$\overline{ST}$ = GND, Vdd = 2.5V, Output is weakly pulled down
		–	0.6	1.3	µA	$\overline{ST}$ = GND, Vdd = 1.8V, Output is weakly pulled down
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	All Vdds
Rise/Fall Time	Tr, Tf	–	1	2	ns	Vdd = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80%
		–	1.3	2.5	ns	Vdd =1.8V, 20% - 80%
		–	0.8	2	ns	Vdd = 2.25V - 3.63V, 20% - 80%
Output High Voltage	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.0V or 3.3V)
Output Low Voltage	VOL	–	–	10%	Vdd	IOL = 4 mA (Vdd = 3.0V or 3.3V)

Table 1. Electrical Characteristics (continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics						
Input High Voltage	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Low Voltage	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Input Pull-up Impedance	Z_in	50	87	150	kΩ	Pin 1, OE logic high or logic low, or $\overline{ST}$ logic high
		2	–	–	MΩ	Pin 1, $\overline{ST}$ logic low
Startup and Resume Timing						
Startup Time	T_start	–	–	5	ms	Measured from the time Vdd reaches its rated minimum value
Enable/Disable Time	T_oe	–	–	122	ns	f = 137 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles
Resume Time	T_resume	–	–	5	ms	Measured from the time ST pin crosses 50% threshold
Jitter						
RMS Period Jitter	T_jitt	–	1.9	3	ps	f = 125 MHz, Vdd = 2.5V, 2.8V, 3.0V or 3.3V
		–	1.8	4	ps	f = 125 MHz, Vdd = 1.8V
Peak-to-peak Period Jitter	T_pk	–	12	25	ps	f = 125 MHz, Vdd = 2.5V, 2.8V, 3.0V or 3.3V
		–	14	30	ps	f = 125 MHz, Vdd = 1.8V
RMS Phase Jitter (random)	T_phj	–	0.5	0.9	ps	Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.3	2	ps	Integration bandwidth = 12 kHz to 20 MHz

Table 2. Pin Description

Pin	Symbol	Functionality	
1	OE/ $\overline{ST}$/NC	Output Enable	H[1]: specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby	H[1]: specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.
		No Connect	Any voltage between 0 and Vdd or Open[1]: Specified frequency output. Pin 1 has no function.
2	GND	Power	Electrical ground
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage[2]

Top View

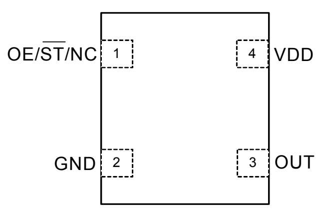


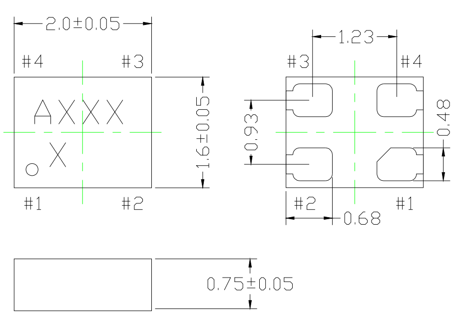
Figure 1. Pin Assignments

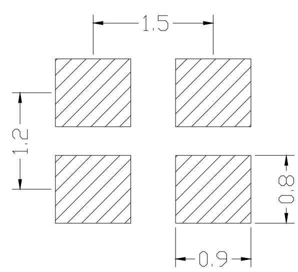
Notes:

1. In OE or $\overline{ST}$ mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
2. A capacitor of value 0.1 μF or higher between Vdd and GND is required.

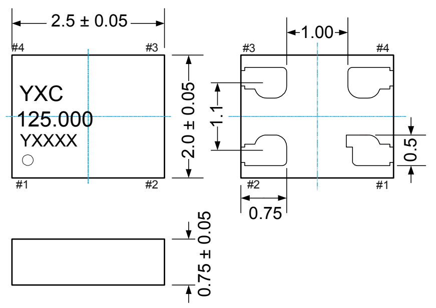
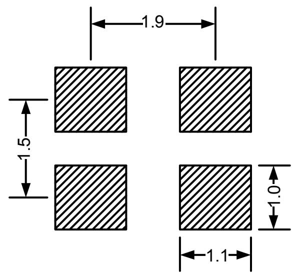
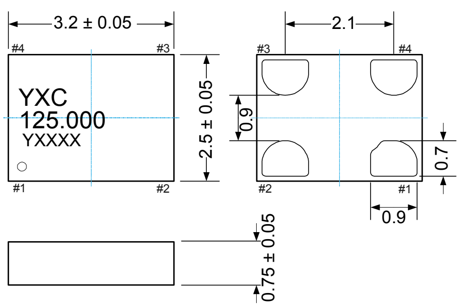
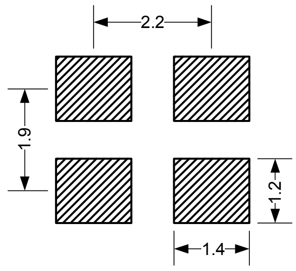
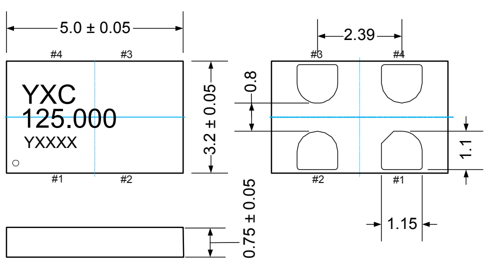
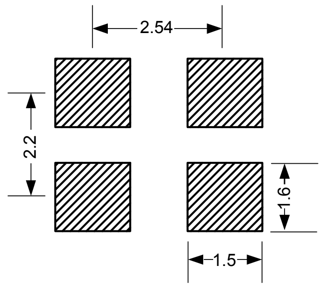
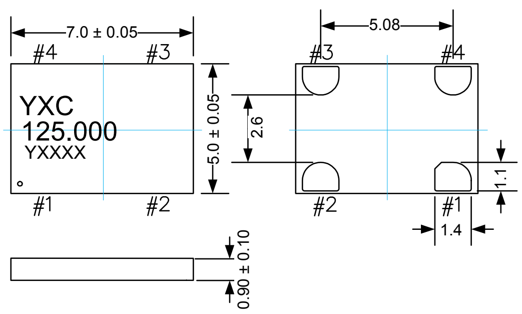
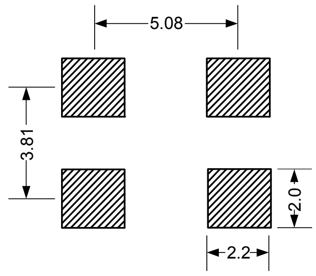
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[3]	Recommended Land Pattern (Unit: mm)[4]
2.0 x 1.6 x 0.75 mm	





Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[3]	Recommended Land Pattern (Unit: mm)[4]
2.5 x 2.0 x 0.75 mm 	
3.2 x 2.5 x 0.75 mm 	
5.0 x 3.2 x 0.75 mm 	
7.0 x 5.0 x 0.90 mm 	

Notes:

3. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
4. A capacitor of value 0.1 µF or higher between Vdd and GND is required.

PART Number Guide

Quartz Crystal Oscillator	Dimensions	Frequency (Hz)	Supply voltage (V)	Frequency Stability Overall (ppm)	Output	Pin	Material	Operating Temp. Range
O	7050	125M	E	D	H	4	M	I

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Junction Temperature[5]	–	150	°C

Note:

5. Exceeding this temperature for extended period of time may damage the device.

Table 4. Thermal Consideration[6]

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	142	273	30
5032	97	199	24
3225	109	212	27
2520	117	222	26
2016	152	252	36

Note:

6. Refer to JESD51 for θJA and θJC definitions, and reference layout used to determine the θJA and θJC values in the above table.

Table 5. Maximum Operating Junction Temperature[7]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	80°C
85°C	95°C

Note:

7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 6. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	**MIL-STD-883F, Method 2002**
Mechanical Vibration	**MIL-STD-883F, Method 2007**
Temperature Cycle	**JESD22, Method A104**
Solderability	**MIL-STD-883F, Method 2003**
Moisture Sensitivity Level	**MSL1 @ 260°C**

Test Circuit and Waveform[8]

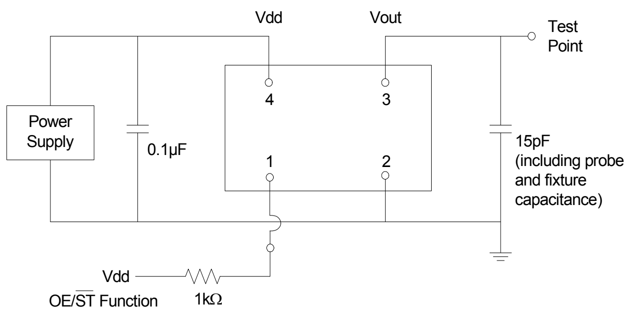


Figure 2. Test Circuit

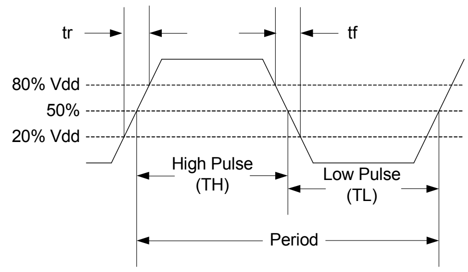
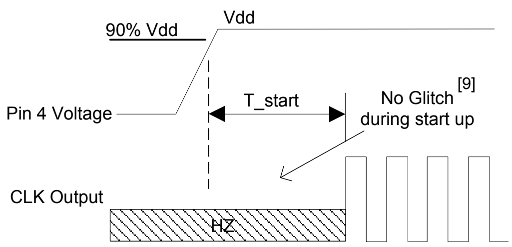


Figure 3. Waveform

Note:

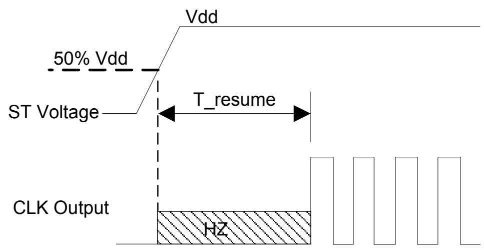
8. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams



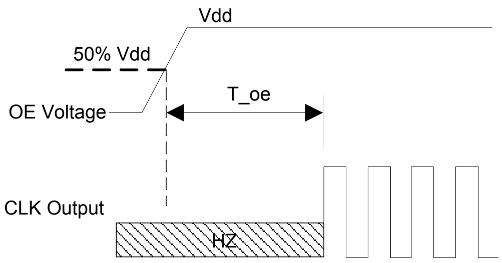
T_start: Time to start from power-off

Figure 4. Startup Timing (OE/ST Mode)



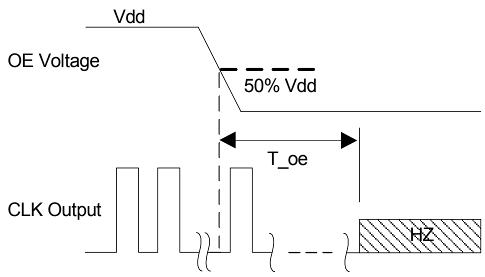
T_resume: Time to resume from ST

Figure 5. Standby Resume Timing (ST Mode Only)



T_oe: Time to re-enable the clock output

Figure 6. OE Enable Timing (OE Mode Only)



T_oe: Time to put the output in High Z mode

Figure 7. OE Disable Timing (OE Mode Only)

Note:

9. YSO8009MR has “no runt” pulses and “no glitch” output during startup or resume.

Performance Plots[10]

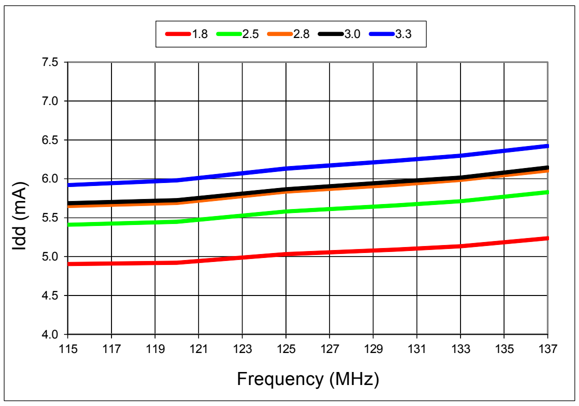


Figure 8. Idd vs Frequency

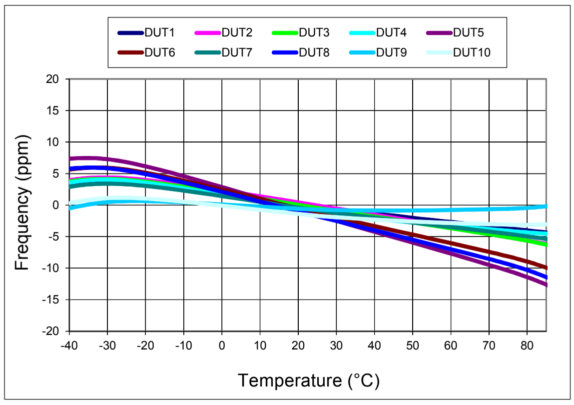


Figure 9. Frequency vs Temperature, 1.8V

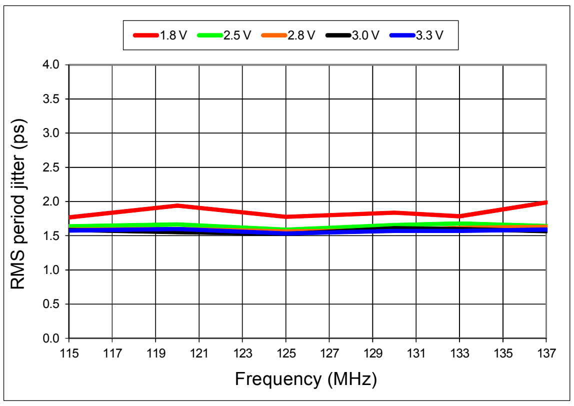


Figure 10. RMS Period Jitter vs Frequency

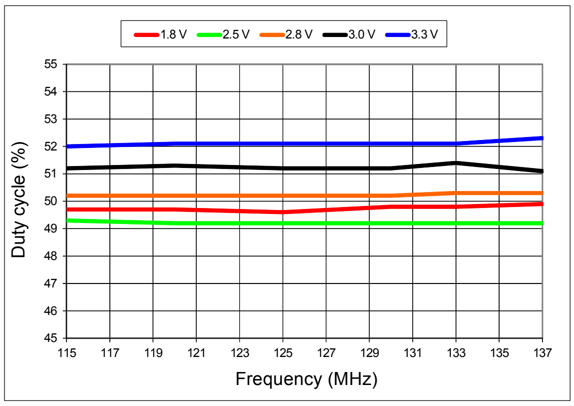


Figure 11. Duty Cycle vs Frequency

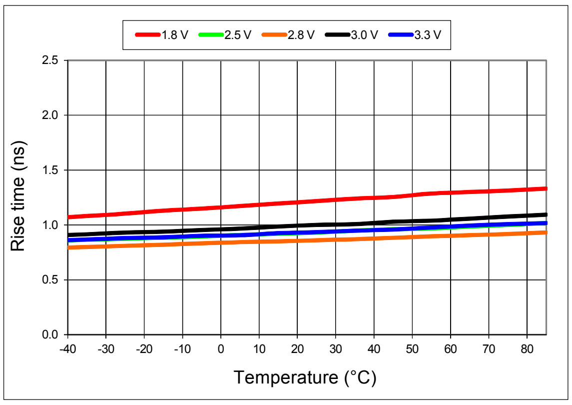


Figure 12. 20%-80% Rise Time vs Temperature

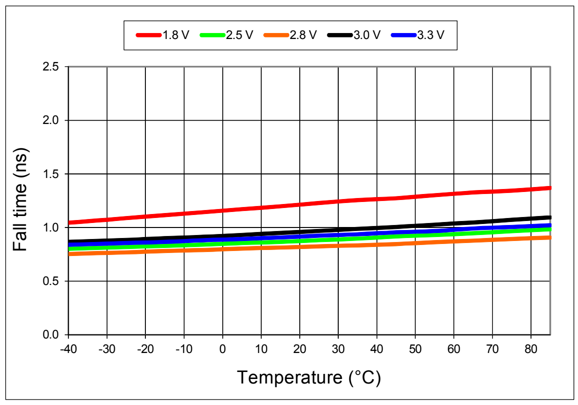


Figure 13. 20%-80% Fall Time vs Temperature

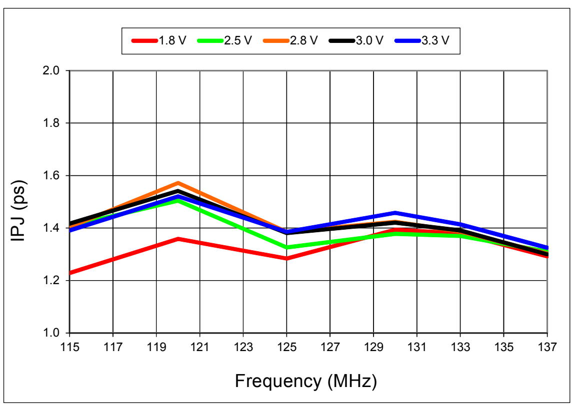


Figure 14. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency[11]

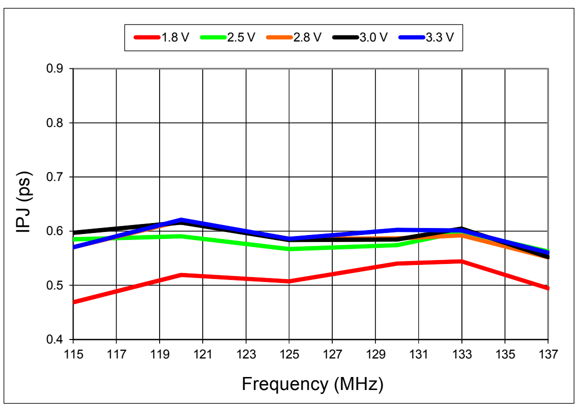


Figure 15. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency[11]

Notes:

10. All plots are measured with 15pF load at room temperature, unless otherwise stated.
11. Phase noise plots are measured with Agilent E5052B signal sorce analyzer.

Programmable Drive Strength

The YSO8009MR includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

EMI Reduction by Slowing Rise/Fall Time

Figure 16 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

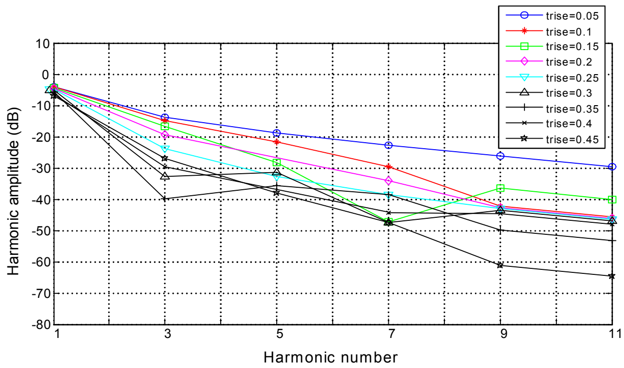


Figure 16. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V YSO8009MR device with default drive strength setting, the typical rise/fall time is 0.46ns for 5 pF output load. The typical rise/fall time slows down to1 ns when the output load increases to 15 pF. One can choose to speed up the rise/fall time to 0.72 ns by then increasing the driven strength setting on the YSO8009MR to "F."

The YSO8009MR can support up to 30 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings.Refer to the Rise/Tall Time Tables (Table 7 to 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time

YSO8009MR Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the YSO8009MR nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 30 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Rise/Fall Time (20% to 80%) vs C_{LOAD} Tables

Table 7. Vdd = 1.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)			
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF
T	0.93	n/a	n/a
E	0.78	n/a	n/a
U	0.70	1.48	n/a
F or "-": default	0.65	1.30	n/a

Table 8. Vdd = 2.5V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)			
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF
R	1.45	n/a	n/a
B	1.09	n/a	n/a
T	0.62	1.28	n/a
E	0.54	1.00	n/a
U or "-": default	0.43	0.96	n/a
F	0.34	0.88	n/a

Table 9. Vdd = 2.8V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)			
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF
R	1.29	n/a	n/a
B	0.97	n/a	n/a
T	0.55	1.12	n/a
E	0.44	1.00	n/a
U or "-": default	0.34	0.88	n/a
F	0.29	0.81	1.48

Table 10. Vdd = 3.0V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)			
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF
R	1.22	n/a	n/a
B	0.89	n/a	n/a
T or "-": default	0.51	1.00	n/a
E	0.38	0.92	n/a
U	0.30	0.83	n/a
F	0.27	0.76	1.39

Table 11. Vdd = 3.3V Rise/Fall Times for Specific C_{LOAD}

Rise/Fall Time Typ (ns)			
Drive Strength \ C_{LOAD}	5 pF	15 pF	30 pF
R	1.16	n/a	n/a
B	0.81	n/a	n/a
T or "-": default	0.46	1.00	n/a
E	0.33	0.87	n/a
U	0.28	0.79	1.46
F	0.25	0.72	1.31

Pin 1 Configuration Options (OE, $\overline{ST}$, or NC)

Pin 1 of the YSO8009MR can be factory-programmed to support three modes: Output enable (OE), standby ($\overline{ST}$) or No Connect(NC).

Output Enable (OE) Mode

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1μs.

Standby ($\overline{ST}$) Mode

In the $\overline{ST}$ mode, a device enters into the standby mode when Pin 1 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few μA. When $\overline{ST}$ is pulled High, the device goes through the “resume” process, which can take up to 5 ms.

No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and output the specified frequency regardless of the logic level on pin 1.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE, $\overline{ST}$, or NC mode.

Table 12. OE vs. $\overline{ST}$ vs. NC

	OE	$\overline{ST}$	NC
Active current 125 MHz (max, 1.8V)	5.6 mA	5.6 mA	5.6 mA
OE disable current (max. 1.8V)	4.0 mA	N/A	N/A
Standby current (typical 1.8V)	N/A	0.6 uA	N/A
OE enable time at 125 MHz (max)	124 ns	N/A	N/A
Resume time from standby (max, all frequency)	N/A	5 ms	N/A
Output driver in OE disable/standby mode	High Z	weak pull-down	N/A

Output on Startup and Resume

The YSO8009MR comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup or resume from the standby mode.In addition, the YSO8009MR has NO RUNT, NO GLITCH output during startup or resume as shown in the waveform captures in Figure 17 and Figure 18.

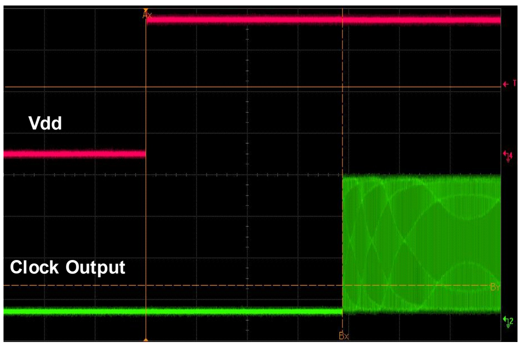


Figure 17. Startup Waveform vs. Vdd

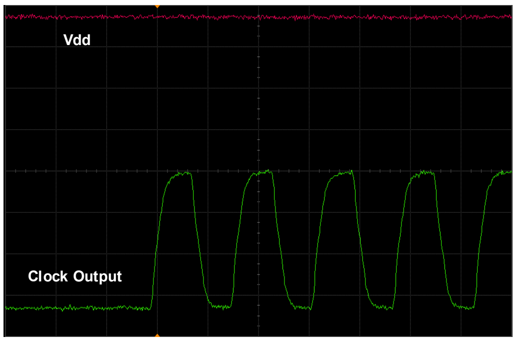


Figure 18. Startup Waveform vs. Vdd (Zoomed-in View of Figure 17)