5A, 28V INPUT, STEP DOWN SWIFT™ DC/DC CONVERTER WITH ECO-mode™

Check for Samples: TPS54531

FEATURES

- **3.5V to 28V Input Voltage Range**
- **Adjustable Output Voltage Down to 0.8V**
- **Integrated 80 mΩ High Side MOSFET Supports up to 5A Continuous Output Current**
- **High Efficiency at Light Loads with a Pulse Skipping Eco-mode™**
- **Fixed 570kHz Switching Frequency**
- **Typical 1µA Shutdown Quiescent Current**
- **Adjustable Slow Start Limits Inrush Currents**
- **Programmable UVLO Threshold**
- **Overvoltage Transient Protection**
- **Cycle-by-Cycle Current Limit, Frequency Fold Back and Thermal Shutdown Protection**
- **Available in Easy-to-Use Thermally Enhanced SOIC8 PowerPAD™ Package**

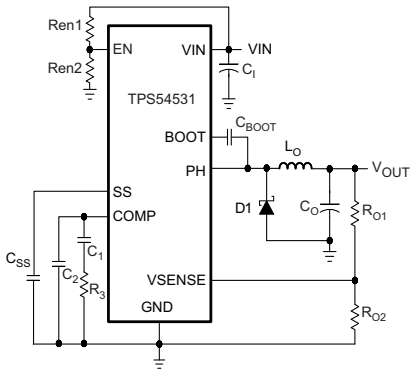
APPLICATIONS

- **Consumer Applications such as Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers**
- **Industrial and Car Audio Power Supplies**
- **5V, 12V and 24V Distributed Power Systems**

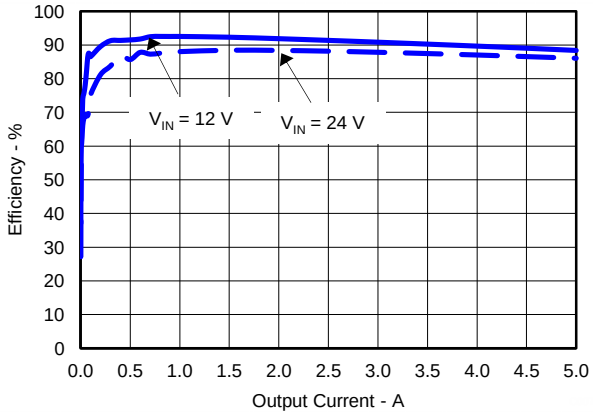
DESCRIPTION

The TPS54531 is a 28-V, 5-A non-synchronous buck converter that integrates a low $R_{DS(on)}$ high side MOSFET. To increase efficiency at light loads, a pulse skipping Eco-mode™ feature is automatically activated. Furthermore, the 1 µA shutdown supply current allows the device to be used in battery powered applications. Current mode control with internal slope compensation simplifies the external compensation calculations and reduces component count while allowing the use of ceramic output capacitors. A resistor divider programs the hysteresis of the input under-voltage lockout. An overvoltage transient protection circuit limits voltage overshoots during startup and transient conditions. A cycle by cycle current limit scheme, frequency fold back and thermal shutdown protect the device and the load in the event of an overload condition. The TPS54531 is available in 8-pin SOIC PowerPAD™ package that have been internally optimized to improve thermal performance.

SIMPLIFIED SCHEMATIC



EFFICIENCY TPS54531



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Eco-mode, PowerPAD are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

For additional design needs, see:

	TPS54231	TPS54232	TPS54233	TPS54531	TPS54332
I_O(Max)	2A	2A	2A	5A	3.5A
Input Voltage Range	3.5V - 28V	3.5V - 28V	3.5V - 28V	3.5V - 28V	3.5V - 28V
Switching Freq. (Typ)	570kHz	1000kHz	285kHz	570kHz	1000kHz
Switch Current Limit (Min)	2.3A	2.3A	2.3A	5.5A	4.2A
Pin/Package	8SOIC	8SOIC	8SOIC	8SO PowerPAD™	8SO PowerPAD™

ORDERING INFORMATION(1)

T_J	PACKAGE	SWITCHING FREQUENCY	PART NUMBER(2)
–40°C to 150°C	8 pin SOIC PowerPAD™	570 kHz	TPS54531DDA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The DDA package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54531DDAR). See applications section of data sheet for layout information.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input Voltage	VIN	–0.3 to 30	V
	EN	–0.3 to 6	
	BOOT	38	
	VSENSE	–0.3 to 3	
	COMP	–0.3 to 3	
	SS	–0.3 to 3	
Output Voltage	BOOT-PH	8	V
	PH	–0.6 to 30	
	PH (10 ns transient from ground to negative peak)	–5	
Source Current	EN	100	µA
	BOOT	100	mA
	VSENSE	10	µA
	PH	Current Limit	A
Sink Current	VIN	Current Limit	A
	COMP	100	µA
	SS	200	
Electrostatic Discharge	Human body model (HBM)	2	kV
	Charged device model (CDM)	1	kV
Operating Junction Temperature		–40 to 150	°C
Storage Temperature		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS(1) (2) (3)

PACKAGE	THERMAL IMPEDANCE JUNCTION TO AMBIENT	PSEUDO THERMAL IMPEDANCE JUNCTION TO TOP
SOIC8 PowerPAD™	50°C/W	5°C/W

(1) Maximum power dissipation may be limited by overcurrent protection
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 150°C for best performance and long-term reliability. See *power dissipation estimate* in application section of this data sheet for more information.
(3) Test board conditions:
(a) 2 inches x 1.5 inches, 2 layers, thickness: 0.062 inch
(b) 2-ounce copper traces located on the top and bottom of the PCB
(c) 6 thermal vias located under the device package

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Operating Input Voltage on (VIN pin)	3.5		28	V
Operating junction temperature, T_J	–40		150	°C

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 150°C, VIN = 3.5V to 28V (unless otherwise noted)

DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Internal undervoltage lockout threshold	Rising and Falling			3.5	V
Shutdown supply current	EN = 0V, VIN = 12V, –40°C to 85°C		1	4	µA
Operating – non switching supply current	VSENSE = 0.85 V		110	190	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising and Falling		1.25	1.35	V
Input current	Enable threshold – 50 mV		-1		µA
Input current	Enable threshold + 50 mV		-4		µA
VOLTAGE REFERENCE					
Voltage reference		0.772	0.8	0.828	V
HIGH-SIDE MOSFET					
On resistance	BOOT-PH = 3 V, VIN = 3.5 V		115	200	mΩ
	BOOT-PH = 6 V, VIN = 12 V		80	150	
ERROR AMPLIFIER					
Error amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		92		µmhos
Error amplifier DC gain(1)	VSENSE = 0.8 V		800		V/V
Error amplifier unity gain bandwidth(1)	5 pF capacitance from COMP to GND pins		2.7		MHz
Error amplifier source/sink current	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±7		µA
Switch current to COMP transconductance(1)	VIN = 12 V		20		A/V
SWITCHING FREQUENCY					
Switching Frequency	VIN = 12V, 25°C	456	570	684	kHz
Minimum controllable on time	VIN = 12V, 25°C		105	130	ns
Maximum controllable duty ratio(1)	BOOT-PH = 6 V	90%	93%		
PULSE SKIPPING ECO-MODE™					
Pulse skipping Eco-mode™ switch current threshold			160		mA
CURRENT LIMIT					
Current limit threshold	VIN = 12 V	6.3	10.5		A

(1) Specified by design

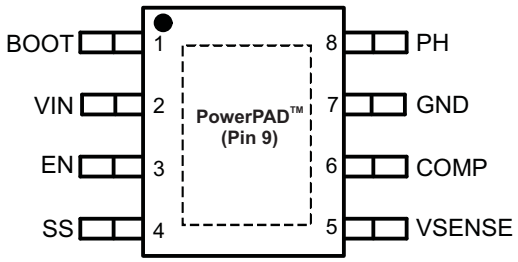
ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 150°C, VIN = 3.5V to 28V (unless otherwise noted)

DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal Shutdown			165		°C
SLOW START (SS PIN)					
Charge current	$V_{(SS)}$ = 0.4 V		2		µA

DEVICE INFORMATION

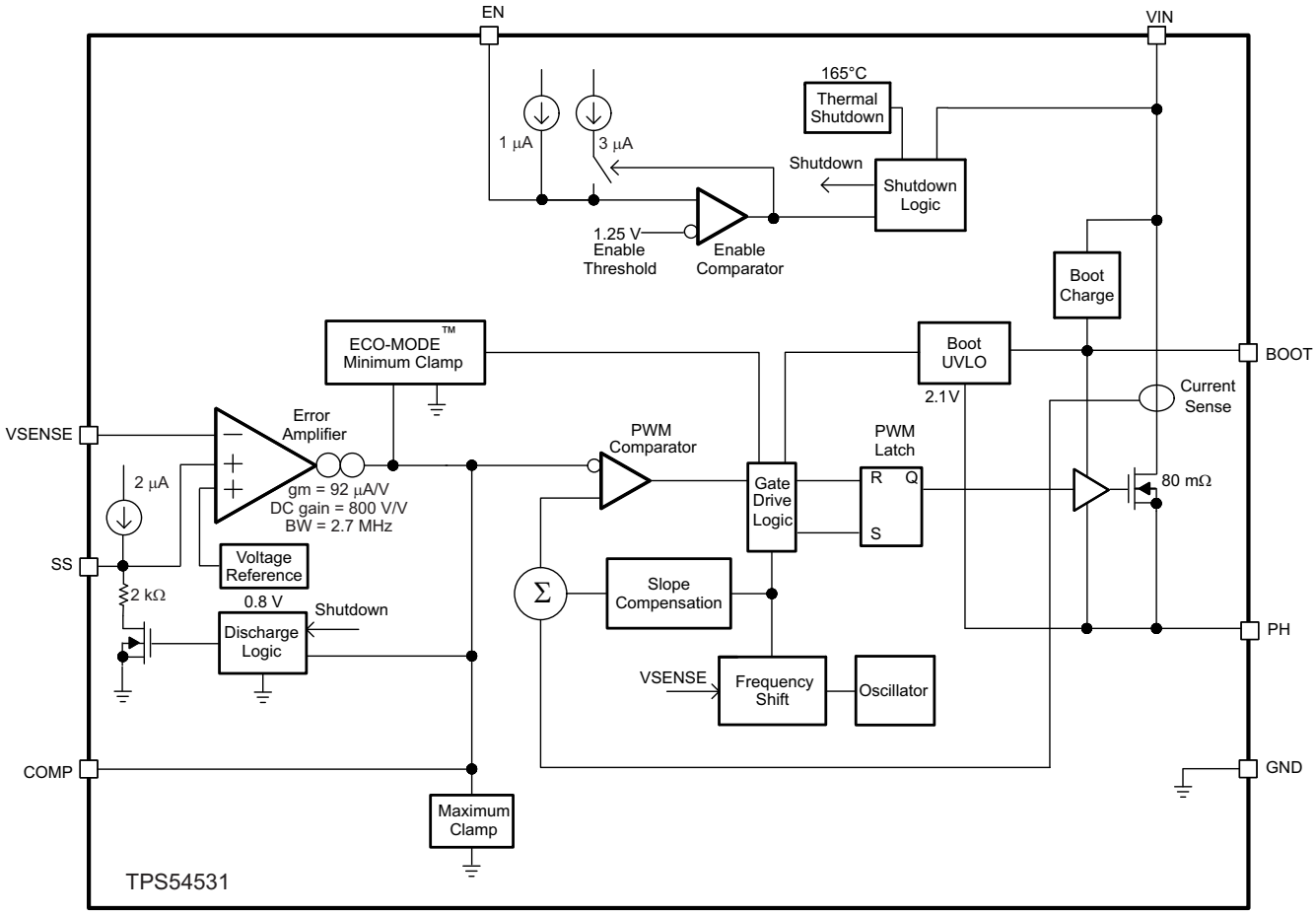
PIN ASSIGNMENTS
DDA PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
BOOT	1	A 0.1 µF bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor falls below the minimum requirement, the high-side MOSFET is forced to switch off until the capacitor is refreshed.
VIN	2	Input supply voltage, 3.5 V to 28 V.
EN	3	Enable pin. Pull below 1.25V to disable. Float to enable. Programming the input undervoltage lockout with two resistors is recommended.
SS	4	Slow start pin. An external capacitor connected to this pin sets the output rise time.
VSENSE	5	Inverting node of the gm error amplifier.
COMP	6	Error amplifier output, and input to the PWM comparator. Connect frequency compensation components to this pin.
GND	7	Ground.
PH	8	The source of the internal high-side power MOSFET.
PowerPAD™	9	GND pin must be connected to the exposed pad for proper operation. This pin is only available in the DDA package.

FUNCTIONAL BLOCK DIAGRAM



CHARACTERIZATION CURVES

ON RESISTANCE vs JUNCTION TEMPERATURE

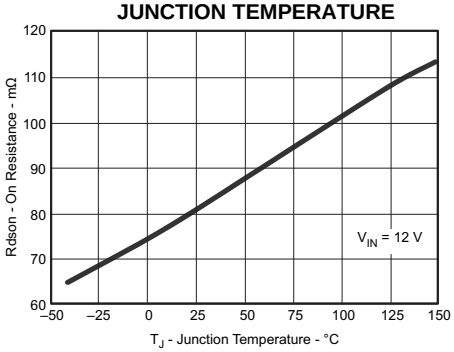


Figure 1.

SHUTDOWN QUIESCENT CURRENT vs INPUT VOLTAGE

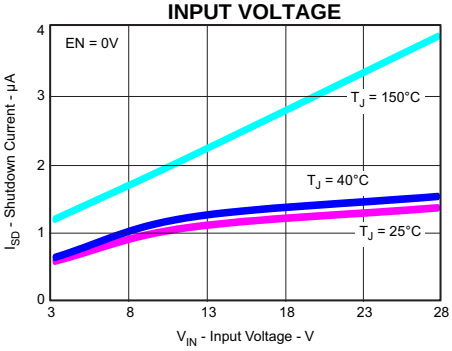


Figure 2.

SWITCHING FREQUENCY vs JUNCTION TEMPERATURE

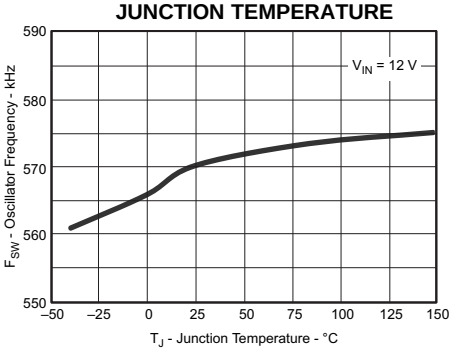


Figure 3.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

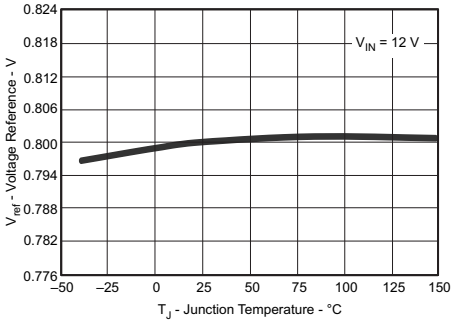


Figure 4.

MINIMUM CONTROLLABLE ON TIME vs JUNCTION TEMPERATURE

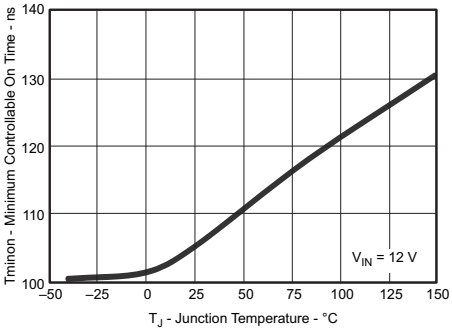


Figure 5.

MINIMUM CONTROLLABLE DUTY RATIO vs JUNCTION TEMPERATURE

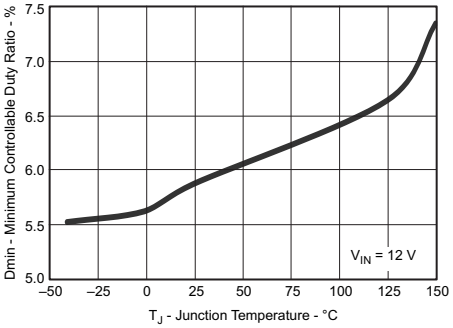


Figure 6.

SS CHARGE CURRENT vs JUNCTION TEMPERATURE

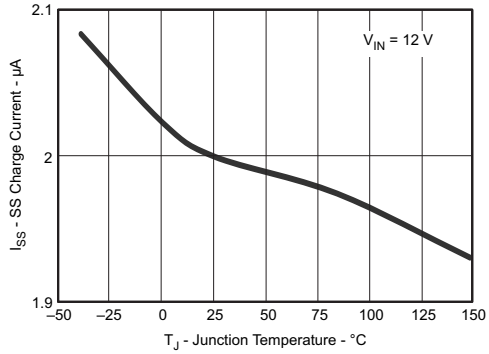


Figure 7.

CURRENT LIMIT THRESHOLD vs INPUT VOLTAGE

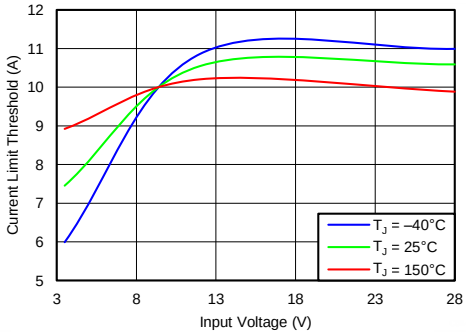


Figure 8.

OVERVIEW

The TPS54531 is a 28-V, 5-A, step-down (buck) converter with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The TPS54531 has a pre-set switching frequency of 570kHz.

The TPS54531 needs a minimum input voltage of 3.5V to operate normally. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under-voltage lockout (UVLO) with two external resistors. In addition, the pull-up current provides a default condition when the EN pin is floating for the device to operate. The operating current is 110 μA typically when not switching and under no load. When the device is disabled, the supply current is 1μA typically.

The integrated 80 mΩ high-side MOSFET allows for high efficiency power supply designs with continuous output currents up to 5A.

The TPS54531 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1V typically. The output voltage can be stepped down to as low as the reference voltage.

By adding an external capacitor, the slow start time of the TPS54531 can be adjustable which enables flexible output filter selection.

To improve the efficiency at light load conditions, the TPS54531 enters a special pulse skipping Eco-mode™ when the peak inductor current drops below 160mA typically.

The frequency foldback reduces the switching frequency during startup and over current conditions to help control the inductor current. The thermal shut down gives the additional protection under fault conditions.

DETAILED DESCRIPTION

FIXED FREQUENCY PWM CONTROL

The TPS54531 uses a fixed frequency, peak current mode control. The internal switching frequency of the TPS54531 is fixed at 570kHz.

ECO-MODE™

The TPS54531 is designed to operate in pulse skipping Eco-mode™ at light load currents to boost light load efficiency. When the peak inductor current is lower than 160 mA typically, the COMP pin voltage falls to 0.5 V typically and the device enters Eco-mode™ . When the device is in Eco-mode™, the COMP pin voltage is clamped at 0.5V internally which prevents the high side integrated MOSFET from switching. The peak inductor current must rise above 160mA for the COMP pin voltage to rise above 0.5V and exit Eco-mode™. Since the integrated current comparator catches the peak inductor current only, the average load current entering Eco-mode™ varies with the applications and external output filters.

VOLTAGE REFERENCE (V_{ref})

The voltage reference system produces a ±2% initial accuracy voltage reference (±3.5% over temperature) by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.8V.

BOOTSTRAP VOLTAGE (BOOT)

The TPS54531 has an integrated boot regulator and requires a 0.1 μF ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS54531 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.1 V typically.

ENABLE AND ADJUSTABLE INPUT UNDER-VOLTAGE LOCKOUT (VIN UVLO)

The EN pin has an internal pull-up current source that provides the default condition of the TPS54531 operating when the EN pin floats.

The TPS54531 is disabled when the VIN pin voltage falls below internal VIN UVLO threshold. It is recommended to use an external VIN UVLO to add at least 500 mV Hysteresis unless VIN is greater than (V_{OUT} + 2 V). To adjust the VIN UVLO with Hysteresis, use the external circuitry connected to the EN pin as shown in Figure 9. Once the EN pin voltage exceeds 1.25 V, an additional 3 µA of hysteresis is added. Use Equation 1 and Equation 2 to calculate the resistor values needed for the desired VIN UVLO threshold voltages. The V_{START} is the input start threshold voltage, the V_{STOP} is the input stop threshold voltage and the V_{EN} is the enable threshold voltage of 1.25 V. The V_{STOP} should always be greater than 3.5 V.

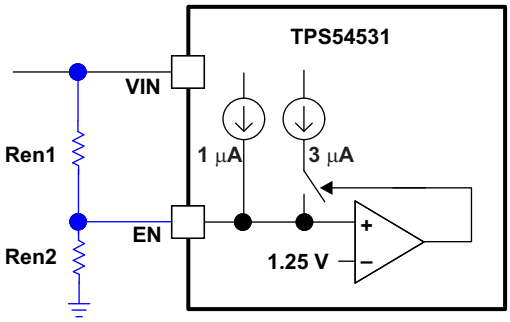


Figure 9. Adjustable Input Undervoltage Lockout

$$Ren1 = \frac{V_{START} - V_{STOP}}{3\ \mu A} \quad (1)$$

$$Ren2 = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{Ren1} + 1\ \mu A} \quad (2)$$

The external start and stop voltages are approximate. Actual start and stop voltages may vary.

PROGRAMMABLE SLOW START USING SS PIN

It is highly recommended to program the slow start time externally because no slow start time is implemented internally. The TPS54531 effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the power supply's reference voltage fed into the error amplifier and will regulate the output accordingly. A capacitor (C_{SS}) on the SS pin to ground implements a slow start time. The TPS54531 has an internal pull-up current source of 2µA that charges the external slow start capacitor. The equation for the slow start time (10% to 90%) is shown in Equation 3 . The V_{ref} is 0.8 V and the I_{SS} current is 2 µA.

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{ref}(V)}{I_{SS}(\mu A)} \quad (3)$$

The slow start time should be set between 1ms to 10 ms to ensure good start-up behavior. The slow start capacitor should be no more than 27nF.

If during normal operation, the input voltage drops below the VIN UVLO threshold, or the EN pin is pulled below 1.25 V, or a thermal shutdown event occurs, the TPS54531 stops switching.

ERROR AMPLIFIER

The TPS54531 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92 µA/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

SLOPE COMPENSATION

In order to prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS54531 adds a built-in slope compensation which is a compensating ramp to the switch current signal.

CURRENT MODE COMPENSATION DESIGN

The device is able to work with various types of output capacitors with appropriate compensation designs. For designs using ceramic output capacitors, proper derating of ceramic output capacitance is recommended when doing the stability analysis. This is because the actual ceramic capacitance drops considerably from the nominal value when the applied voltage increases. Please refer to the *Step by Step Design Procedure* in the Application Information section for the detailed guidelines.

OVERCURRENT PROTECTION AND FREQUENCY SHIFT

The TPS54531 implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle by cycle basis. Every cycle the switch current and the COMP pin voltage are compared; when the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limit the output current.

The TPS54531 provides robust protection during short circuits. There is potential for overcurrent runaway in the output inductor during a short circuit at the output. The TPS54531 solves this issue by increasing the off time during short circuit conditions by lowering the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 0.8 V on VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is shown in Table 1.

Table 1. Switching Frequency Conditions

SWITCHING FREQUENCY	VSENSE PIN VOLTAGE
570 kHz	VSENSE ≥ 0.6 V
570 kHz / 2	0.6 V > VSENSE ≥ 0.4 V
570 kHz / 4	0.4 V > VSENSE ≥ 0.2 V
570 kHz / 8	0.2 V > VSENSE

OVERVOLTAGE TRANSIENT PROTECTION

The TPS54531 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above 109% × V_{ref}, the high-side MOSFET will be forced off. When the VSENSE pin voltage falls below 107% × V_{ref}, the high-side MOSFET will be enabled again.

THERMAL SHUTDOWN

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 165°C, the device reinitiates the power up sequence.

APPLICATION INFORMATION

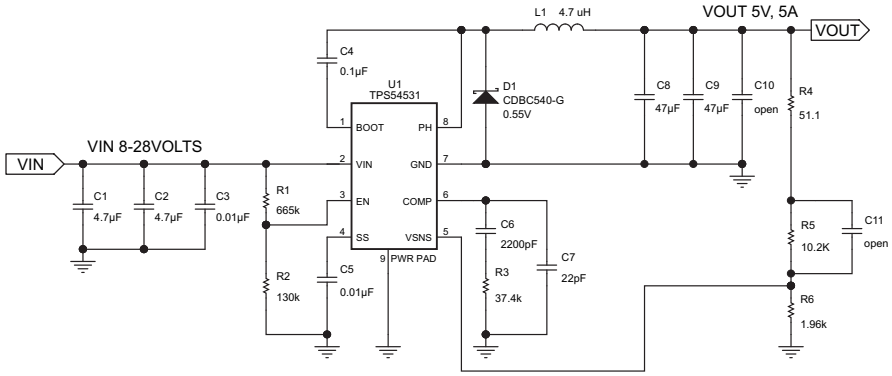


Figure 10. Typical Application Schematic

STEP BY STEP DESIGN PROCEDURE

The following design procedure can be used to select component values for the TPS54531. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

For this design example, use the following as the input parameters

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 V to 28V
Output voltage	5 V
Transient response, 2.5 A load step	ΔVout = +/- 5 %
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	5 A
Operating Frequency	570 kHz

SWITCHING FREQUENCY

The switching frequency for the TPS54531 is fixed at 570 kHz.

OUTPUT VOLTAGE SET POINT

The output voltage of the TPS54531 is externally adjustable using a resistor divider network. In the application circuit of Figure 10, this divider network is comprised of R5 and R6. The relationship of the output voltage to the resistor divider is given by Equation 4 and Equation 5:

$$R6 = \frac{R5 \times V_{REF}}{V_{OUT} - V_{REF}} \quad (4)$$

$$V_{OUT} = V_{REF} \times \left[\frac{R5}{R6} + 1\right] \quad (5)$$

Choose R5 to be approximately 10.0 kΩ. Slightly increasing or decreasing R5 can result in closer output voltage matching when using standard value resistors. In this design, R5 = 10.2 kΩ and R6 = 1.96 kΩ, resulting in a 4.96 V output voltage. The 51.1 ohm resistor R4 is provided as a convenient place to break the control loop for stability testing.

Under Voltage Lockout Set Point

The Under Voltage Lock Out (UVLO) can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between VIN and the EN pin of the TPS54531 and R2 is connected between EN and GND . The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the minimum input voltage is 8 V, so the start voltage threshold is set to 7 V with 2 V hysteresis. Equation 1 and Equation 2 can be used to calculate the values for the upper and lower resistor values of R1 and R2.

INPUT CAPACITORS

The TPS54531 requires an input decoupling capacitor and depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value may be used as long as all other requirements are met; however 10 µF has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be needed, especially if the TPS54531 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design two 4.7 µF capacitors are used for the input decoupling capacitor. They are X7R dielectric rated for 50 V. The equivalent series resistance (ESR) is approximately 2mΩ, and the current rating is 3 A. Additionally, a small 0.01 µF capacitor is included for high frequency filtering.

This input ripple voltage can be approximated by Equation 6

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (6)$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_{BULK} is the bulk capacitor value and ESR_{MAX} is the maximum series resistance of the bulk capacitor.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 7

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (7)$$

In this case, the input ripple voltage would be 243 mV and the RMS ripple current would be 2.5 A. It is also important to note that the actual input voltage ripple will be greatly affected by parasitics associated with the layout and the output impedance of the voltage source. The actual input voltage ripple for this circuit is shown in Design Parameters and is larger than the calculated value. This measured value is still below the specified input limit of 300 mV. The maximum voltage across the input capacitors would be VIN max plus ΔVIN/2. The chosen bulk and bypass capacitors are each rated for 50 V and the ripple current capacity is greater than 3 A, both providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

OUTPUT FILTER COMPONENTS

Two components need to be selected for the output filter, L_{OUT} and C_{OUT}. Since the TPS54531 is an externally compensated device, a wide range of filter component types and values can be supported.

Inductor Selection

To calculate the minimum value of the output inductor, use Equation 8

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times F_{SW}} \quad (8)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, this value is at the discretion of the designer; however, the following guidelines may be used. For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3 and the minimum inductor value is calculated to be 4.8 µH. For this design, a close standard value was chosen: 4.7 µH.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 9

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right)^2} \quad (9)$$

and the peak inductor current can be determined with Equation 10

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (10)$$

For this design, the RMS inductor current is 5.03 A and the peak inductor current is 5.96 A. The chosen inductor is a Wurth 4.7 µH. It has a saturation current rating of 19.0 A and an RMS current rating of 7.0 A, meeting these requirements. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wishes to allow so long as the other design requirements are met. Larger value inductors will have lower ac current and result in lower output voltage ripple, while smaller inductor values will increase ac current and output voltage ripple. In general, inductor values for use with the TPS54531 are in the range of 1 µH to 47µH.

Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Equation 11 shows the minimum output capacitance necessary to accomplish this.

$$Co > \frac{2 \cdot \Delta Iout}{fsw \cdot \Delta Vout} \quad (11)$$

Where ΔIout is the change in output current, Fsw is the regulators switching frequency and ΔVout is the allowable change in the output voltage. For this example, the transient load response is specified as a 5% change in Vout for a load step of 2.5 A. For this example, ΔIout = 2.5 A and ΔVout = 0.05 x 5.0 = 0.250 V. Using these numbers gives a minimum capacitance of 35 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 12 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Voripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. Under this requirement Equation 12, yields 14 µF.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{Voripple}{Iripple}} \tag{12}$$

Equation 13 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 13 indicates the ESR should be less than 15.6 mΩ. In this case, the ceramic caps' ESR is much smaller than 15.6 mΩ.

$$Resr < \frac{Voripple}{Iripple} \tag{13}$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, two 47 µF 10V X5R ceramic capacitor with 3 mΩ of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation 14 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 14 yields 554 mA.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C} \right) \tag{14}$$

COMPENSATION COMPONENTS

There are several possible methods to design closed loop compensation for dc/dc converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at -20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and starts to fall one decade below the modulator pole frequency reaching a minimum of -90 degrees one decade above the modulator pole frequency. The modulator pole is a simple pole shown in Equation 15

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \tag{15}$$

For the TPS54531 most circuits will have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics will deviate from the ideal approximations. The phase loss of the power stage will now approach -180 degrees, making compensation more difficult. The power stage transfer function can be solved but it is a tedious hand calculation that does not lend itself to simple approximations. It is best to use Pspice to accurately model the power stage gain and phase so that a reliable compensation circuit can be designed. Alternately, a direct measurement of the power stage characteristics can be used. That is the technique used in this design procedure. For this design, L1 = 4.7 µH. C8 and C9 are set to 47µF each, and the ESR is 3 mΩ. Now the power stage characteristics are shown in Figure 11.

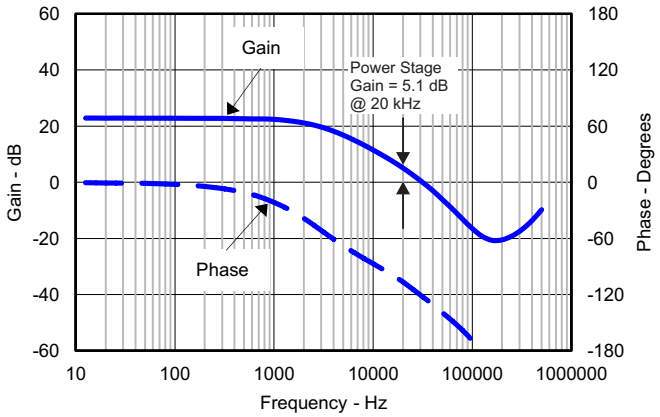


Figure 11. Power Stage Gain and Phase Characteristics

For this design, the intended crossover frequency is 20 kHz. From the power stage gain and phase plots, the gain at 20 kHz is 5.1 dB and the phase is about -100 degrees. For 60 degrees of phase margin, additional phase boost from a feed forward capacitor in parallel with the upper resistor of the voltage set point divider is not needed. R3 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. The required value of R3 can be calculated from Equation 16.

$$R3 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{EA}} \cdot \frac{V_{REF}}{V_{OUT}} \tag{16}$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 20 kHz. The required value for C6 is given by Equation 17.

$$C6 = \frac{1}{2 \cdot \pi \cdot R3 \cdot \frac{F_{CO}}{10}} \tag{17}$$

To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 20 kHz. The pole can also be useful to offset the ESR of aluminum electrolytic output capacitors. The value for C7 can be calculated from Equation 18.

$$C7 = \frac{1}{2 \cdot \pi \cdot R3 \cdot 10 \cdot F_{CO}} \tag{18}$$

For this design the calculated values for the compensation components are R3 = 37.4 kΩ ,C6 = 2200 pF and C7 = 22 pF.

BOOTSTRAP CAPACITOR

Every TPS54531 design requires a bootstrap capacitor, C4. The bootstrap capacitor must be 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT pin. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

CATCH DIODE

The TPS54531 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is VINMAX + 0.5 V. Peak current must be greater than IOUTMAX plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a CDBC540-G is chosen, with a reverse voltage of 40 V, forward current of 5 A, and a forward voltage drop of 0.55 V.

SLOW START CAPACITOR

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54531 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft start capacitor value can be calculated using Equation 3. For the example circuit, the soft start time is not too critical since the output capacitor value is 2 x 47 µF which does not require much current to charge to 5 V. The example circuit has the soft start time set to an arbitrary value of 4 ms which requires a 10 nF capacitor. In TPS54531, Iss is 2 µA and Vref is 0.8V.

OUTPUT VOLTAGE LIMITATIONS

Due to the internal design of the TPS54531, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 91% and is given by Equation 19:

$$V_{Omax} = 0.91 \times \left(\left(V_{IN\ min} - I_{O\ max} \times R_{DS(on)\ max}\right) + V_D\right) - \left(I_{O\ max} \times R_L\right) - V_D \quad (19)$$

Where:

$V_{IN\ min}$ = Minimum input voltage
$I_{O\ max}$ = Maximum load current
V_D = Catch diode forward voltage
R_L = Output inductor series resistance

The equation assumes maximum on resistance for the internal high-side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 130 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by Equation 20:

$$V_{Omin} = 0.089 \times \left(\left(V_{IN\ max} - I_{O\ min} \times R_{DS(on)\ min}\right) + V_D\right) - \left(I_{O\ min} \times R_L\right) - V_D \quad (20)$$

Where:

$V_{IN\ max}$ = Maximum input voltage
$I_{O\ min}$ = Minimum load current
V_D = Catch diode forward voltage
R_L = Output inductor series resistance

This equation assumes nominal on-resistance for the high-side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to assure proper functionality.

POWER DISSIPATION ESTIMATE

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working in the discontinuous conduction mode (DCM) or pulse skipping Eco-mode™.

The device power dissipation includes:

1) Conduction loss: $P_{con} = I_{out}^2 \times R_{DS(on)} \times V_{OUT}/V_{IN}$

2) Switching loss: $P_{sw} = 0.5 \times 10^{-9} \times V_{IN}^2 \times I_{OUT} \times F_{sw}$

3) Gate charge loss: $P_{gc} = 22.8 \times 10^{-9} \times F_{sw}$

4) Quiescent current loss: $P_q = 0.11 \times 10^{-3} \times V_{IN}$

Where:

I_{OUT} is the output current (A).

$R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω).

VOUT is the output voltage (V).

VIN is the input voltage (V).

Fsw is the switching frequency (Hz).

So

Ptot = Pcon + Psw + Pgc + Pq

For given T_A , $T_J = T_A$ + Rth x Ptot.

For given T_{JMAX} = 150°C, $T_{AMAX} = T_{JMAX}$– Rth x Ptot.

Where:

Ptot is the total device power dissipation (W).

T_A is the ambient temperature (°C).

T_J is the junction temperature (°C) .

Rth is the thermal resistance of the package (°C/W).

T_{JMAX} is maximum junction temperature (°C).

T_{AMAX} is maximum ambient temperature (°C).

PCB LAYOUT

The VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The typical recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the source of the anode of the catch diode. See Figure 12 for a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the IC. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Since the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the exposed thermal pad should be soldered directly to the top side ground area under the IC. Use thermal vias to connect the top side ground area to an internal or bottom layer ground plane. The total copper area must provide adequate heat dissipation. Additional vias adjacent to the device can b used to improve heat transfer to the infernal or bottom layer ground plane . The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate layout schemes, however this layout has been shown to produce good results and is intended as a guideline.

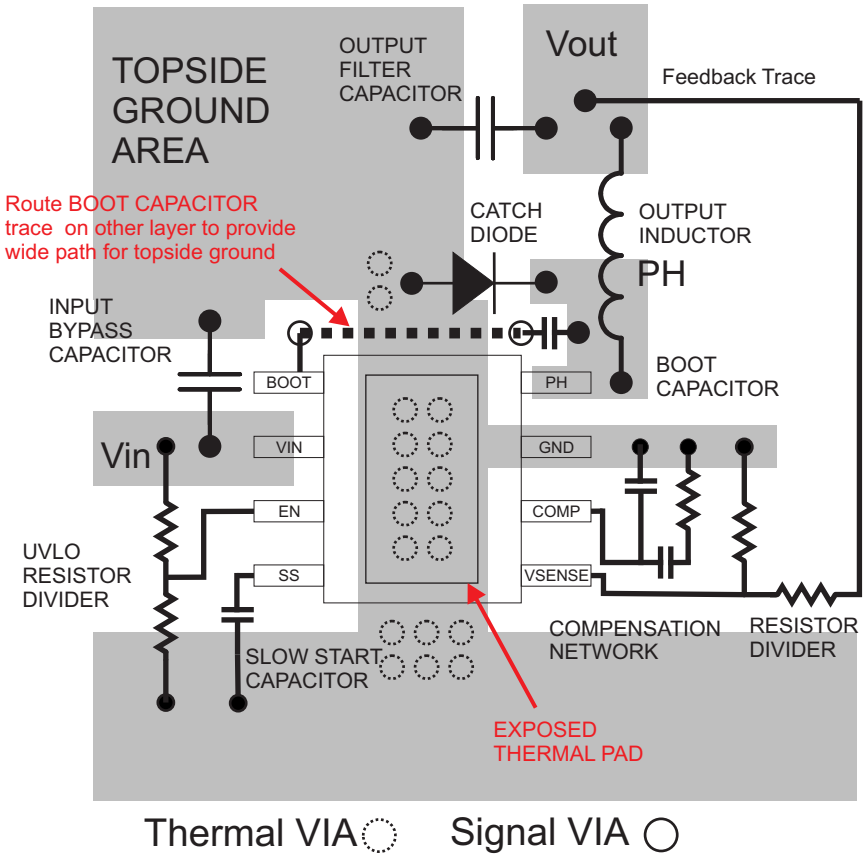


Figure 12. TPS54531DDA Board Layout

ELECTROMAGNETIC INTERFERENCE (EMI) CONSIDERATIONS

As EMI becomes a rising concern in more and more applications, the internal design of the TPS54531 takes measures to reduce the EMI. The high-side MOSFET gate drive is designed to reduce the PH pin voltage ringing. The internal IC rails are isolated to decrease the noise sensitivity. A package bond wire scheme is used to lower the parasitics effects.

To achieve the best EMI performance, external component selection and board layout are equally important. Follow the *Step by Step Design Procedure* above to prevent potential EMI issues.

APPLICATION CURVES

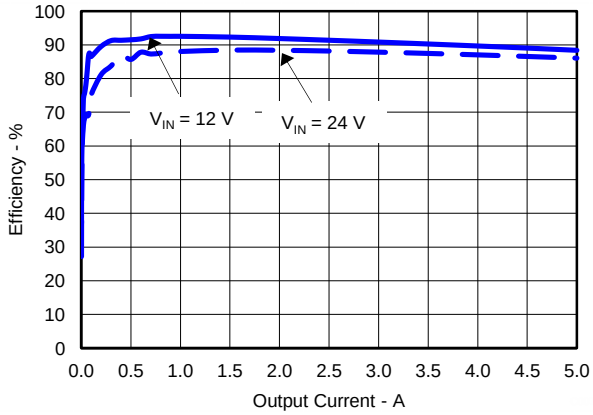


Figure 13. TPS54531D Efficiency

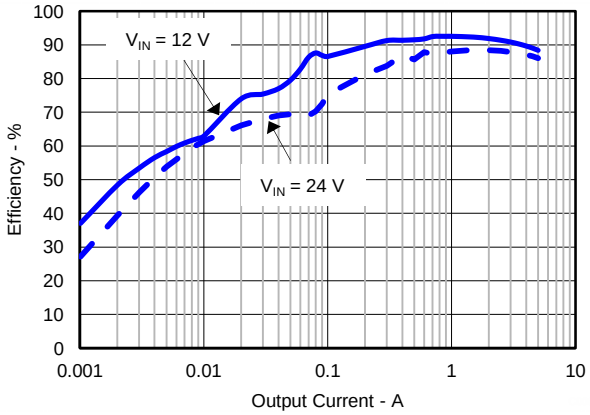


Figure 14. TPS54531D Low Current Efficiency

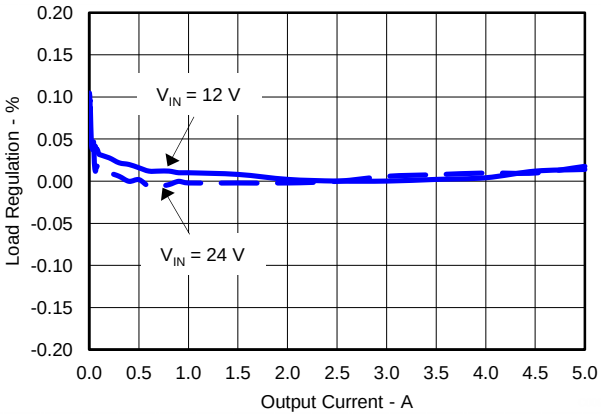


Figure 15. TPS54531D Load Regulation

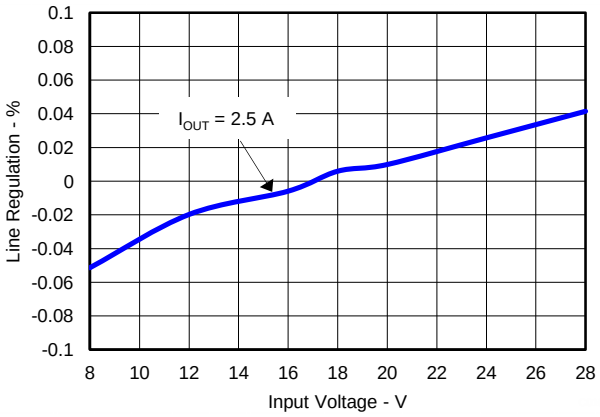


Figure 16. TPS54531D Line Regulation

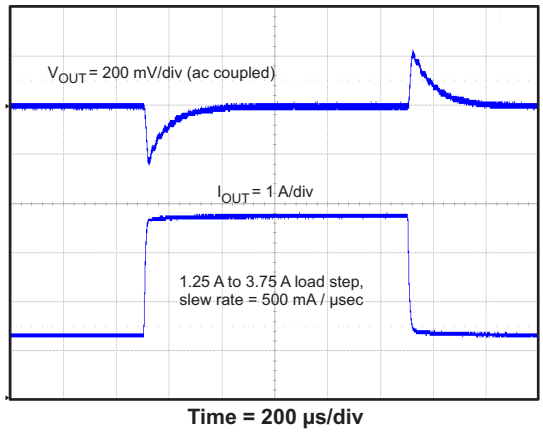


Figure 17. TPS54531 Transient Response

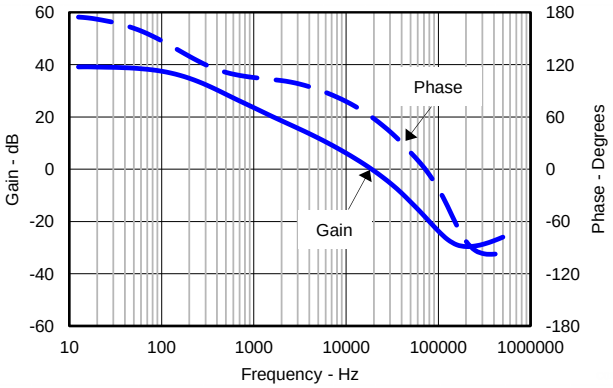


Figure 18. TPS54531 Loop Response

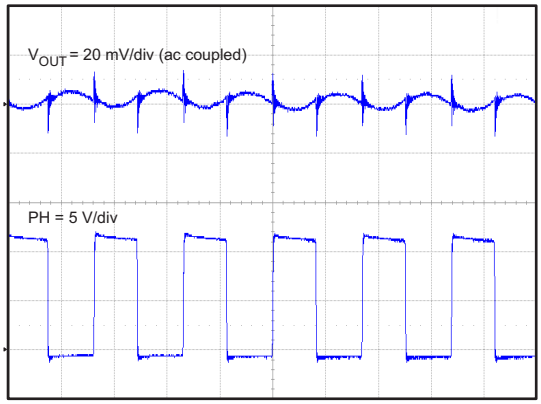


Figure 19. TPS54531 Full Load Output Ripple

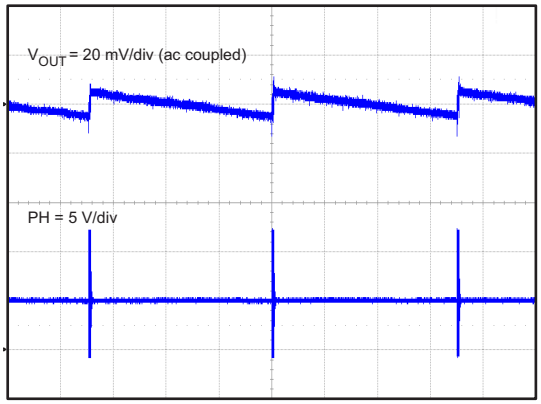


Figure 20. TPS54531 Eco-mode™Output Ripple

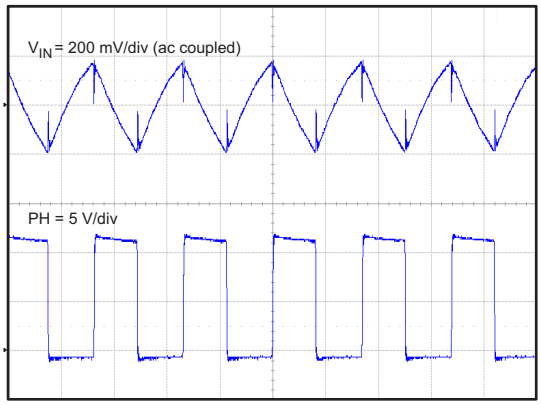


Figure 21. TPS54531 Full Load Input Ripple

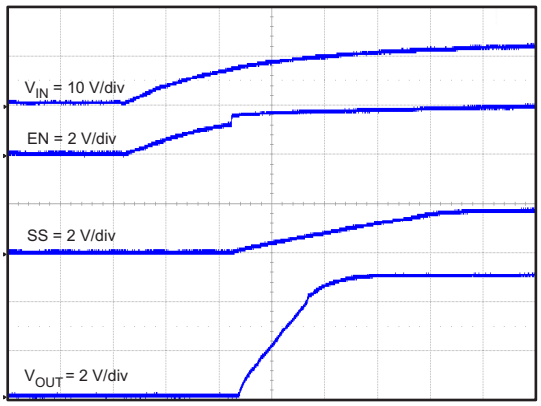


Figure 22. TPS54531 Start Up Relative to VIN

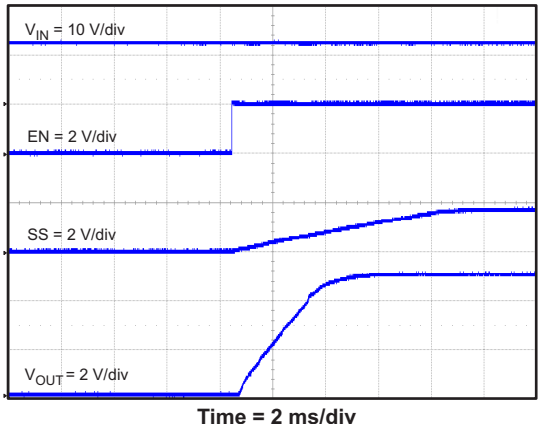


Figure 23. TPS54531 Start-up Relative to Enable

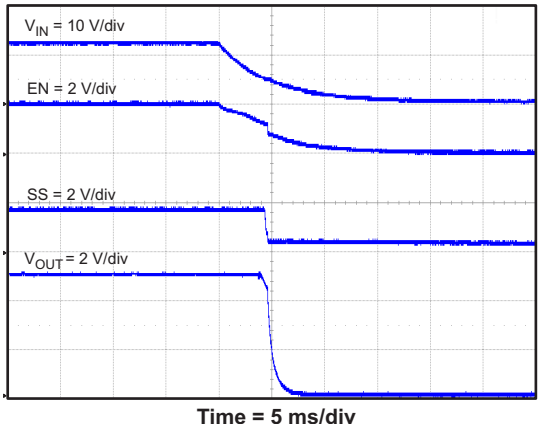


Figure 24. TPS54531 Shut Down Relative to VIN

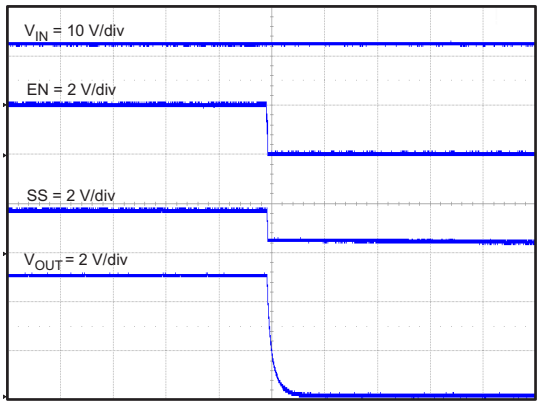


Figure 25. TPS54531 Shut Down Relative to EN

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54531DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54531	Samples
TPS54531DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	54531	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

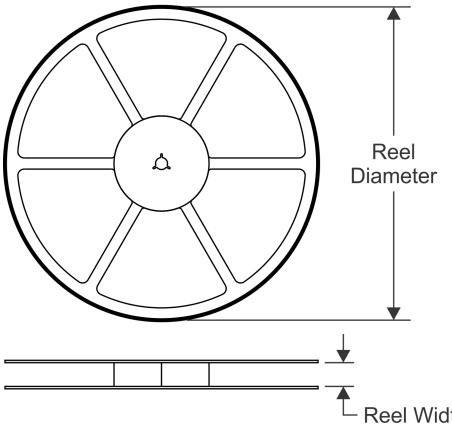
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

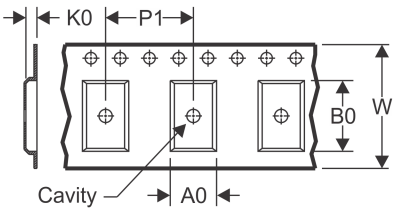
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

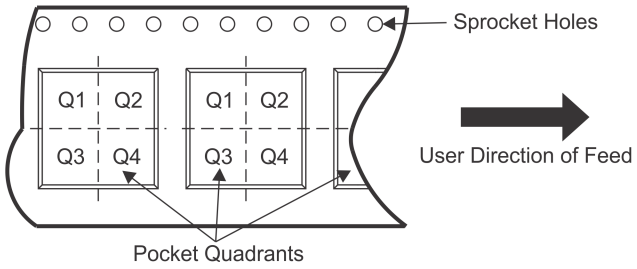


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

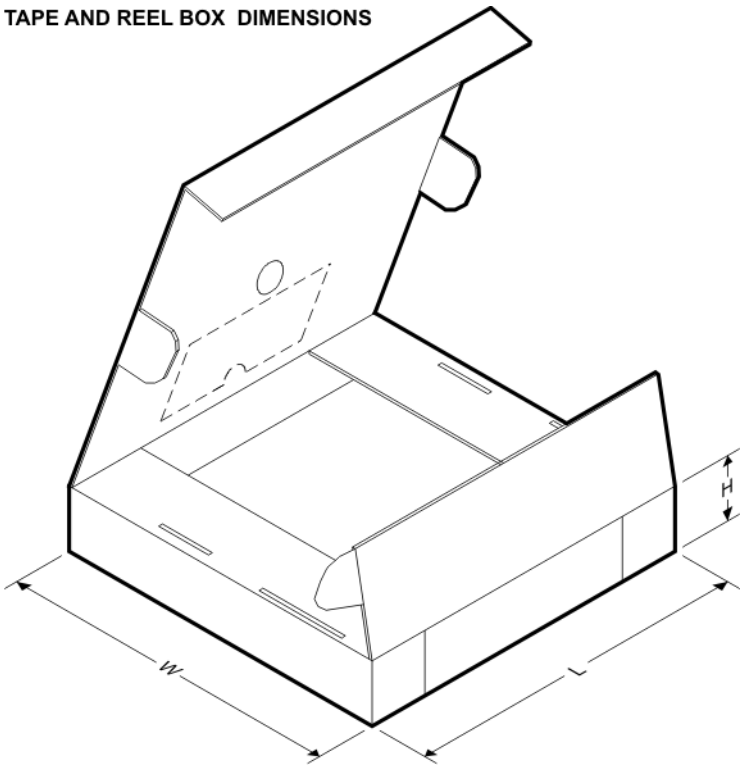
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54531DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

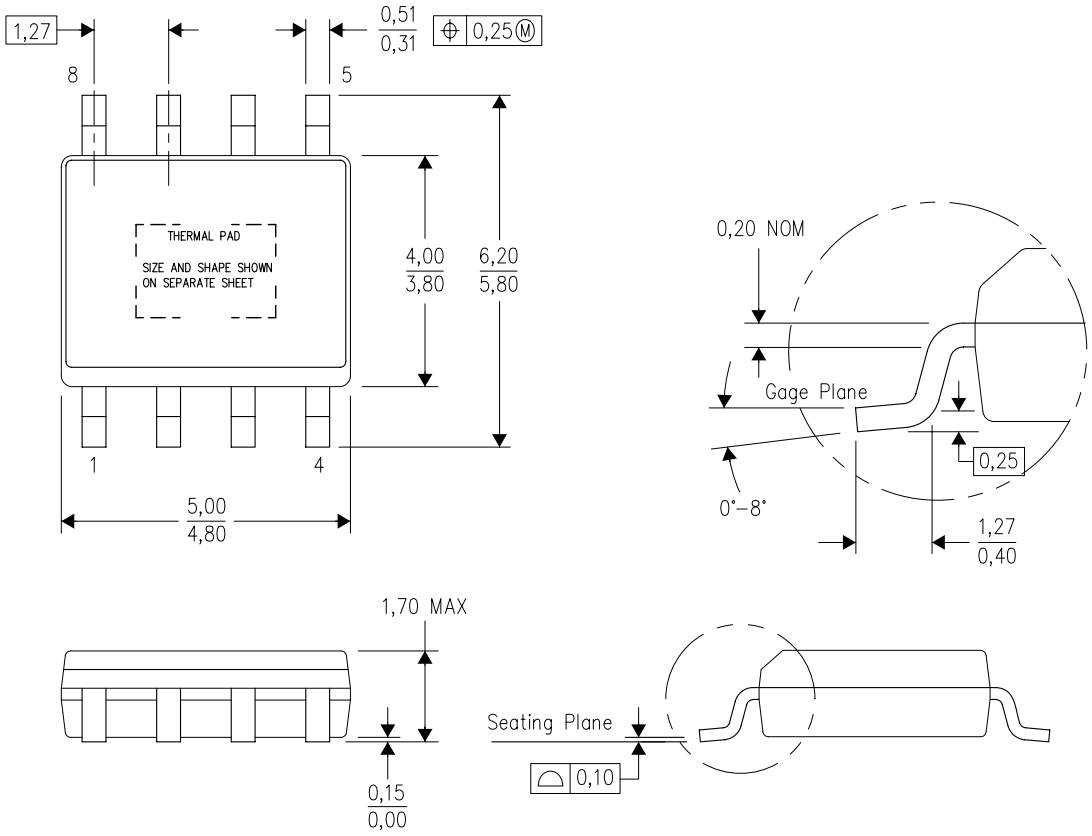
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54531DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

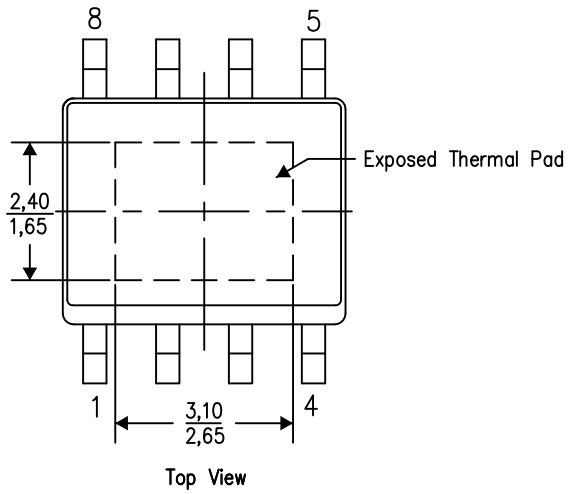
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



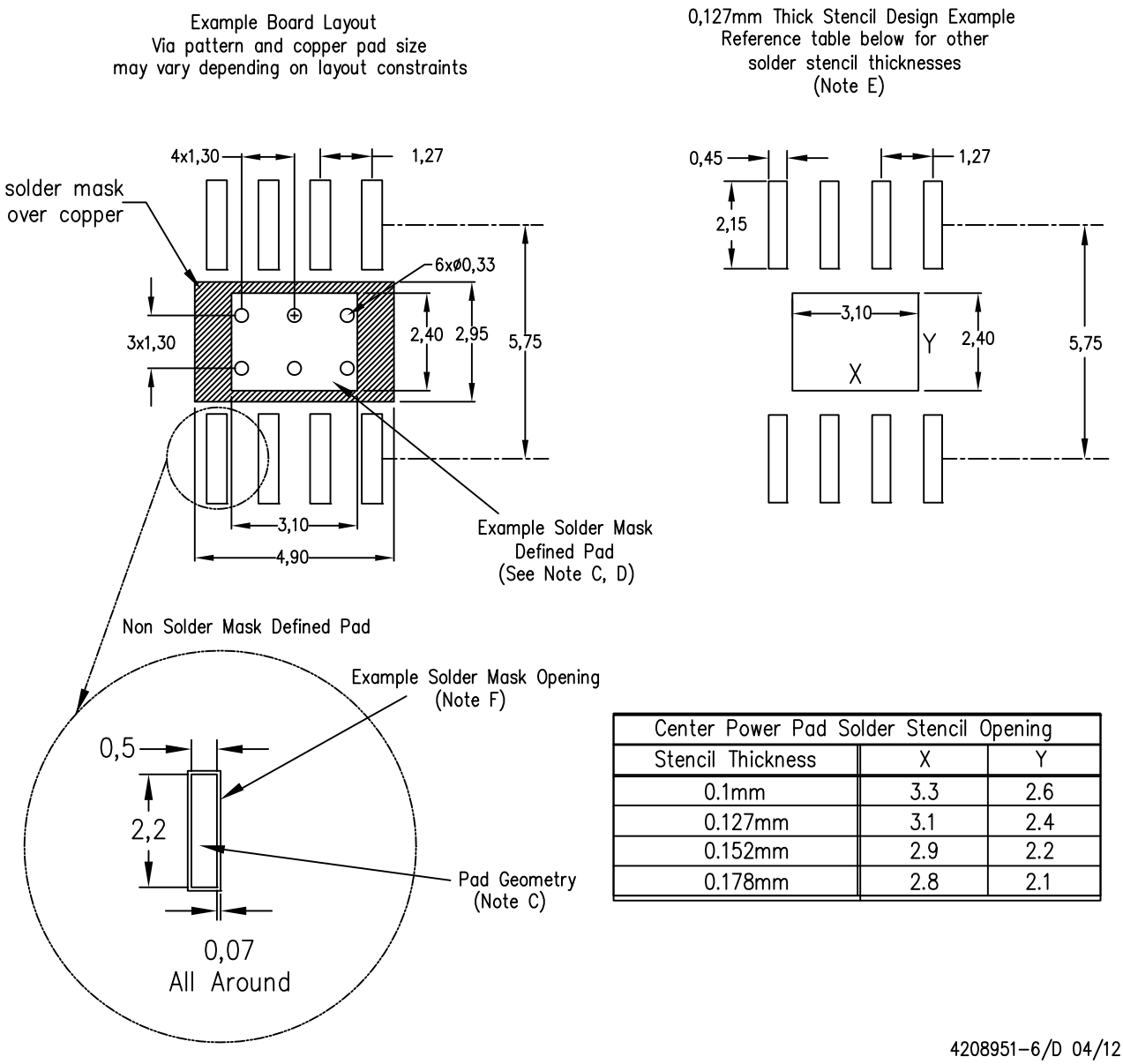
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265