TPS63802 2-A, High-Efficient, Low I_Q Buck-Boost Converter with Small Solution Size

1 Features

- Input Voltage Range: 1.3 V to 5.5 V
  - >1.8 V for Device Start-up
- Output Voltage Range: 1.8 V to 5 V (adjustable)
- 2-A Output Current for V_{IN} ≥ 2.3 V, V_{OUT} = 3.3 V
- High Efficiency Over the Entire Load Range
  - 11-µA Operating Quiescent Current
  - Power Save Mode with Mode Selection
- Peak Current Buck-Boost Mode Architecture
  - Seamless Transition Between Buck, Buck-Boost and Boost operation modes
  - Operates With Low and High Output Capacitance values
  - Forward and Reverse Current Operation
  - Start-up Into Pre-Biased Outputs
- Safety- and Robust Operation Features
  - Integrated Soft Start
  - Over-Temperature- and Over-Voltage-Protection
  - True Shutdown Function with Load Disconnect
  - Forward and Backward current limit
- Small Solution Size
  - 2 mm x 3 mm Package size
  - Small 1 µH inductor
  - Works With 22 µF Minimum Output Capacitor

2 Applications

- System Pre-Regulator (Smartphone, Tablet, EFT Terminal, Telematics)
- Point-of-Load Regulation (Wired Sensor, Port/Cable Adapter and Dongle)
- Fingerprint, Face-ID, Camera Sensors (Smartphone, Electronic Smart Lock, IP Network Camera)
- RF Amplifier Supply (Smart Sensors)
- Thermoelectric Device (TEC/TEM) Supply (Datacom, Optical Modules, Cooling/Heating)

3 Description

The TPS63802 is a high efficiency, high output current buck-boost converter. It is used when the input voltage is higher, equal, or lower than the output voltage. Output currents up to 2 A are supported over a wide voltage range. The device limits the peak current at 4.5 A in Boost-Mode and 3.5 A in Buck-Mode. The device is adjusted to the programmed output voltage. It automatically changes from buck to boost operation based on the input voltage. It remains in a 3-cycle buck-boost mode when the input voltage is approximately equal to the output voltage. The transitions happen seamlessly and avoids unwanted toggling within the modes. The TPS63802 comes in a 2 mm x 3 mm package. The device works with tiny passive components to keep the overall solution size small.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS63802	HotRod QFN, 10-Pin (0.5mm pitch)	3.0 mm × 2.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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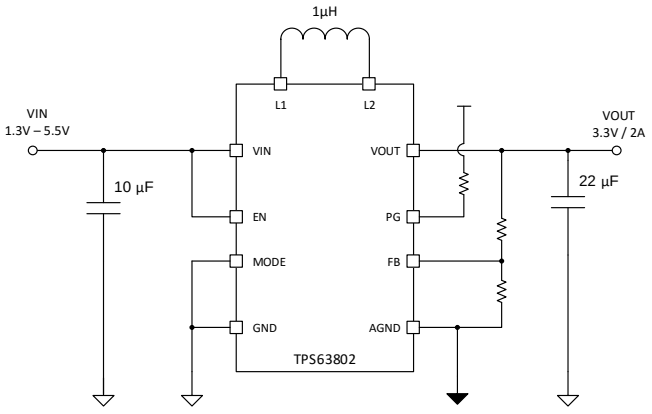
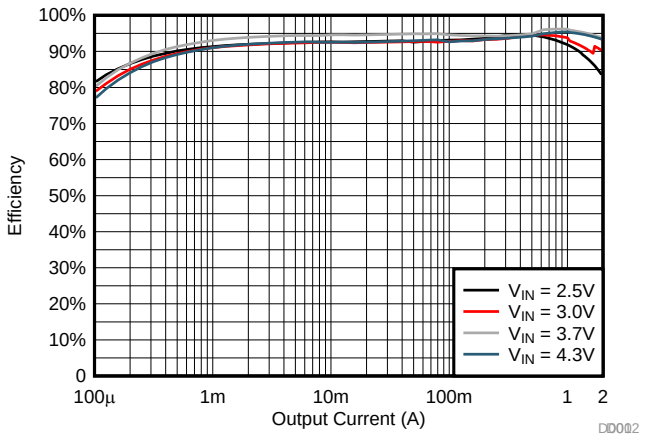
Typical Application



Efficiency vs Output Current (V_O = 3.3V)



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4 Revision History

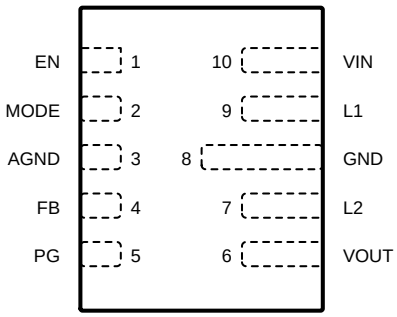
DATE	REVISION	NOTES
November 2018	*	Initial release

5 Device Comparison Table

PART NUMBER	VOUT
TPS63802	Adjustable

6 Pin Configuration and Functions

Top View



Not to scale

Pin Functions

PIN		DESCRIPTION
NO	NAME	
10	VIN	Supply voltage input
9	L1	Connection for inductor
1	EN	Device Enable input. Set HIGH to enable and LOW to disable. It must not be left floating
8	GND	Power ground
2	MODE	PFM/PWM mode selection. Set LOW for power safe mode, set HIGH for forced PWM mode. It must not be left floating
3	AGND	Analog ground
7	L2	Connection for inductor
6	VOUT	Power stage output
4	FB	Voltage feedback sensing Pin
5	PG	Power good indicator, open drain output

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7 Specifications

7.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, L1, L2, EN, PFM/PWM, VOUT, FB	–0.3	6	V
	L1, L2 (AC, less than 10ns)	–3	9	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.3		5.5	V
V_{OUT}	Output voltage	1.8		5 (1)	V
C_{IN}	Effective capacitance connected to V_{IN}	4	5		µF
L	Effective inductance	0.7	1	1.2	µH
C_{OUT}	Effective capacitance connected to V_{OUT}	6	10		µF
T_J	Operating junction temperature	–40		125	°C

(1) Vo margin for accuracy and load steps is considerd in absolut maximum ratings

7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPS63802 HotRod QFN 10 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	81.0	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	36.4	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.5	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

V_{IN}= 1.8 V to 5.5 V, V_{OUT} = 1.8 V to 5 V , T_J= –40°C to +125°C, typical values are at T_J= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$V_{IN;LOAD}$	Minimum input voltage for full load, once started	I_{OUT} = 2 A, VOUT = 3.3 V, T_J = 25°C		2.3		V
$I_{Q;VIN}$	Quiescent current into VIN	T_J = 25°C, EN = V_{IN} = 3.6 V, V_{OUT} = 3.3 V, not switching		11		µA
I_{SD}	Shutdown current into VIN	EN = low, -40°C ≤ T_J ≤ 85°C, V_{IN} = 3.6 V, V_{OUT} = 0 V		10	600	nA
UVLO	Undervoltage lockout threshold	V_{IN} falling, VOUT ≥ 1.8 V, once started	1.2	1.25	1.29	V
	Undervoltage lockout threshold	V_{IN} rising	1.6	1.7	1.79	V
T_{SD}	Thermal shutdown	Temperature rising		150		°C
$T_{SD;HYST}$	Thermal shutdown hysteresis			20		°C
SOFT-START, POWER GOOD						
Tramp	Soft-start, Current limit ramp time	T_J = 25°C, VIN = 3.6 V, VOUT = 3.3 V, I_O = 3.5A, from 0A to 3.5A		0.28		ms
T_{delay}	Delay from EN-edge until rising V_{OUT}	T_J = 25°C, VIN = 3.6 V		100		µs
LOGIC SIGNALS EN, MODE						
$V_{THR;EN}$	Threshold Voltage rising for EN-Pin		1.07	1.1	1.13	V
$V_{THF;EN}$	Threshold Voltage falling for EN-Pin		0.97	1	1.03	V
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
$V_{PG;rising}$	Power Good threshold voltage	VOUT rising, referenced to VOUT nominal		95%		
$V_{PG;falling}$		VOUT falling, referenced to VOUT nominal		90%		
$V_{PG;Low}$	Power Good low-level output voltage	I_{SINK} = 1 mA			0.4	V
$t_{PG;delay}$	Power Good delay time	V_{FB} falling		40		µS
I_{lkg}	Input leakage current			0.01	0.2	µA
OUTPUT						
I_{SD}	Shutdown current into VOUT	EN = low, -40°C ≤ T_J ≤ 85°C, V_{IN} = 0.0 V, V_{OUT} = 3.3 V		10	600	nA
V_{FB}	Feedback Regulation Voltage			500		mV
V_{FB}	Feedback Voltage accuracy	PWM mode	–1%		1%	
	Overvoltage Protection Threshold	V_{OUT} rising	5.5	5.66	5.78	V
		V_{IN} rising	5.5	5.66	5.78	V
$I_{PWM/PFM}$	Peak Inductor Current to enter PFM-Mode	V_{IN} = 3.6 V; V_{OUT} = 3.3 V	550	700	900	mA
I_{FB}	Feedback Input Bias Current	V_{FB} = 500 mV		10	100	nA
I_{PK}	Peak Current Limit, Boost Mode	V_{IN} ≥ 2.5V	3.5	4.8	5.8	A
	Peak Current Limit, Buck-Boost Mode			4.8		A
	Peak Current Limit, Buck Mode			3.5		A
$I_{PK;Reverse}$	Peak Current Limit for Reverse Operation	V_{IN} = 3.6 V, V_{OUT} = 3.3 V		–0.75	–0.5	A
Buck $R_{DS;ON}$	High-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V		47		mΩ
	Low-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V		30		mΩ
Boost $R_{DS;ON}$	High-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V		43		mΩ
	Low-side FET on-resistance	V_{IN} = 3 V, V_{OUT} = 3.3 V		18		mΩ

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Electrical Characteristics (continued)

V_{IN}= 1.8 V to 5.5 V, V_{OUT} = 1.8 V to 5 V , T_J= –40°C to +125°C, typical values are at T_J= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Inductor Switching Frequency, Boost Mode	V_{IN} = 2.3V, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C		2.1		MHz
	Inductor Switching Frequency, Buck-Boost Mode	V_{IN} = 3.3V, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C		1.4		MHz
	Inductor Switching Frequency, Buck Mode	V_{IN} = 4.3, V_{OUT} = 3.3V, no Load, MODE = HIGH, T_J = 25°C		2.7		MHz
	Line regulation	V_{IN} = 2.4 V to 5.5 V, V_{OUT} = 3.3V, I_{OUT} = 2 A		0.05		%
	Load regulation	V_{IN}= 3.6 V, V_{OUT} = 3.3V, I_{OUT} = 0 A to 2 A, PWM Mode		0.1		%

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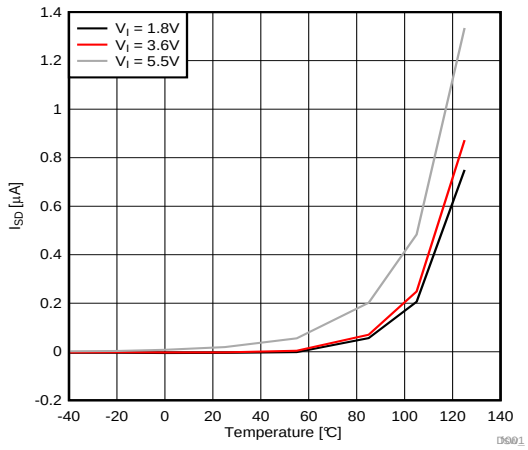
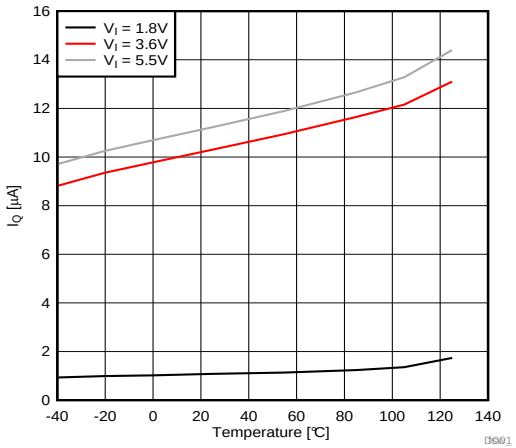
7.6 Typical Characteristics



EN = LOW

Figure 1. Shutdown Current vs. Temperature



MODE = LOW V_O = 3.3V, 0mA load, not switching

Figure 2. Quiescent Current vs Temperature

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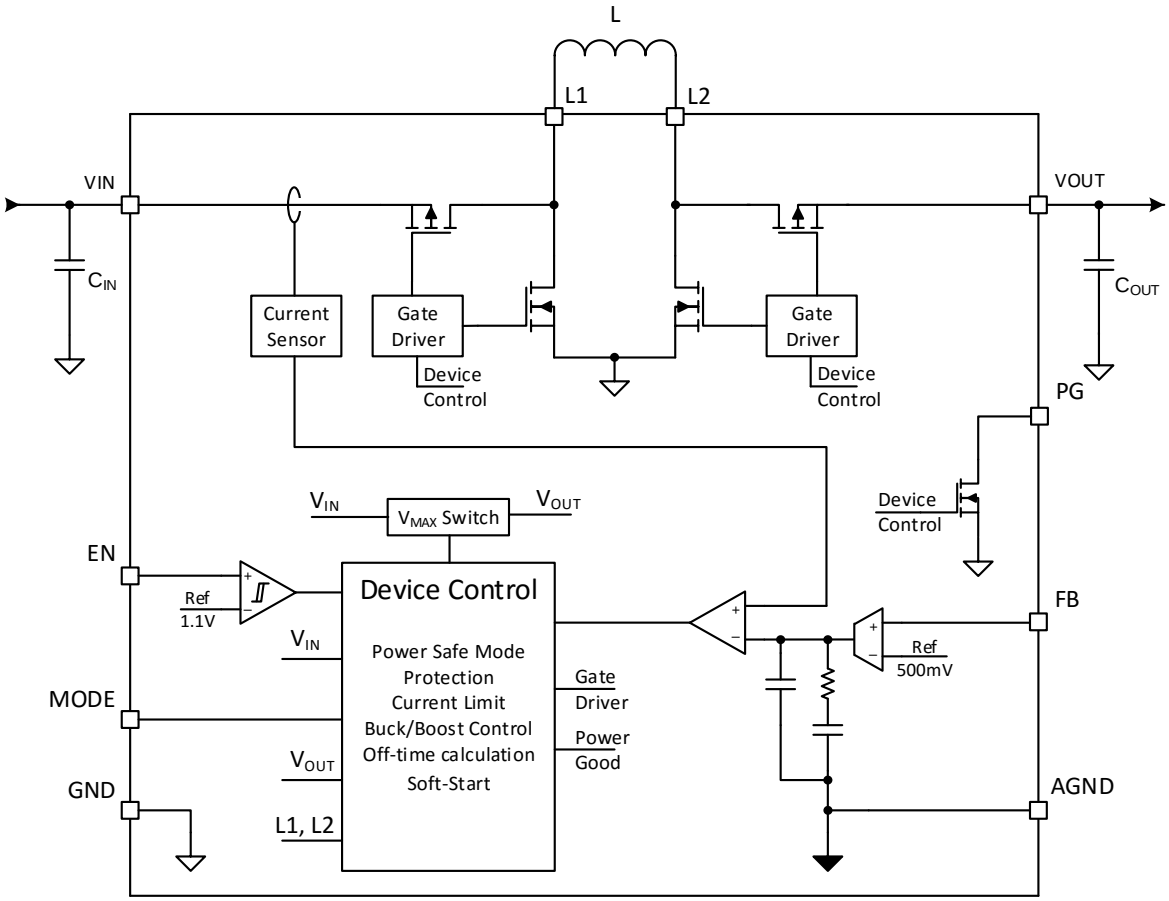
8 Detailed Description

8.1 Overview

The TPS63802 Buck-Boost converter uses 4 internal switches to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output load range. To regulate the output voltage at all possible input voltage conditions, the device automatically transits between buck, buck-boost and boost operation as required by the configuration. In buck and boost modes, it always uses one active switch, one rectifying switch, one switch on, and one switch held off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. When the input voltage is close to the output voltage, it operates in a 3-cycle buck-boost operation. In this mode all 4 switches are active (seeBuck-Boost Operation) The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep high efficiency over the complete input voltage range. The device provides a seamless transition between all modes.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Control Loop Description

TPS63802 uses a peak current mode control architecture. It has an inner current loop where it measures the peak current of the boost High-Side MOSFET and compares it to a reference current. This current is the output of the outer voltage loop. It measures the output voltage via the FB-Pin and compares it with the internal voltage reference. That means, the outer voltage loop measures the voltage error (V_{REF}-V_{FB}) and transforms it into the system current demand (I_{REF}) for the inner Current Loop.

Figure 3 shows the simplified schematic of the control loop. The Error Amplifier and its Type-2 compensation represent the voltage loop. Its voltage output is converted into ther reference current IREF and fed into the current comparator.

The Scheme shows as well the Skip-Comparator handling the Power Safe Mode (PFM) to achieve high Efficiency at light loads. See Power Save Mode Operation for further details.

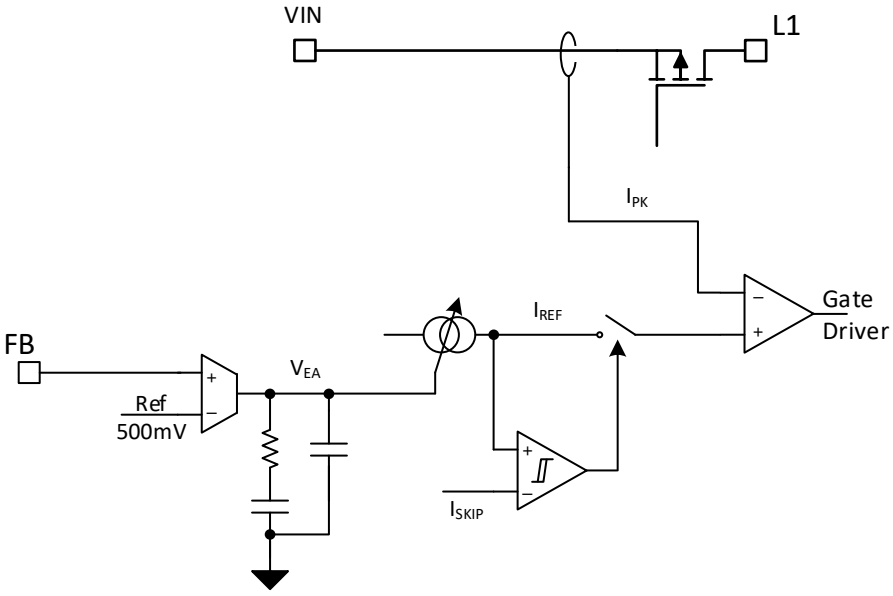


Figure 3. Control Loop Architecture Scheme

8.3.2 Precise Device Enable: Threshold- or delayed Enable

The Enable-Pin is a digital input to enable or disable the device by applying a high- or low-level. The device enters shutdown when EN is set low. In addition, this input features a precise threshold and can be used as a comparator that enables/disables the part at a defined threshold. This allows to drive the state by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. The enable pin can also be used with an external voltage divider to set a user-defined minimum supply voltage. For proper operation, the EN pin must be terminated and must not be left floating.

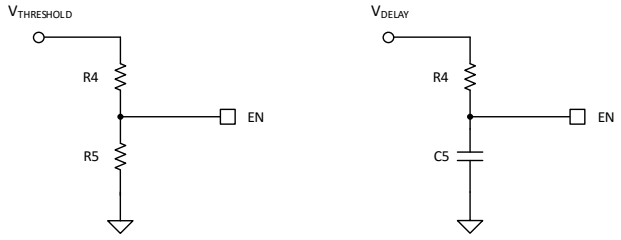


Figure 4. Circuit Example how to use the Precise Device Enable feature

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Feature Description (continued)

8.3.3 Mode Selection (PFM/PWM)

The Mode-Pin is a digital input to enable the automatic PWM/PFM Mode that features highest efficiency by allowing Pulse-Frequency-Modulation for lower output currents. This mode is enabled by applying a low level. The device can be forced in PWM operation regardless of the output current to achieve minimum output ripple by applying a high level. This pin must not be left floating

8.3.4 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. It activates the device once the input voltage (V_I) has risen the $UVLO_{rising}$ value. Once active, the device allows operation down to even smaller input voltages which is determined by the $UVLO_{falling}$. This behavior requires V_O to be higher than the minimum value of 1.8V.

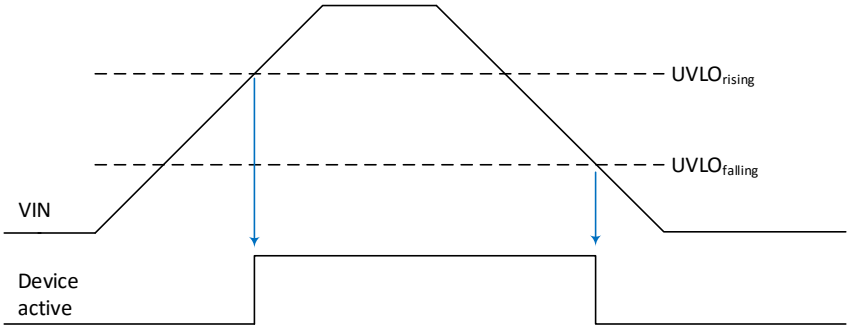

Figure 5. Rising and falling Undervoltage Lockout behavior

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Feature Description (continued)

8.3.5 Softstart

To minimize inrush current and output voltage overshoot during start-up, the device features a controlled soft start-up. After device enable, the device starts all internal reference and control circuits within the enable delay time T_{delay}. After that, the maximum switch current limit raises monotonic from zero mA to the current limit. The loop stops switching once V_O is reached. This allows a quick output voltage raise for small capacitors at the output. The bigger the output capacitor, the longer it takes to settle Vout. A potential load during start is lengthening the ramp as well. The raise of the current limit allows smallest inrush current for no-load conditions, as well as the possibility to start into high loads at start-up.

The converter can start-up into pre-biased loads, by a forced operation in PFM during the soft-start until the first switching cycle request from the output voltage control loop.

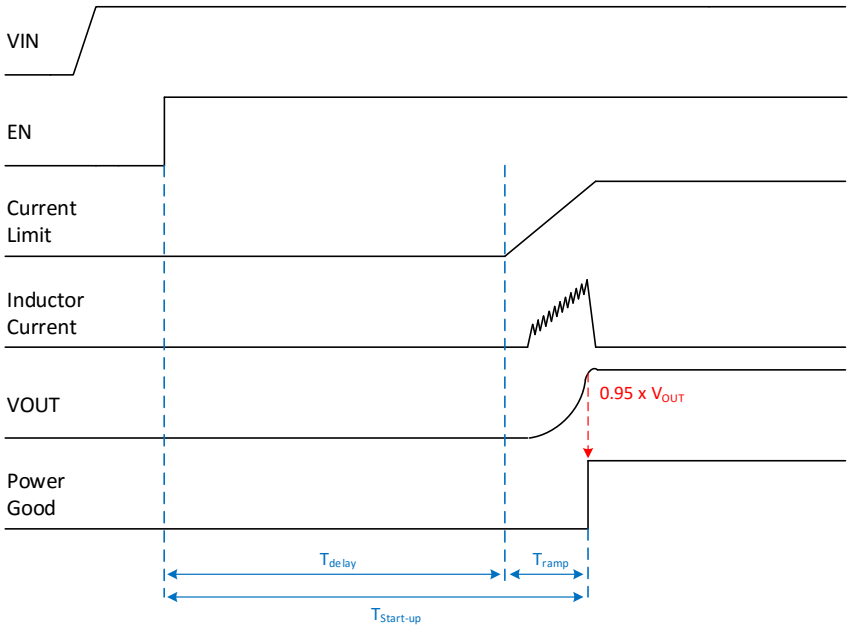

Figure 6. Device Start-up Scheme

8.3.6 Adjustable Output Voltage

The devices output voltage is adjusted by applying an external resistive divider between V_O, FB-Terminal and GND. This allows to program the output voltage in the recommended range. The divider should provide a low-side resistor of less than 100 KΩ. The high-side resistor is chosen accordingly.

8.3.7 Over Temperature Protection - Thermal Shutdown

The device has a built-in temperature sensor which monitors the IC temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the over-temperature threshold.

8.3.8 Input Overvoltage - Reverse-Boost Protection (IVP)

TPS63802 can operate in reverse mode where the device transfers energy from the output back to the input. If the source would not be able to sink that current, potentially charge can build up uncontrolled and V_{IN} rises. To protect the device and other components from that scenario, the device features an Input Voltage Protection (IVP) for reverse Boost Operation. Once the input voltage is above the threshold, the converter forces PFM mode and the negative current operation is interrupted.

The PG signal goes low to indicate that behavior.

ADVANCE INFORMATION

Feature Description (continued)

8.3.9 Output Overvoltage Protection (OVP)

In case of a broken feedback-path connection the device can loose V_O information and is not able to regulate. To avoid a uncontrolled boosting of V_O, TPS63802 features an Output Overvoltage Protection. It measures the voltage on VOUT-Pin and stops switching when V_O is greater than the threshold avoid harm of the converter and of other components.

8.3.10 Power Good Indicator

The power good goes high-impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. This feature also indicates Overvoltage and device shutdown cases as shown in the table The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

Table 1. Power Good Indicator Truth Table

Logic Signals					PG LOGIC STATUS
EN	VOUT	VIN	OVP	IVP	
X	< 1.8V	< UVLO_R	X	X	undefined
LOW	X	> UVLO_F	X	X	LOW
HIGH	VOUT < 0.9 * target-VOUT	> 1.3V	X	X	LOW
HIGH	X	> UVLO_F	HIGH	X	LOW
HIGH	X	> UVLO_F	X	HIGH	LOW
HIGH	VOUT > 0.95 * target-VOUT	> UVLO_F	LOW	LOW	HIGH Z

8.4 Device Functional Modes

8.4.1 Peak Current Mode Architecture

The TPS63802 is based on a Peak Current Mode Architecture. The Error Amplifier provides a peak current target (voltage that is translated into a equivalent current, see Figure 3), based on the current demand from the voltage loop. This target is compared with the actual inductor current during the ON-time. The ON-time is ended once the inductor current is equal to the current target and OFF-time is initiated. The OFF-time is calculated by the control and a function of V_I and V_O.

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Device Functional Modes (continued)

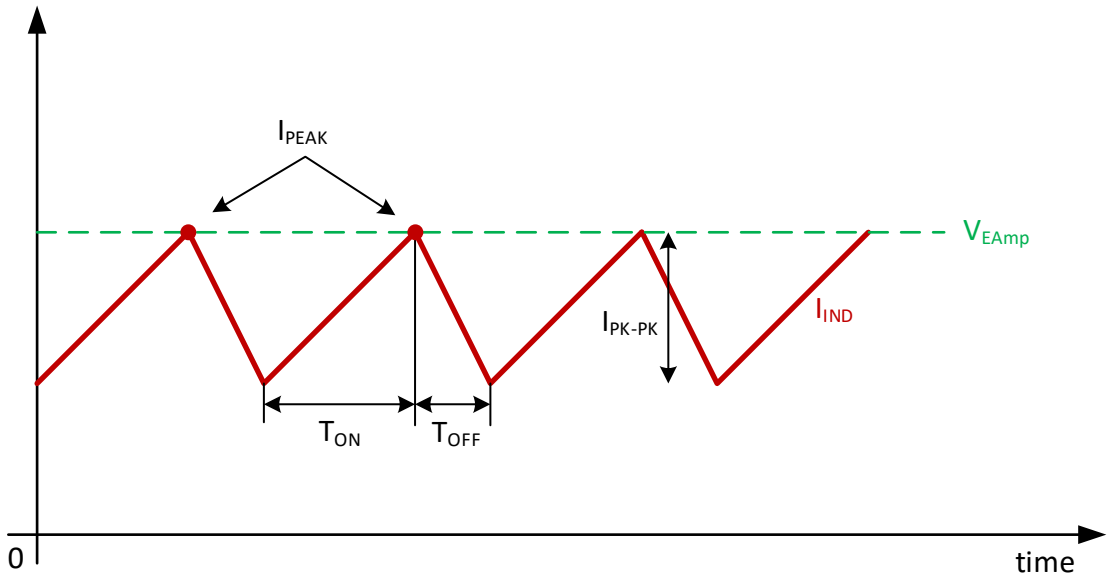

Figure 7. Peak Current Architecture Operation

8.4.1.1 Reverse Current Operation, Negative Current

When theTPS63802 is forced to PWM operation (MODE = HIGH), the device current can flow in reverse direction. This happens by the negative current capability of theTPS63802 . The Error Amplifier provides a peak current target (voltage that is translated into a equivalent current, see Figure 3), even so the target has a negative value. The maximum average current is even more negative than the peak current.

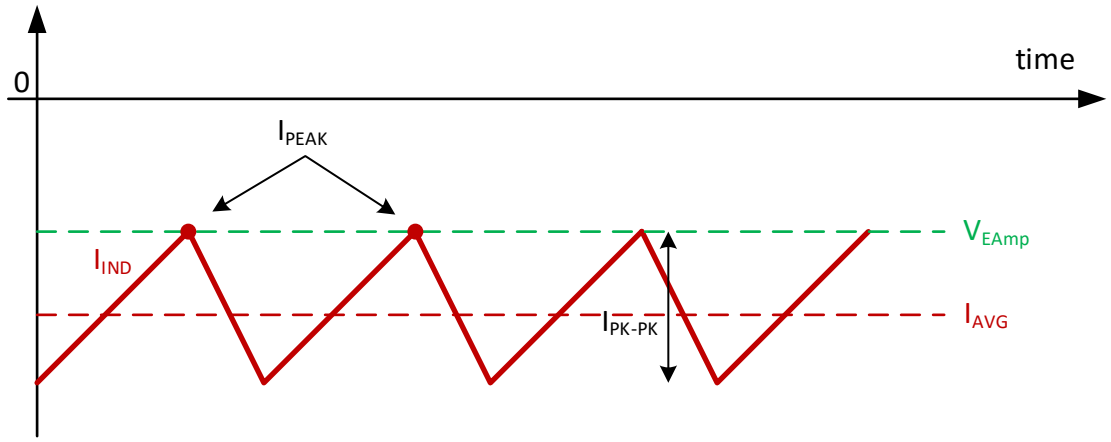

Figure 8. Peak Current Operation, Reverse Current

8.4.1.2 Boost Operation

When V_I is smaller than V_O (and the voltages are not close enough to trigger Buck-Boost operation),TPS63802 operates in Boost Mode where the Boost High-Side & Low-Side Switches are active. The Buck High-Side Switch is always turned on, the Buck Low-Side Switch is always turned off. This lets TPS63802 operate as a classical Boost Converter.

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Device Functional Modes (continued)

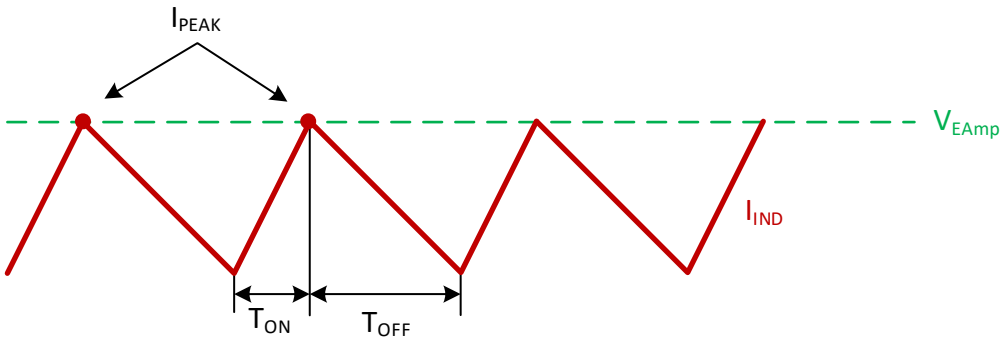

Figure 9. Peak Current Boost Operation

8.4.1.3 Buck-Boost Operation

When V_I is close to V_O, TPS63802 operates in Buck-Boost Mode, where all switches are active and the device repeats 3-cycles

- T_{ON}: Boost Charge Phase where Boost Low-Side and Buck High-Side are closed and inductor current is built up
- T_{OFF}: Buck Discharge Phase where Boost High-Side and Buck Low-Side are closed and inductor is discharged
- T_{COM}: V_I connected to V_O where all High-Side switches are closed and input is connected to output

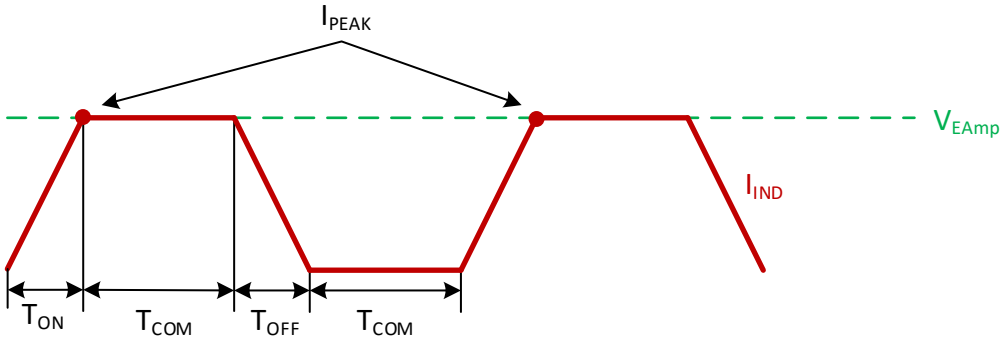

Figure 10. Peak Current Buck-Boost Operation

8.4.1.4 Buck Operation

When V_I is greater than V_O (and the voltages are not close enough to trigger Buck-Boost operation),TPS63802 operates in Buck Mode where the Buck High-Side & Low-Side Switches are active. The Boost High-Side Switch is always turned on, the Boost Low-Side Switch is always turned off. This lets TPS63802 operate as a classical Buck Converter.

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Device Functional Modes (continued)

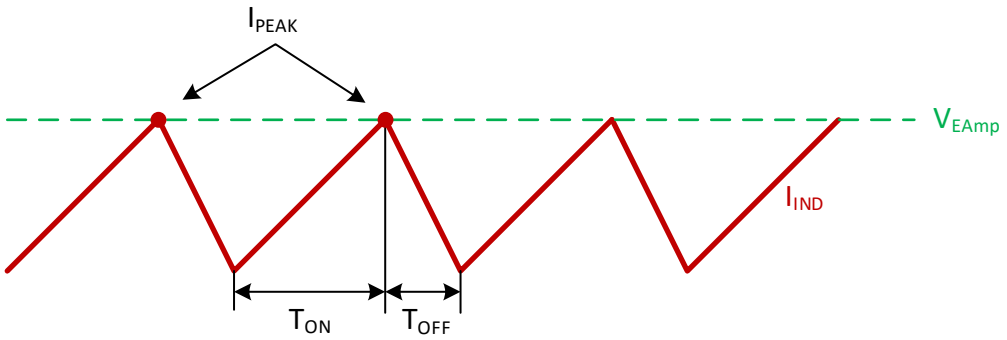

Figure 11. Peak Current Buck Operation

8.4.2 Power Save Mode Operation

Besides Continuos Conduction (PWM) Mode, TPS63802 features Power Safe (PFM) Mode operation to achieve high efficiency at light load currents. This is implented by pausing the switching operation depending on the load current.

The Skip Comparator manages the switching or pause operation. It compares the current demand signal from the Voltage Loop I_{REF} with the skip threshold I_{SKIP} as shown in Figure 3. If the current demand is lower than the skip value, the comparator pauses switching operation. If the current demand goes higher (due to falling V_O) the comparator activates the current loop and allows switching according to the loop behavior. Whenever the current loop has risen V_O by bringing charge to the output, the Voltage loop output I_{REF} (respectively V_{EA}) decreases. When I_{REF} falls below I_{SKIP}-Hysteresis, it automatically goes into pause again.

ADVANCE INFORMATION

Device Functional Modes (continued)

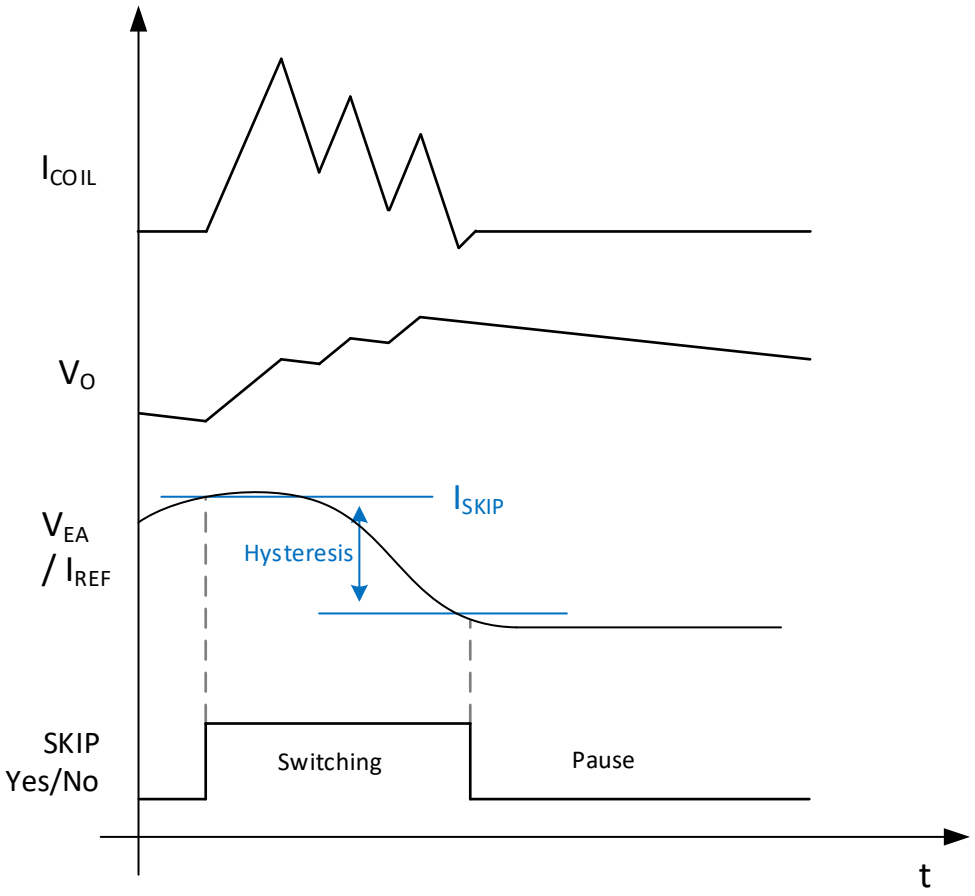

Figure 12. Power Safe Mode Operation Curves

8.4.2.1 Current Limit Operation

For limiting current and protecting the device and the application, the maximum peak inductor current is limited internally on the IC. It is measured at the Buck High-Side Switch which turns into an input current detection. To provide a certain load current across all Operation Modes, the Boost & Buck-Boost peak current limit is higher than in Buck Mode. It limits the input current and allows no further increase of the delivered current. When using the device in this Mode, it behaves similar to a current source.

The current limit depends on the operation Mode (Buck, Buck-Boost or Boost Mode) and is listed in the section

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS63802 is a high efficiency, high current Buck-Boost converter suitable for application where the input voltage is higher, lower or equal to the output voltage.

9.2 Typical Application

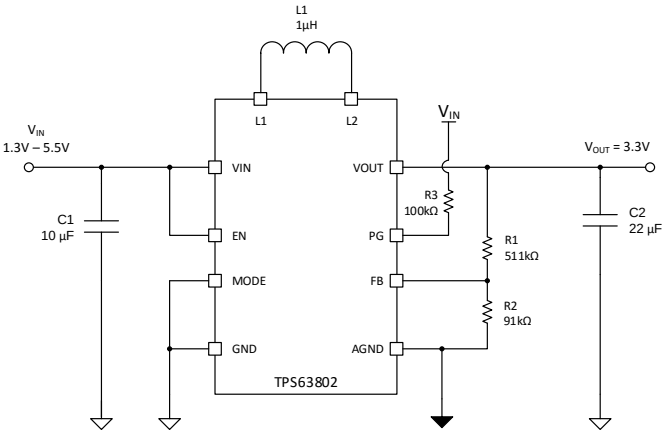

Figure 13. 3.3V_{OUT} Typical Application

9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions.

Table 2 shows the list of components for the Application Characteristic Curves.

Table 2. Components for Application Characteristic Curves(1)

REFERENCE	DESCRIPTION	Part Number	MANUFACTURER
	TPS63802 2A Buck-Boost Converter (2mmx3mm QFN)	TPS63802RMW	Texas Instruments
L1	1.0µH, 4mmx4mmx2mm, 5.4A, 10mΩ	XFL4020-102ME	Coilcraft
C1	10µF, 0603, Ceramic Capacitor, ±20%, 6.3V	GRM188R60J106ME84	Murata
C2	47uF, 0603, Ceramic Capacitor, ±20%, 6.3V	GRM188R60J476ME15	Murata
R1	511kΩ, 0603 Resistor, 1%, 100mW	Standard	Standard
R2	91kΩ, 0603 Resistor, 1%, 100mW	Standard	Standard
R3	100kΩ, 0603 Resistor, 1%, 100mW	Standard	Standard

(1) See *Third-Party Products Discalimer*

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9.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process outlines possible inductor and capacitor value combinations.

9.2.2.1 Output Capacitor

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. The recommended nominal output capacitor value is a single 22 µF for all programmed output voltages ≤ 4 V. Above that voltage 1x47 µFcapacitors are recommended. It is key to make sure that the effective capacitance is given according the recommended value in Recommended Operating Conditions. In general, consider DC-bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a tradeoff between size and transient behavior as higher capacitance reduces transient response over/undershoot.

There is no upper limit for the output capacitance value.

9.2.2.2 Input Capacitor Selection

A 10 µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS63802 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

9.2.2.3 Inductor Selection

The inductor selection is affected by several parameter like inductor ripple current, output voltage ripple, transition point into Power Save Mode, and efficiency. See Table 3 for typical inductors.

Table 3. List of Recommended Inductors(1)

INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (LxWxH mm)	Isat/DCR
1 µH	Coilcraft XAL4020-102ME	4 X 4 X 2	5.4A/10mΩ
1 µH	Toko, DFE322512C	32.5 X 2.0 X 1.2	4.7A/40mΩ
1 µH	Taiyo Yuden ,HTEK20161T-1R0MSR	2.0x1.6x1	4.2/43mΩ

(1) See *Third-party Products Disclaimer*

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 2. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{2}$$

Where,

- D =Duty Cycle in Boost mode
- f = Converter switching frequency (typical 2.5 MHz)
- L = Inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)

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NOTE

The calculation must be done for the minimum input voltage which is possible to have in boost mode

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It's recommended to choose an inductor with a saturation current 20% higher than the value calculated using *Equation 2*. Possible inductors are listed in *Table 3*.

9.2.2.4 Setting The Output Voltage

The output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB and GND. The feedback Voltage is 500 mV nominal. The low-side resistor R2 (between FB and GND) should not exceed 100 kΩ. The high-side resistor (between FB and VOUT) R1 is calculated by Equation 3.

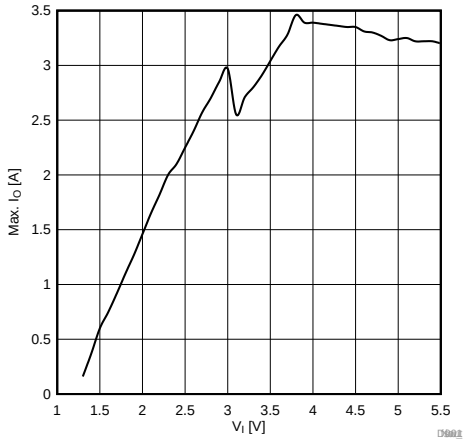
$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (3)$$

Table 4. Resistor selection for typ. voltages

VOUT	R1	R2
2.5 V	365 kΩ	91 kΩ
3.3 V	511 kΩ	91 kΩ
3.6 V	562 kΩ	91 kΩ
5 V	806 kΩ	91 kΩ

ADVANCE INFORMATION

9.2.3 Application Curves



V_O = 3.3 T_A = 25°C

Figure 14. Typical Output Current Capability vs. Input Voltage

Graph Placeholder

V_O= 5 V T_A = 25°C MODE = LOW

Figure 15. Efficiency vs. Output Current

Graph Placeholder

V_O = 3.3V T_A = 25°C MODE = LOW

Figure 16. Efficiency vs. Output Current

Graph Placeholder

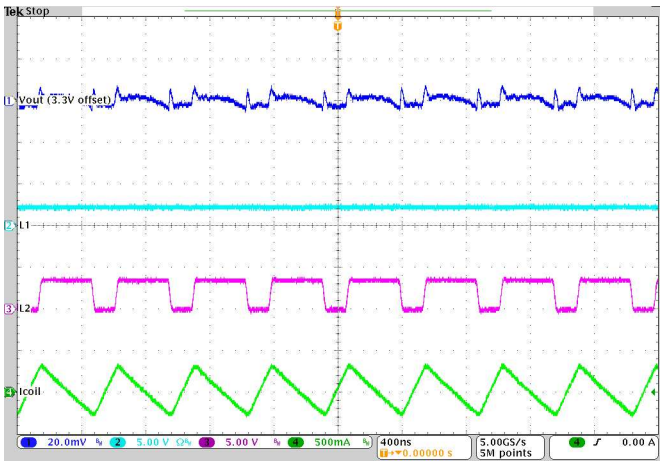
V_O = 3.3V T_A = 25°C MODE = HIGH

Figure 17. Efficiency vs. Output Current

Graph Placeholder

V_O = 1.8V T_A = 25°C MODE = LOW

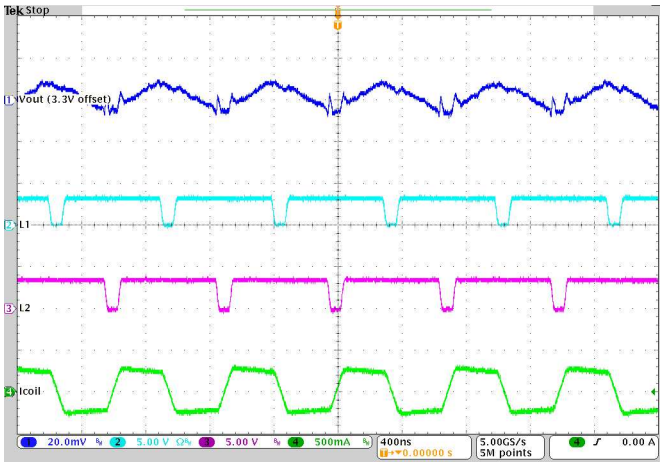
Figure 18. Efficiency vs. Output Current



V_I = 2.3V, V_O = 3.3V no Load, MODE = HIGH

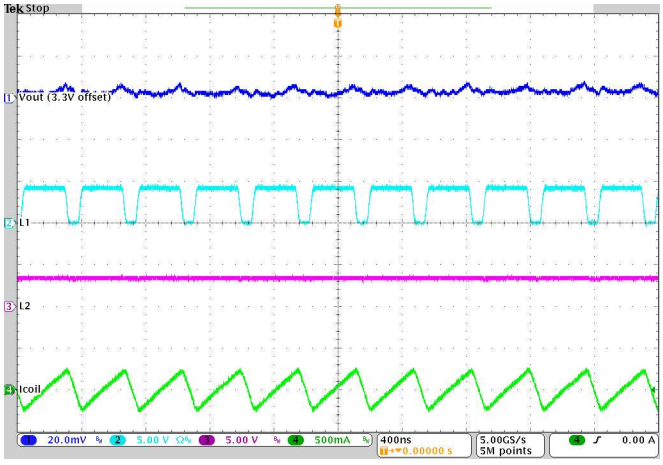
Figure 19. Switching Waveforms, PWM Boost Operation

ADVANCE INFORMATION



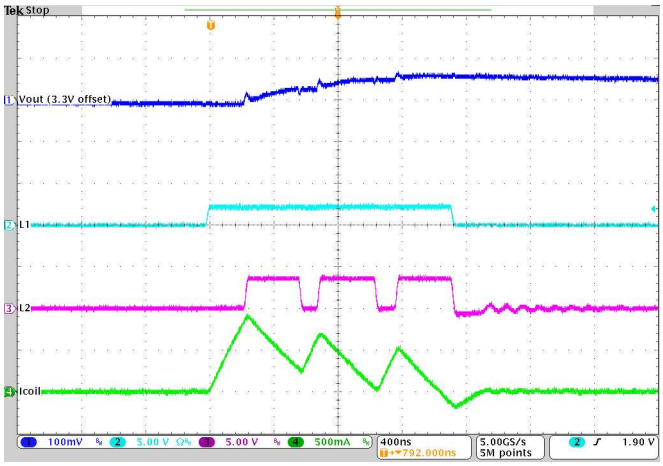
V_I = 3.3V, V_O = 3.3V no Load, MODE = HIGH

Figure 20. Switching Waveforms, PWM Buck-Boost Operation



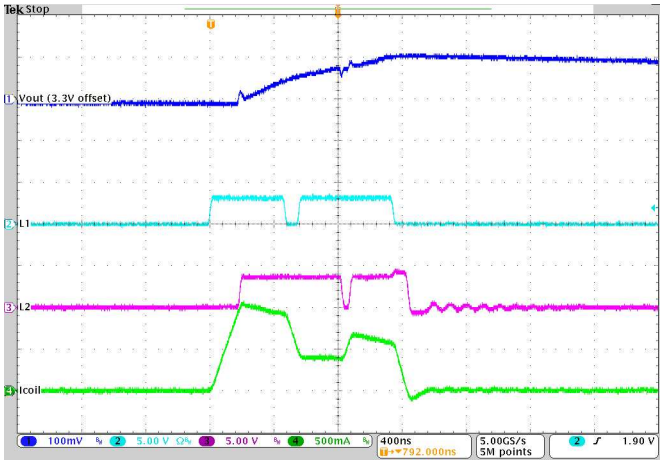
V_I = 4.3V, V_O = 3.3V no Load, MODE = HIGH

Figure 21. Switching Waveforms, PWM Buck Operation



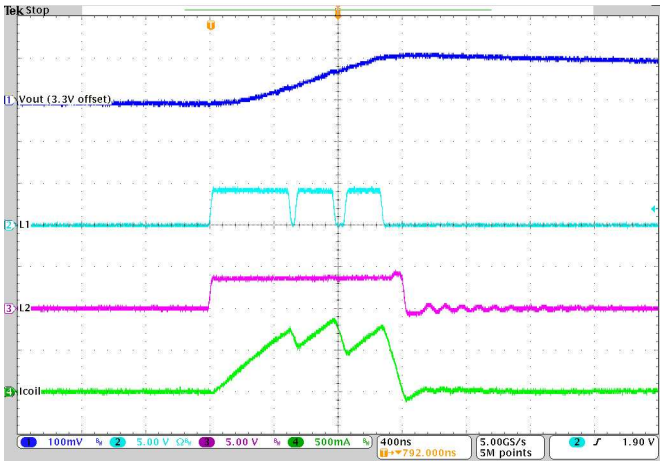
V_I = 4.3V, V_O = 3.3V no Load, MODE = LOW

Figure 22. Switching Waveforms, PFM Boost Operation



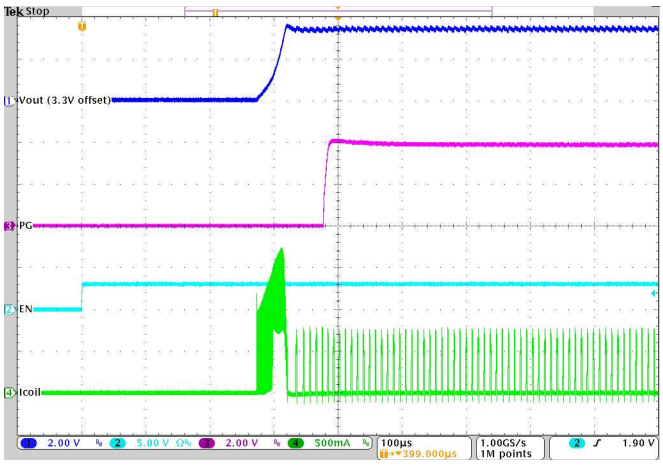
V_I = 4.3V, V_O = 3.3V no Load, MODE = LOW

Figure 23. Switching Waveforms, PFM Buck-Boost Operation



V_I = 4.3V, V_O = 3.3V no Load, MODE = LOW

Figure 24. Switching Waveforms, PFM Buck Operation



V_I = 3.8V, V_O = 3.3V 10mA load, MODE = LOW

Figure 25. Start-up Behavior from rising Enable

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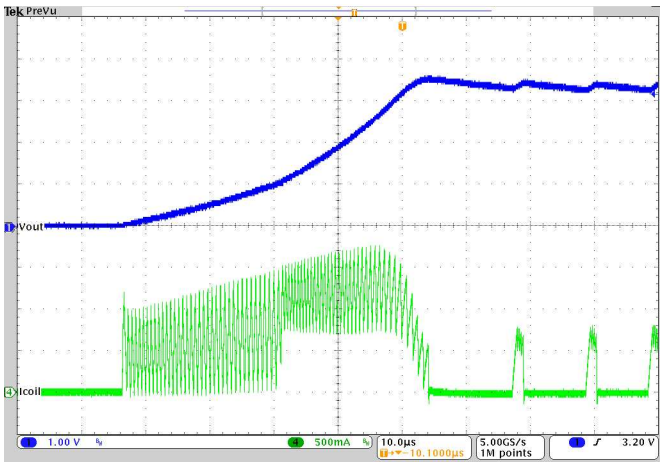
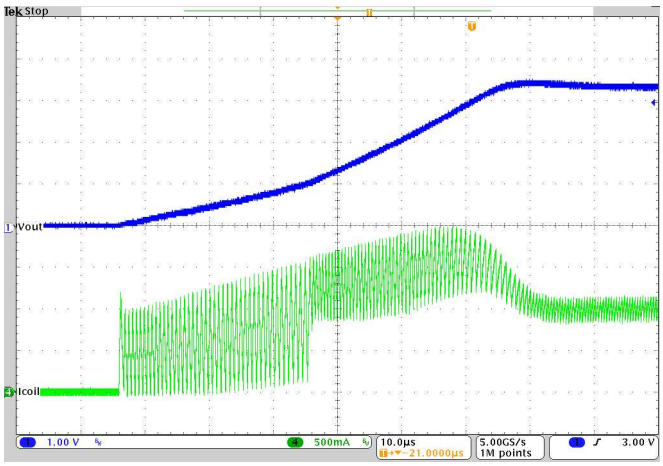


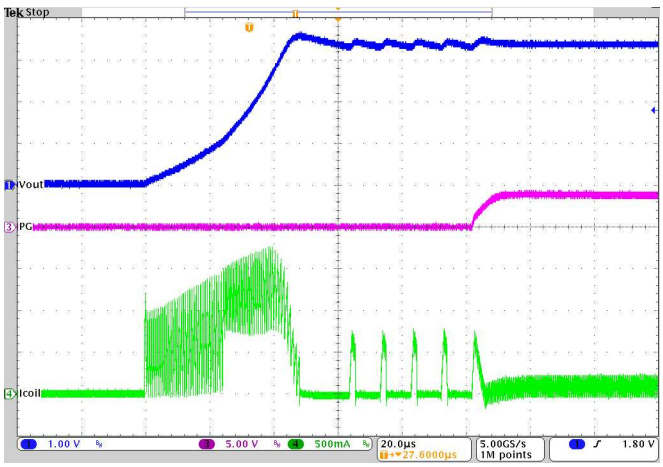
V_I = 3.8V, V_O = 3.3V 10mA load, MODE = LOW

Figure 26. Softstart Waveforms in PFM Mode



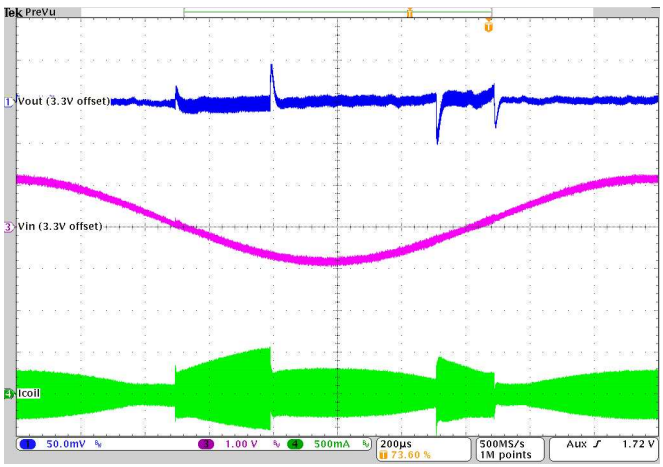
V_I = 3.8V, V_O = 3.3V 1A load, MODE = LOW

Figure 27. Softstart Waveforms in PFM Mode



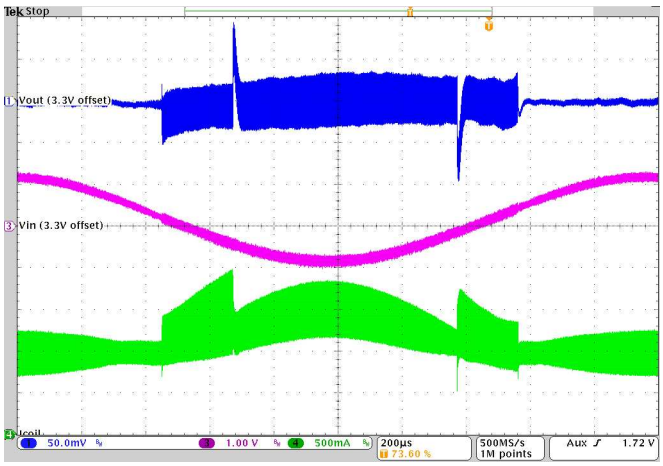
V_I = 3.8V, V_O = 3.3V 10mA load, MODE = HIGH

Figure 28. Softstart Waveforms in forced PWM Mode



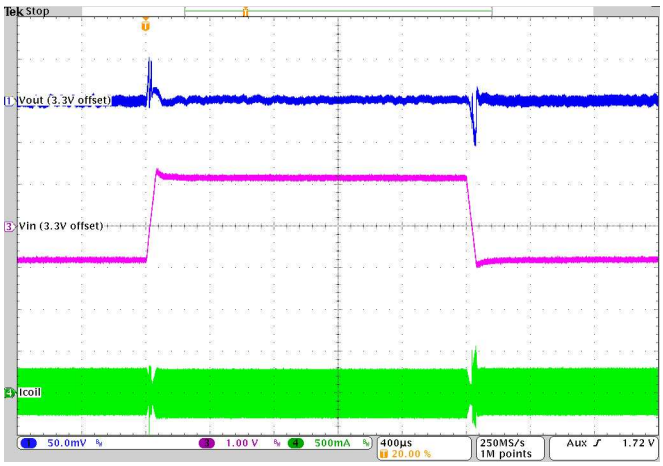
V_O = 3.3V 0mA load, MODE = HIGH

Figure 29. Linesweep Waveforms



V_O = 3.3V 1A load, MODE = HIGH

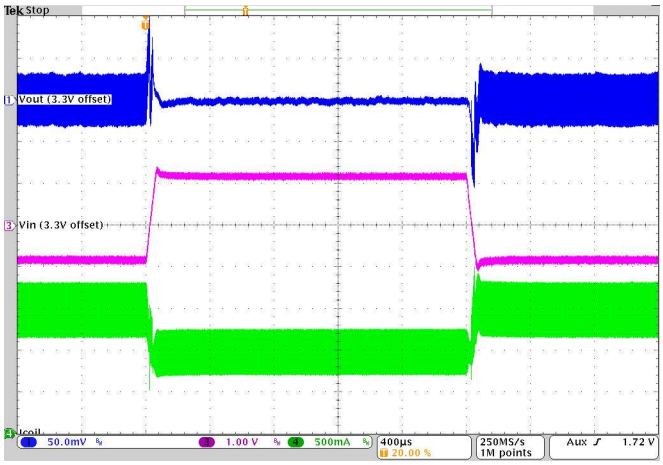
Figure 30. Linesweep Waveforms



V_O = 3.3V 0mA load, MODE = HIGH

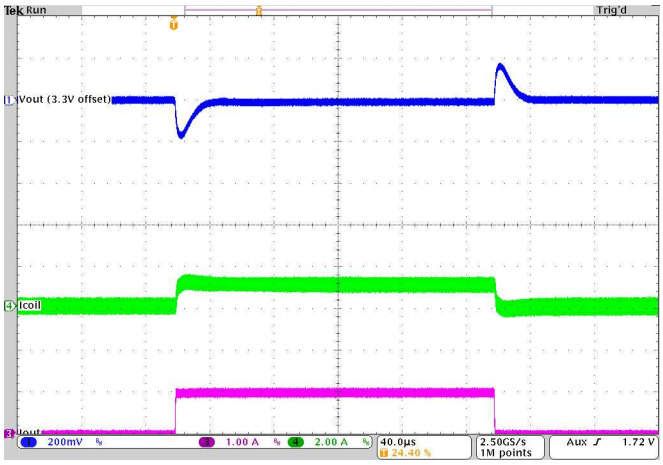
Figure 31. Linestep Waveforms

ADVANCE INFORMATION



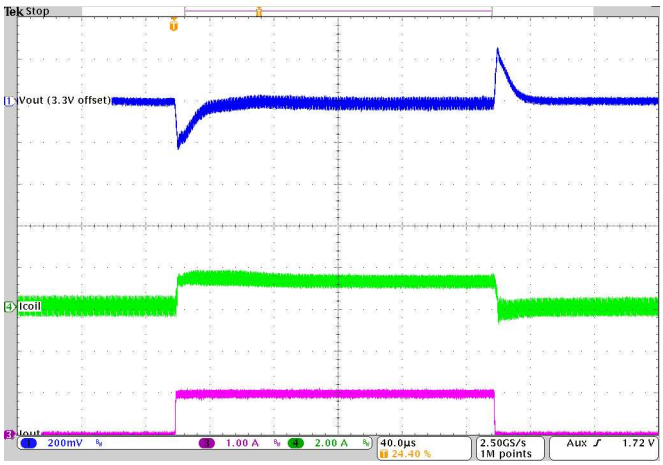
V_O = 3.3V 1A load, MODE = HIGH

Figure 32. Linestep Waveforms



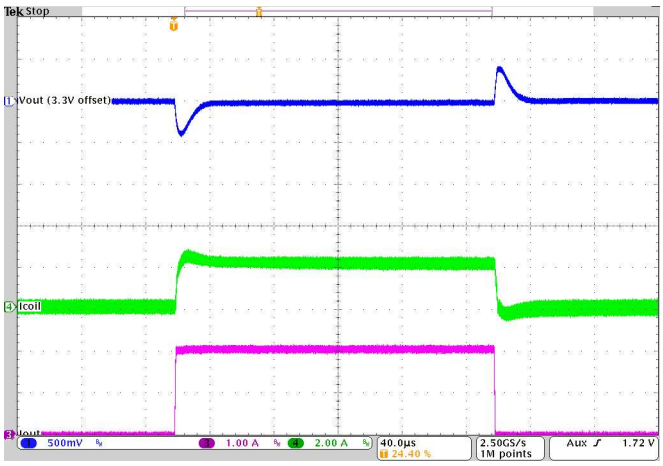
V_I = 4.3V, V_O = 3.3V V_O = 200mV/div

Figure 33. 1A-Loadstep Waveforms



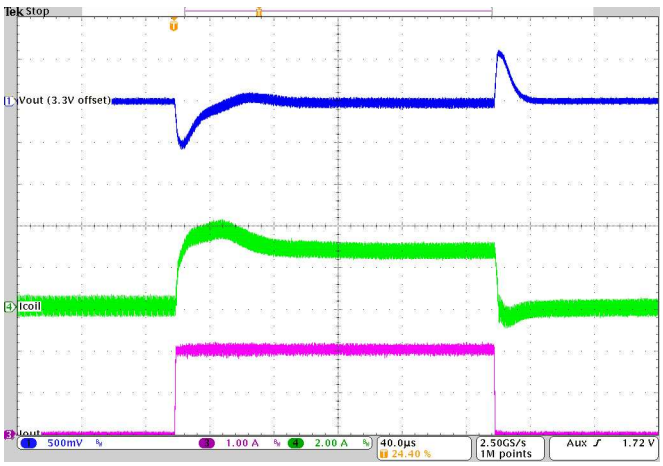
V_I = 3.0V, V_O = 3.3V V_O = 200mV/div

Figure 34. 1A-Loadstep Waveforms



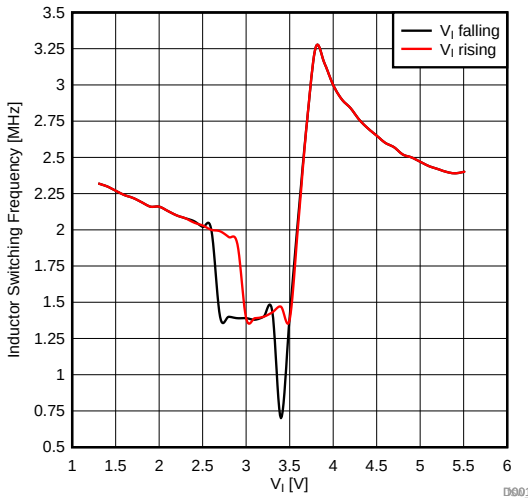
V_I = 4.3V, V_O = 3.3V V_O = 500mV/div

Figure 35. 2A-Loadstep Waveforms



V_I = 3.0V, V_O = 3.3V V_O = 500mV/div

Figure 36. 2A-Loadstep Waveforms



V_O = 3.3V no Load T_A = 25°C, MODE = HIGH

Figure 37. Typical Inductor Switching Frequency vs. Input Voltage

ADVANCE INFORMATION

10 Power Supply Recommendations

The TPS63802 device family has no special requirements for its input power supply. The input power supply output current needs to be rated according to the supply voltage, output voltage and output current of the TPS63802 .

11 Layout

11.1 Layout Requirements

The PCB layout is an important step to maintain the high performance of the TPS63802 devices.

- Place input and output capacitors as close as possible to the IC. Traces need to be kept short. Routing wide and direct traces to the input and output capacitor results in low trace resistance and low parasitic inductance.
- Separate AGND and PGND: Do not connect AGND and PGND directly at the IC! See as an example.
- Use a common-power GND but connect AGND & PGND through a via at a different layer.
- Use separate traces for the supply voltage of the power stage; and, the supply voltage of the analog stage.
- The sense trace connected to FB is signal trace. Keep these traces away from L1 and L2 nodes.

11.2 Layout Example

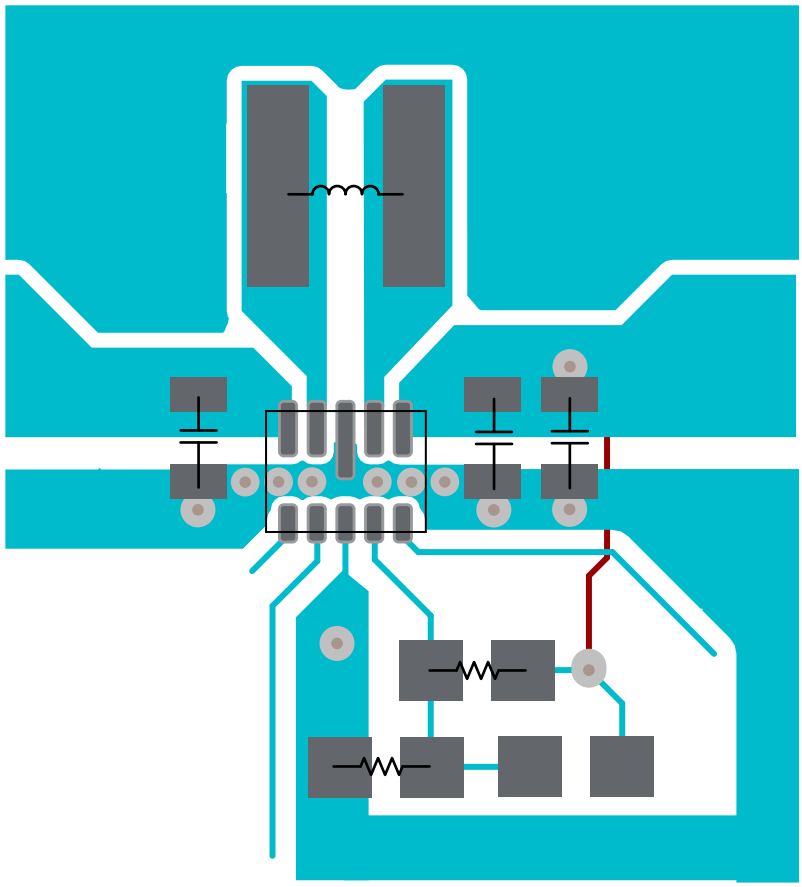


Figure 38. TPS6380x Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63802DLAR	PREVIEW	VSON-HR	DLA	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	63802	
TPS63802DLAT	PREVIEW	VSON-HR	DLA	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	63802	
XPS63802DLAT	ACTIVE	VSON-HR	DLA	10	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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