TPS566235 4.5-V to 18-V input, 6-A synchronous step-down converter

1 Features

- Input voltage range: 4.5 V to 18 V
- Output voltage range: 0.6 V to 7 V
- ±1% reference voltage at room temperature
- Supports 6-A continuous output current
- D-CAP3™ architecture control for fast transient response
- Integrated 25-mΩ and 12-mΩ $R_{DS(on)}$ power FETs
- 108-µA low quiescent current
- Selectable Eco-Mode™, Out-Of-Audio™ and FCCM by MODE pin
- Out-Of-Audio™ light-load operation with switching frequency over 25 kHz
- Supports pre-biased start up function
- 600-kHz switching frequency
- Internal 1-ms soft start
- Supports ceramic output capacitors
- Power good indicator
- Cycle-by-cycle valley over current protection
- Non-latched for OC, OV, UV, OT and UVLO protections
- 3.0-mm × 2.0-mm HotRod™ VQFN package
- Create a Custom Design Using the TPS566235 With the WEBENCH® Power Designer

2 Applications

- DTV and STB
- Switcher and router
- Server and enterprise SSD
- Surveillance and single board computer
- Distributed power systems

3 Description

The TPS566235 is a cost effective, high-voltage input, high efficiency synchronous BUCK converter with integrated FETs. It enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution.

The TPS566235 employs the D-CAP3™ mode control that provides a fast transient response and good line/load regulation with no external compensation components. It also has a proprietary circuit that enables the device to support low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors. The control topology supports seamless transition between CCM mode at heavy load conditions and DCM operation at light load conditions. There are three operation modes can be configured by MODE pin at light load: Eco-Mode™, Out-Of-Audio™ (OOA) and Forced Continuous Conduction Mode (FCCM). The OOA mode is a unique control feature that keeps the switching frequency above audible frequency with minimum reduction in efficiency.

The TPS566235 supports pre-biased start up and power good indicator. It provides complete protection including OVP, UVP, OCP, OTP and UVLO. The device is available in 3.0-mm x 2.0-mm HotRod™ package and the junction temperature is specified from –40°C to 125°C.

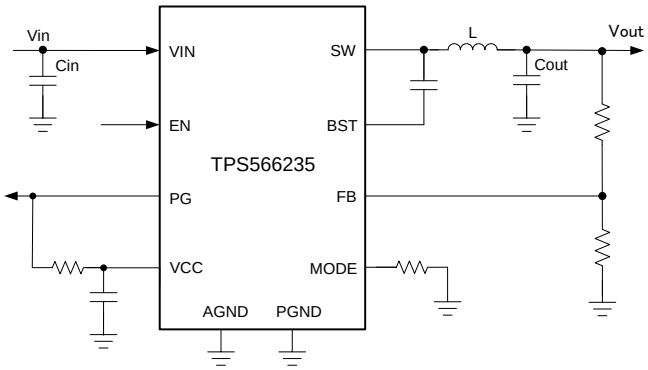
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS566235	VQFN (13)	3.00 mm × 2.00 mm

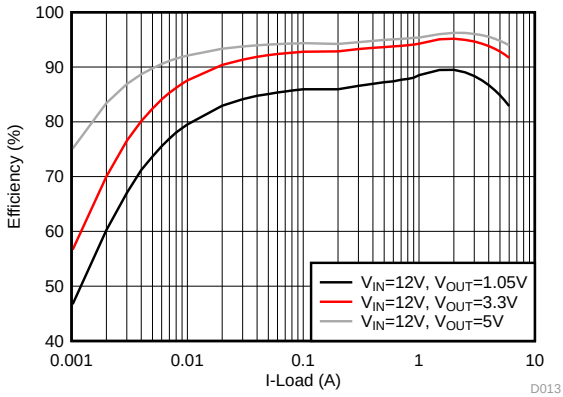
(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADVANCE INFORMATION

Typical Application



Efficiency vs Output Current Eco-mode



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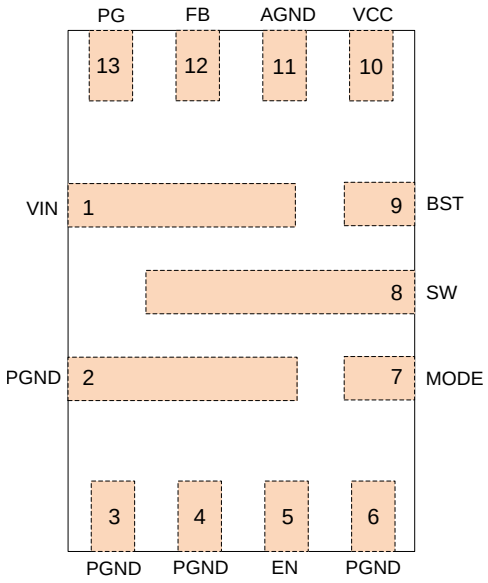
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2019) to Revision A	Page
• Changed Minimum Value for V_{CC}.	5
• Changed Minimum Value and Maximum Value for $V_{EN(ON)}$.	5
• Changed Typical Value for T_{OOA}.	6
• Deleted Maximum Value for T_{OOA}.	6
• Changed Typical Value for $T_{PGDLYLH}$.	6

5 Pin Configuration and Functions

RJN Package
13-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
PGND	2,3,4,6	G	Power GND terminal for the controller circuit and the internal circuitry.
EN	5	I	Enable pin of buck converter. EN pin is a digital input pin, decides turn on/off buck converter. Internal pull down current to disable converter if leave this pin open.
MODE	7	I	Eco-Mode™/OOA/FCCM Mode selection pin with external 1% resistor or connecting to VCC.
SW	8	O	Switching node connection to the output inductor and bootstrap capacitor.
BST	9	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect the bootstrap capacitor between BST and SW, 0.1 uF is recommended.
VCC	10	P	Internal LDO output for control and driver. Decouple with a minimum 1 μF ceramic capacitor as close to VCC as possible.
AGND	11	G	Ground of internal analog circuitry. Connect AGND to GND plane with a short trace.
FB	12	I	Feedback sensing pin for buck output voltage. Connect this pin to the resistor divider between output voltage and AGND.
PG	13	O	Open drain power good indicator. It is asserted low if output voltage is out of PG threshold, over voltage or if the device is under thermal shutdown, EN shutdown or during soft start.

ADVANCE INFORMATION

6 Specifications

7 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	20	V
	BST – SW	–0.3	6	V
	BST	–0.3	25	V
	FB, EN, MODE	–0.3	6	V
	PGND, AGND	–0.3	0.3	V
Output voltage	SW	–0.3	20	V
	SW (10-ns transient)	–3.0	22	V
	PG	–0.3	6	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

9 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	4.5	18	V
	BST – SW	–0.3	5.5	V
	BST	–0.3	23	V
	FB, EN, MODE	–0.3	5.5	V
	PGND, AGND	–0.3	0.3	V
Output voltage	SW	–0.3	18	V
	SW(10 ns transient)	–3.0	20	V
	PG, VCC	–0.3	5.5	V
I_{OUT}	Output current (1)		6	A
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–40	150	°C

(1) In order to be consistent with the TI reliability requirement of 100k Power-On-Hours at 105°C junction temperature, the output current should not exceed 6A continuously under 100% duty operation as to prevent electromigration failure in the solder. Higher junction temperature or longer power-on hours are achievable at lower than 6A continuous output current.

ADVANCE INFORMATION

10 Thermal Information

THERMAL METRIC(1)		TPS566235 RJN (VQFN) 13 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance with TI EVM	34.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

11 Electrical Characteristics

Tj = -40°C to 125°C, V_{IN} = 12 V, typical values are at Tj = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
V_{IN}	Input Voltage Range		4.5		18	V
I_{VIN}	VIN Supply Current	V_{EN} = 3.3V,Non Switching		108		µA
I_{VINSDN}	VIN Shutdown Current	V_{EN} = 0V		3		µA
VCC OUTPUT						
V_{CC}	VCC Output Voltage	V_{IN} > 5.0V	4.75	4.83	4.92	V
		V_{IN} = 4.5, no Load	4.3	4.5		V
I_{VCC}	VCC Current Limit		20			mA
FEEDBACK VOLTAGE						
V_{FB}	V_{FB} Voltage	T_J = 25°C	594	600	606	mV
		T_J = -40 to 125°C	591	600	609	mV
UVLO						
UVLO	VIN Under-Voltage Lockout	Wake up VIN voltage		4.2	4.4	V
		Shut down VIN voltage	3.6	3.7		V
		Hysteresis VIN voltage		500		mV
LOGIC THRESHOLD						
$V_{EN(ON)}$	EN Threshold High-level		1.24	1.32	1.4	V
$V_{EN(OFF)}$	EN Threshold Low-level		1.05	1.12	1.19	V
I_{EN}	EN Pull Down Current	V_{EN} = 0.8V		2		µA
I_{MODE}	MODE Sourcing Current			5		µA

ADVANCE INFORMATION

Electrical Characteristics (continued)

Tj = -40°C to 125°C, V_{IN} = 12 V, typical values are at Tj = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET						
$R_{DS(ON)H}$	High Side MOSFET Rds(on)			25		mΩ
$R_{DS(ON)L}$	Low Side MOSFET Rds(on)			12		mΩ
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching Frequency			600		kHz
T_{MIN_ON}	Minimum On-time			50		ns
T_{MIN_OFF}	Minimum Off-time				200	ns
OOA Function						
T_{OOA}	Mode Operation Period			32		µs
SOFT START						
T_{SS}	Soft Start Time			1		ms
POWER GOOD						
$T_{PGDLYLH}$	PG Low to High Delay	PG from low to high		160		µs
$T_{PGDLYHL}$	PG High to Low Delay	PG from high to low		32		µs
V_{PGTH}	PG Threshold	V_{FB} falling (fault)		85		%
		V_{FB} rising (good)		90		%
		V_{FB} rising (fault)		115		%
		V_{FB} falling (good)		110		%
I_{PGSK}	PG Sink Current	V_{PG} = 0.5V		52		mA
I_{PGLK}	PG Leak Current	V_{PG} = 5.5V			1	µA
CURRENT LIMIT						
I_{OCL}	Over Current Threshold	Valley current set point	6.6	7.6	8.6	A
I_{NOCL}	Negative Over Current Threshold			3.4		A
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP Trip Threshold	V_{FB} rising (fault)		125		%
		V_{FB} falling (good)		120		%
t_{OVPDLY}	OVP Prop Deglitch			32		µs
V_{UVP}	UVP Trip Threshold	V_{FB} falling (fault)		60		%
		V_{FB} rising (good)		65		%
t_{UVPDLY}	UVP Prop Deglitch			256		µs
THERMAL PROTECTION						
T_{OTP}	OTP Trip Threshold(1)			150		°C
T_{OTPHYS}	OTP Hysteresis(1)			20		°C

(1) Not production tested

ADVANCE INFORMATION

11.1 Typical Characteristics

T_J=-40°C to 125°C, V_{IN}=12V(unless otherwise noted)

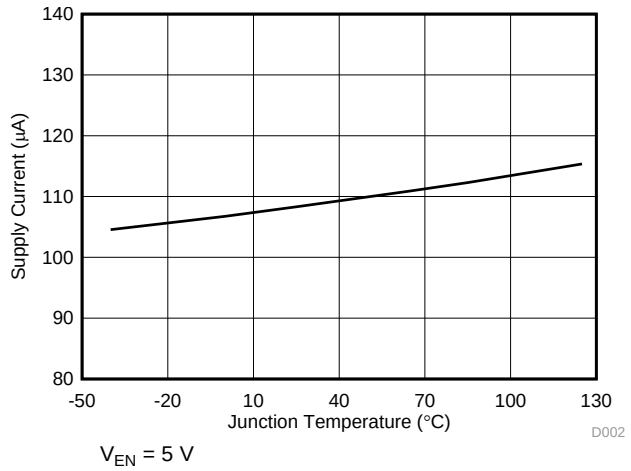


Figure 1. Supply Current vs Junction Temperature

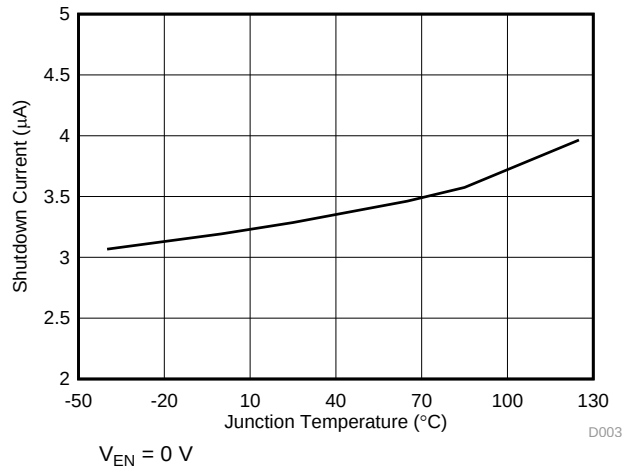


Figure 2. Shutdown Current vs Temperature

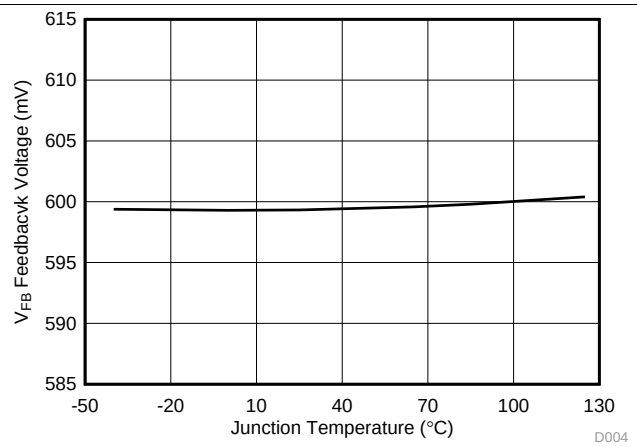


Figure 3. Feedback Voltage vs Junction Temperature

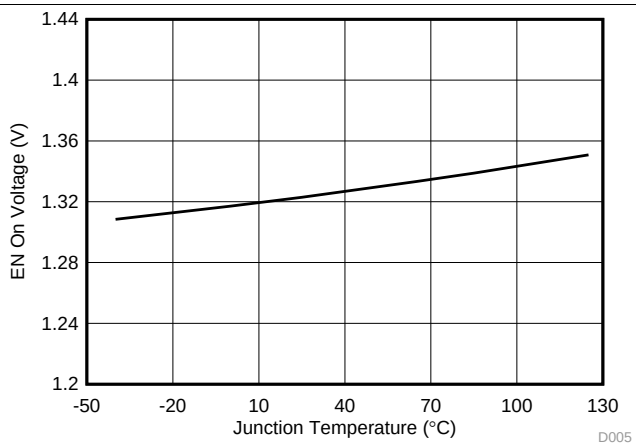


Figure 4. Enable On Voltage vs Junction Temperature

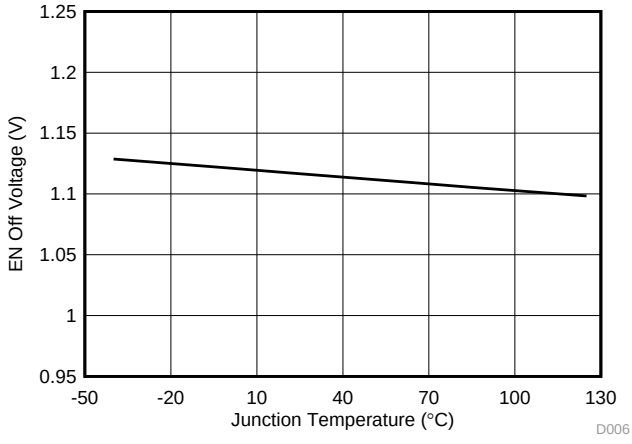


Figure 5. Enable Off Voltage vs Junction Temperature

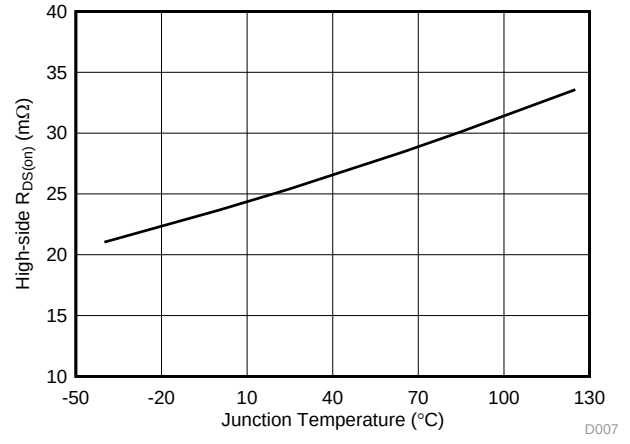


Figure 6. High-Side R_{DS}(on) vs Junction Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

T_J=-40°C to 125°C, V_{IN}=12V(unless otherwise noted)

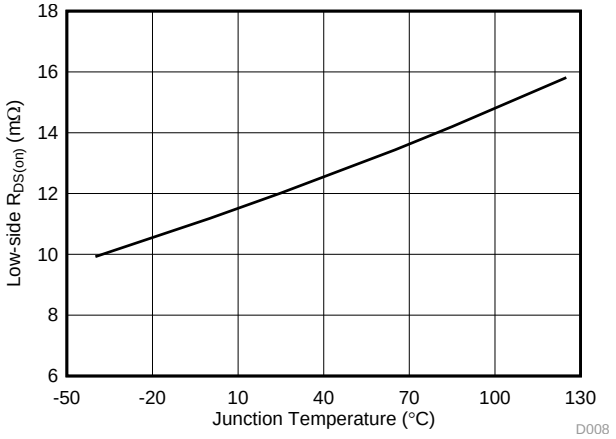


Figure 7. Low-Side $R_{DS(on)}$ vs Junction Temperature

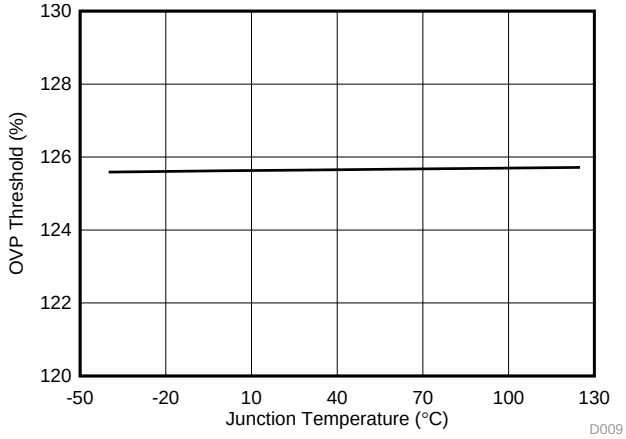


Figure 8. OVP Threshold vs Junction Temperature

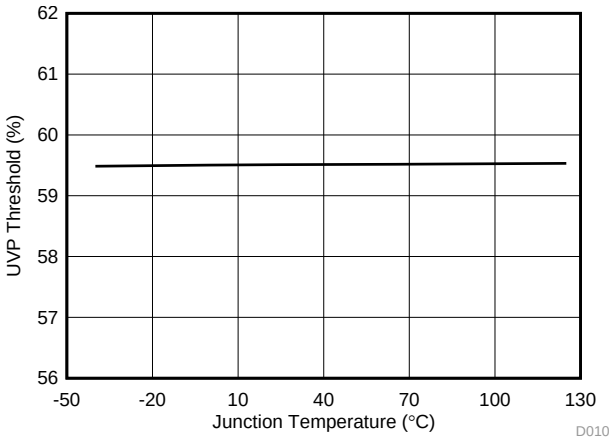


Figure 9. UVP Threshold vs Junction Temperature

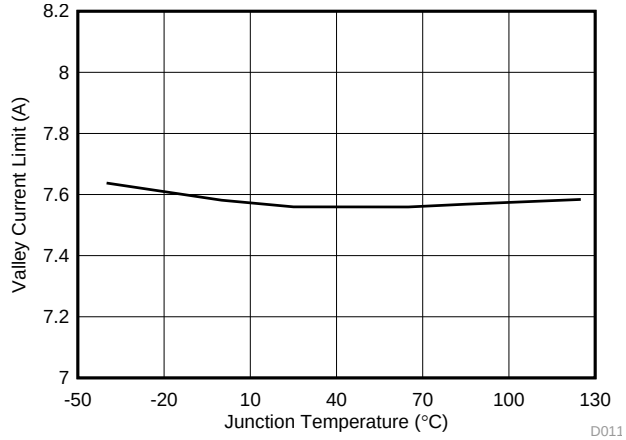


Figure 10. Valley Current Limit vs Junction Temperature

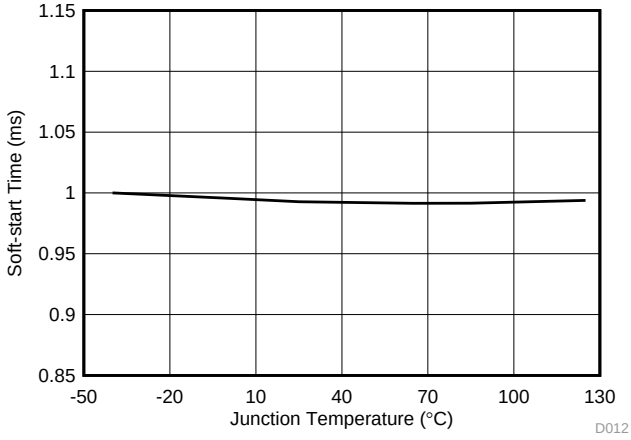


Figure 11. Soft-Start Time vs Junction Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

T_J=-40°C to 125°C, V_{IN}=12V(unless otherwise noted)

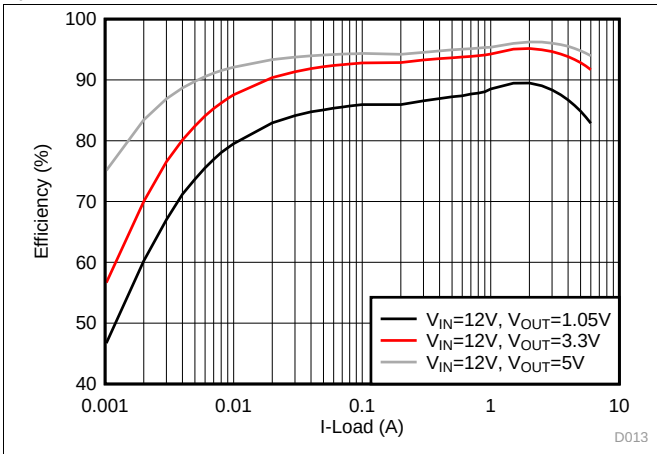


Figure 12. Efficiency, Eco-mode

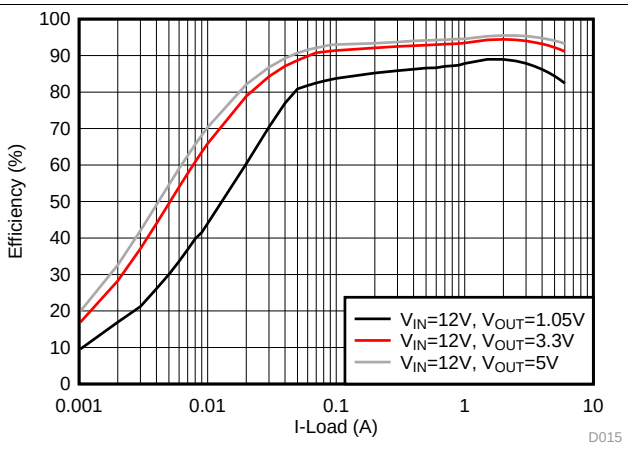


Figure 13. Efficiency, OOA-mode

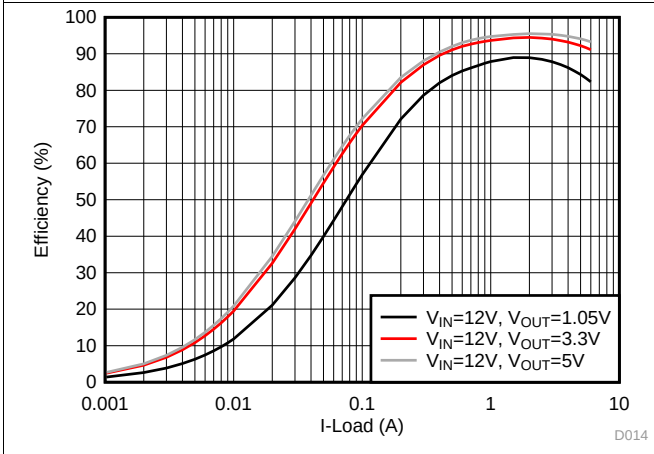


Figure 14. Efficiency, FCCM

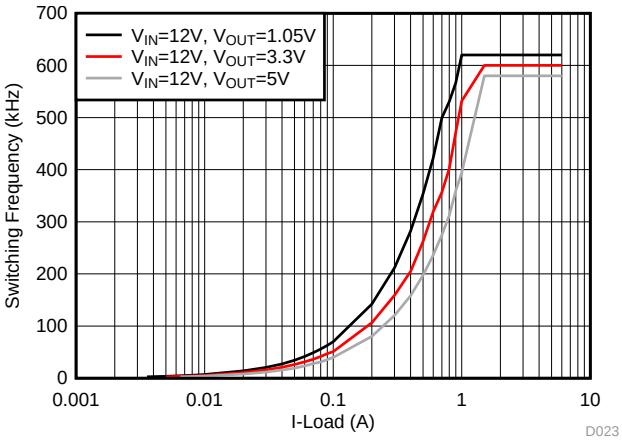


Figure 15. Switching Frequency vs Output Load, Eco-mode

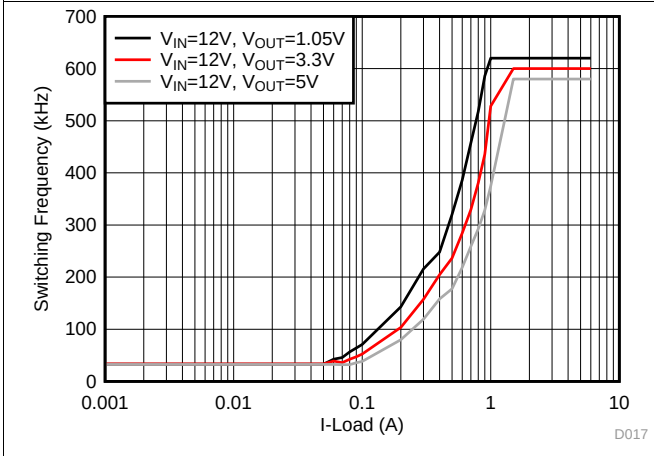


Figure 16. Switching Frequency vs Output Load, OOA-mode

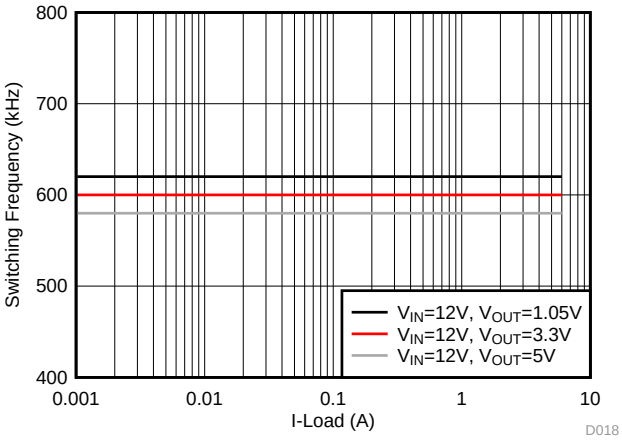


Figure 17. Switching Frequency vs Output Load, FCCM

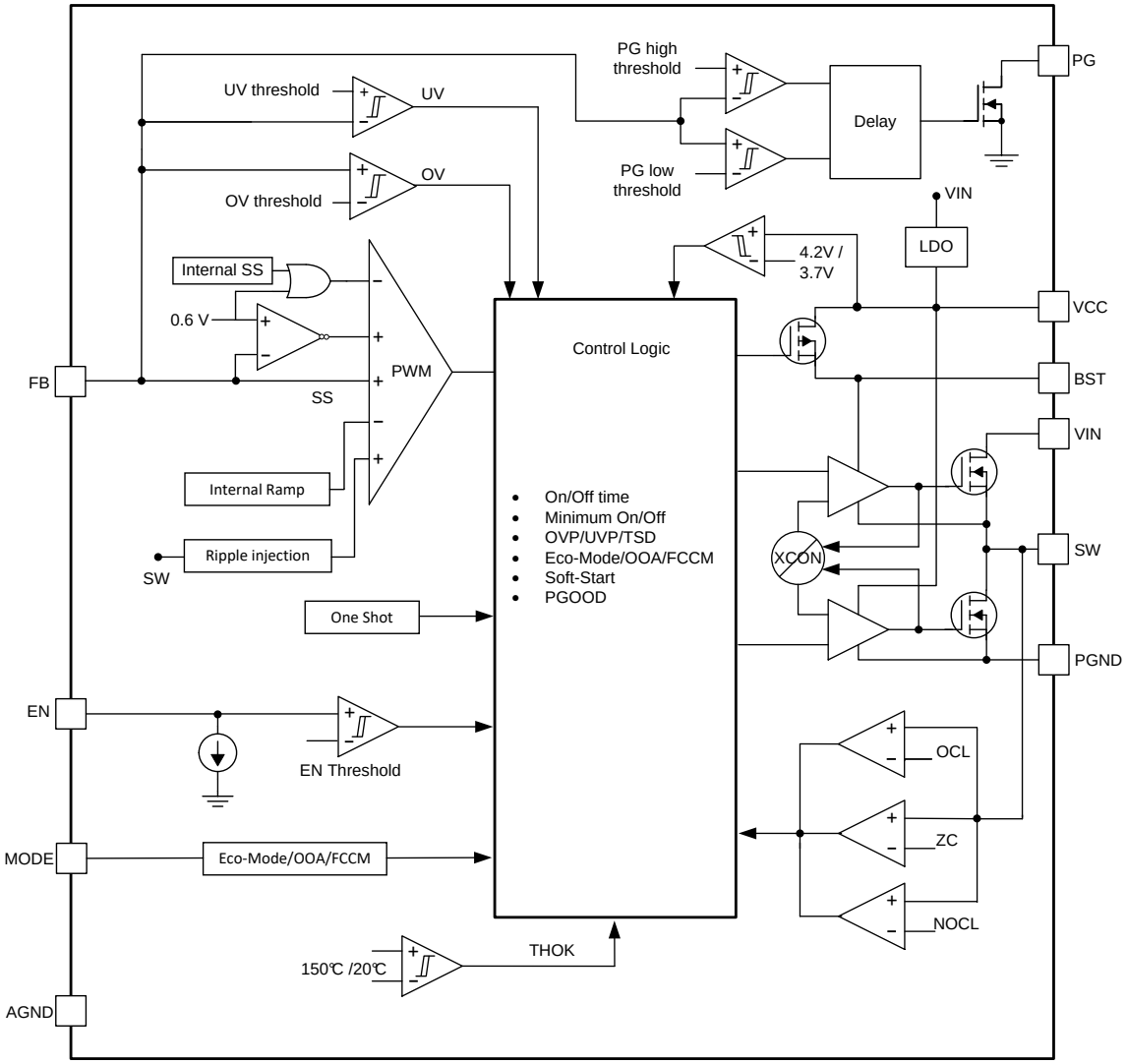
ADVANCE INFORMATION

12 Detailed Description

12.1 Overview

The TPS566235 is high density synchronous BUCK converter which operates from 4.5 V to 18 V input voltage (V_{IN}), and the output range is from 0.6 V to 7 V. It has 25-mΩ and 12-mΩ integrated MOSFETs that enable high efficiency up to 6 A. The proprietary D-CAP3™ mode enables low external component count, ease of design, optimization of the power design for cost, size and efficiency. The TPS566235 has ultra-low quiescent current (ULQ™) mode. This feature is beneficial for long battery life in system standby mode. The device employs D-CAP3™ mode control that provides fast transient response with no external compensation components. The control topology supports seamless transition between CCM mode at heavy load conditions and DCM operation at light load conditions. There are three operation modes can be configured by MODE pin at light load: Eco-Mode™, OOA and FCCM. Eco-Mode™ allows the TPS566235 to maintain high efficiency at light load. OOA mode makes switching frequency above audible frequency (25kHz), even there is no loading at output side. FCCM mode has the constant switching frequency at both light and heavy load. TPS566235 are able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

12.2 Functional Block Diagram



12.3 Feature Description

12.3.1 PWM Operation and D-CAP3™ Control

The main control loop of the BUCK is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3™ mode control. The D-CAP3™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS566235 also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and it is inversely proportional to the converter input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3™ control topology.

For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS566235 is a low-pass L-C circuit. This L-C filter has a double-pole frequency described in Equation 1.

$$f_p = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS566235. The low-frequency L-C double pole has a 180 degree drop in phase. At the output filter frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is related to the switching frequency. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency (F_{SW}).

12.3.2 Power Good

The Power Good (PG) pin is an open drain output. Once the FB pin voltage is between 90% and 110% of the internal reference voltage (V_{REF}=0.6V), the PG is de-asserted and floats after a 160 µs de-glitch time. A pull-up resistor of 100 kΩ is recommended to pull it up to VCC. The PG pin is pulled low when the FB pin voltage is lower than 85% or greater than 115% threshold or in an event of thermal shutdown or during the soft-start period. PG de-glitch time (from high to low) is 32 µs.

12.3.3 Over current Protection and Undervoltage Protection

The TPS566235 has the over current protection and undervoltage protection. The output over current limit (OCL) is implemented using a cycle-by-cycle valley detect circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over current protection. When the load current is higher than the over current threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it, the device will shut off after a wait time of 256 µs and then re-start after the hiccup time (typically 7xTss). When the over current condition is removed, the output will be recovered.

ADVANCE INFORMATION

Feature Description (continued)

12.3.4 Over Voltage Protection

TPS566235 has the over voltage protection function by monitoring the feedback voltage (V_{FB}). When the feedback voltage becomes higher than 125% of V_{REF}, the OVP comparator output goes high and turns off both high-side and low-side MOSFETs after a wait time of 32 µs. This protection is a non-latching operation. The device re-starts switching when the feedback voltage falls below 120% of V_{REF}.

12.3.5 UVLO Protection

The undervoltage lockout (UVLO) protection monitors the VCC pin voltage to protect the internal circuitry from low input voltages. When the voltage is lower than UVLO threshold voltage, the under-voltage lockout circuit prevents mis-operation of the device by turning off both high-side and low-side MOSFETs. The converter begins operation again when the input voltage exceeds the threshold by a hysteresis of 500 mV (typical).This is a non-latch protection.

12.3.6 Thermal Shutdown

The device monitors the internal die temperature. If it exceeds the thermal shutdown threshold value (typically 150°C), the device shuts off. This is a non-latch protection.

12.4 Device Functional Modes

12.4.1 Light Load Operation

TPS566235 has a MODE pin which can setup three different modes of operation for light load running. The light load operation mode includes Eco-Mode™, Out-Of-Audio™ mode and FCCM mode.

12.4.2 Advanced Eco-Mode™ Control

The advanced Eco-Mode™ control scheme to maintain high efficiency at light loads. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it is in continuous conduction mode so that it takes more time to discharge the output to the level of reference voltage with a smaller load current. The light load current where the transition to Eco-Mode™ operation happens ($I_{OUT(LL)}$) can be calculated from Equation 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{OUT(max)}$ (peak current in the application).

12.4.3 Out-Of-Audio™ Mode

Out-Of-Audio™ (OOA) light-load mode is a unique control feature that keeps the switching frequency above audible frequency with minimum reduction in efficiency. It prevents audio noise generation from the output capacitors and inductor. During Out-of-Audio operation, the OOA control circuit monitors the states of both high-side and low-side MOSFETs and forces them switching if both MOSFETs are off for more than 32 µs. When both high-side and low-side MOSFETs are off for more than 32 µs during a light-load condition, the low side FET will discharge until reverse OC happens or output voltage drops to trigger the high-side FET on.

If the MODE pin is selected to operate in OOA mode, when the device works at light load, the minimum switching frequency is above 25 kHz which avoids the audible noise in the system.

ADVANCE INFORMATION

Device Functional Modes (continued)

12.4.4 Force CCM Mode

Force CCM (FCCM) mode keeps the converter to operate in continuous conduction mode during light-load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency (F_{SW}) is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

12.4.5 MODE Pin Configuration

TPS566235 detect the voltage on the MODE pin during start-up and latches onto one of the MODE options listed below in Table 1. TPS566235 internally has a comparator to compare this voltage with reference voltage and decide which mode to choose. The voltage on the MODE pin can be set by connecting to VCC pin or connecting a resistor R_M between this pin and AGND. There is a source current of 5 µA at the mode pin and generate voltage for mode selection to avoid noise and spurious trigger. The V_{MODE} voltage range and recommended resistor value is shown in Table 1. The MODE pin setting can be reset only by VIN power cycling or EN toggle.

Table 1. Mode Pin Settings

V_{MODE}	0-0.3 V	0.3 V-1.2 V	>1.2 V
Recommended Resistor	0 Ω	100 kΩ-150 kΩ	To VCC (recommend) or R_M>400kΩ
Operating Mode	Eco-Mode™	OOA	FCCM

Figure 18 shows the typical start-up sequence of the device once the enable signal crosses the EN turn on threshold (V_{IN} is higher then UVLO threshold). After the voltage on VCC crosses the rising UVLO threshold, it takes about 60 µs to read the mode setting .The output voltage starts ramping after 10 µs from the mode reading is done.

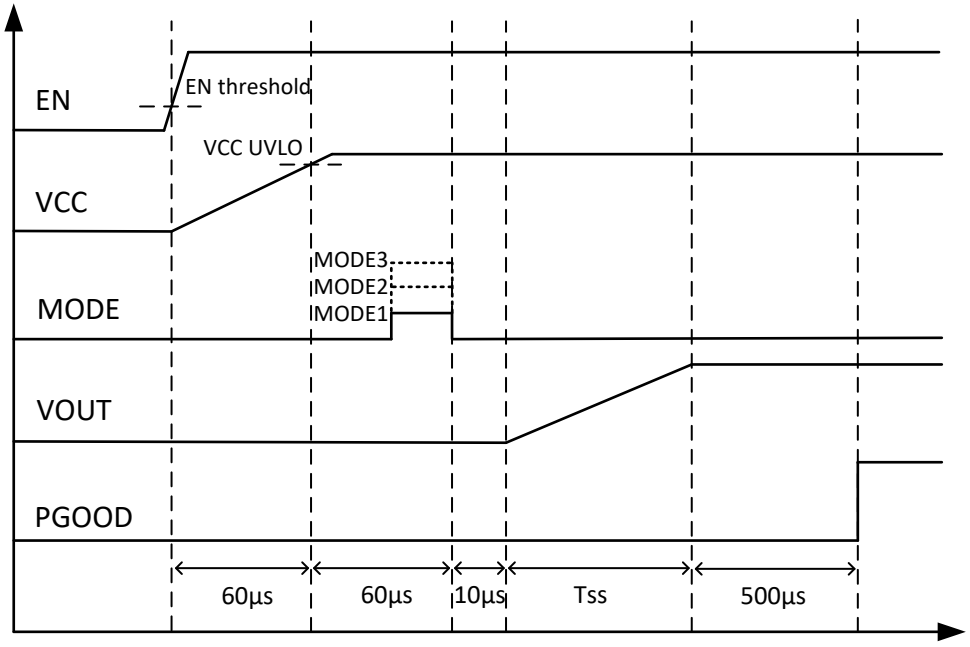


Figure 18. Start-Up Sequence

12.4.6 Standby Operation

The TPS566235 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 3 µA when in standby condition. EN pin is pulled low internally when it is floating and the device is disabled by default.

ADVANCE INFORMATION

13 Application and Implementation

NOTE

Information in the following application sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

13.1 Application Information

The schematic of Figure 19 shows a typical application for TPS566235. This design converts an input voltage range of 4.5 V to 18 V down to 1.05 V with a maximum output current of 6 A.

13.2 Typical Application

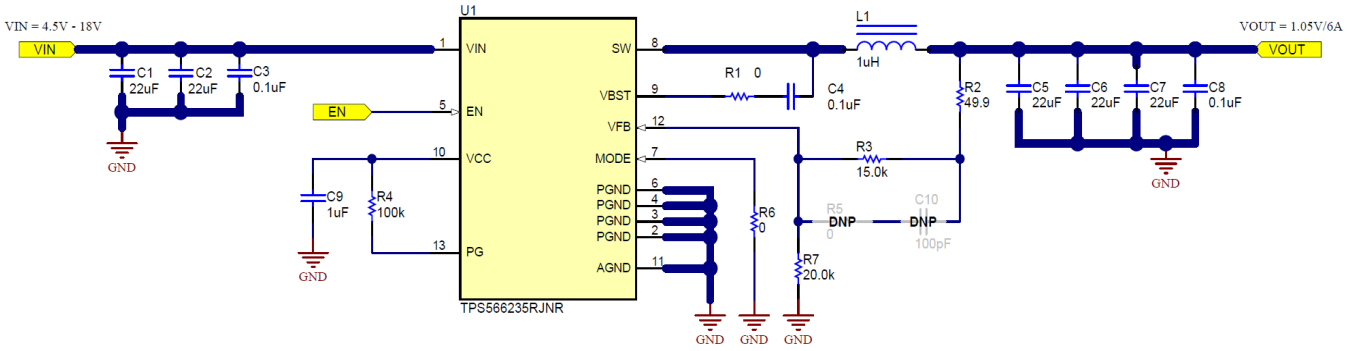


Figure 19. Application Schematic

13.2.1 Design Requirements

Table 2. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			1.05		V
I_{OUT}	Output current			6		A
ΔV_{OUT}	Transient response	I_{OUT}: 10%-90%, 2.5A/µs		±5% x V_{OUT}		
V_{IN}	Input voltage		4.5	12	18	V
$V_{OUT(ripple)}$	Output voltage ripple			2% x V_{OUT}		
F_{SW}	Switching frequency			600		kHz
	Light load operation mode			Eco-Mode™		
T_A	Ambient temperature			25		°C

13.2.2 Detailed Design Procedure

13.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS566235 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance

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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

13.2.2.2 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor should have a ripple current rating higher than the inductor ripple current. See Table 3 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using Equation 3 and Equation 4. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{\left(I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT} \right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}} \right)^2 \right)} \quad (3)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (4)$$

During transient/short circuit conditions the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

13.2.2.3 Output Capacitor Selection

After selecting the inductor the output capacitor needs to be optimized. In D-CAP3™, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in Table 3

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor should be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$

Table 3. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	L_{OUT} (µH)			C_{OUT} (µF)		C_{FF} (pF)	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX
1	20	13.3	0.68	1	4.7	44	110	-	-
1.05	20	15	0.68	1	4.7	44	110	-	-
1.2	20	20	1	1.2	4.7	44	110	-	-
1.5	20	30	1	1.2	4.7	44	110	-	-
1.8	20	40	1.2	1.5	4.7	44	110	-	-
2.5	20	63.3	1.5	2.2	4.7	44	110	-	-
3.3	20	90	1.5	2.2	4.7	44	110	10	220
5	30	220	1.5	2.2	4.7	44	110	10	220

13.2.2.4 Input Capacitor Selection

The minimum input capacitance required is given in Equation 5.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (5)$$

TI recommends using a high quality X5R or X7R input decoupling capacitors of 44 µF on the input voltage pin. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 6 below:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT} \right)}{V_{IN(min)}}} \quad (6)$$

ADVANCE INFORMATION

13.2.3 Application Curves

Figure 20 through Figure 35 applies to the circuit of Figure 19. V_{IN} = 12 V, T_J = 25°C (unless otherwise specified)

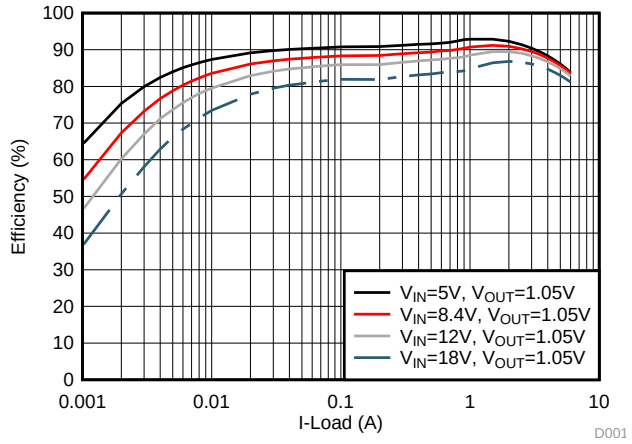


Figure 20. Efficiency Curve

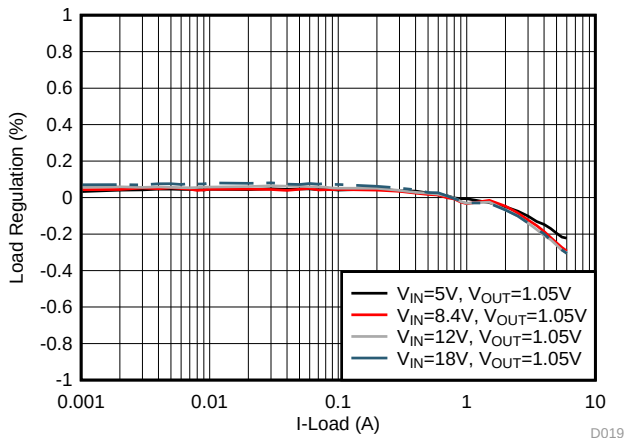


Figure 21. Load Regulation

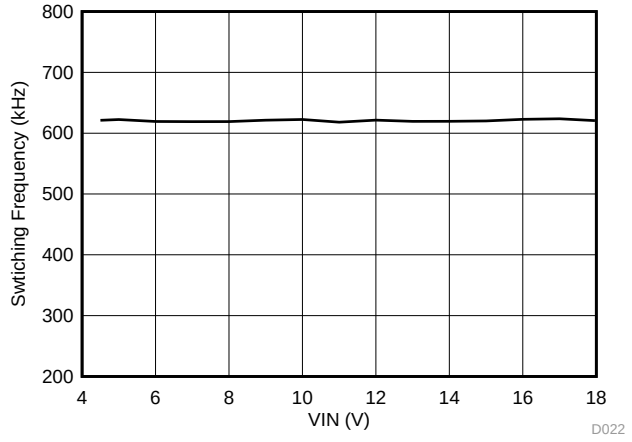


Figure 22. Switching Frequency vs Input Voltage

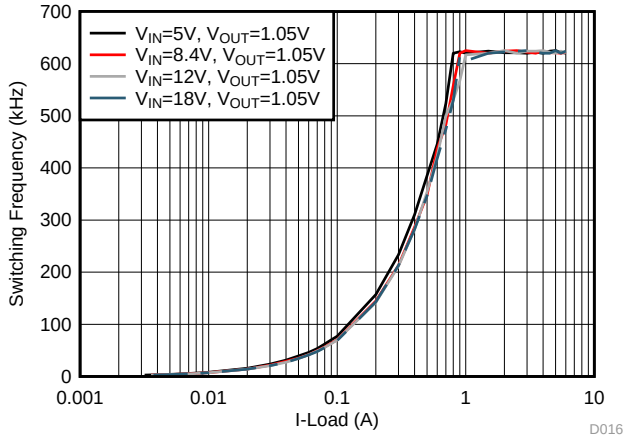


Figure 23. Switching Frequency vs Output Load

ADVANCE INFORMATION

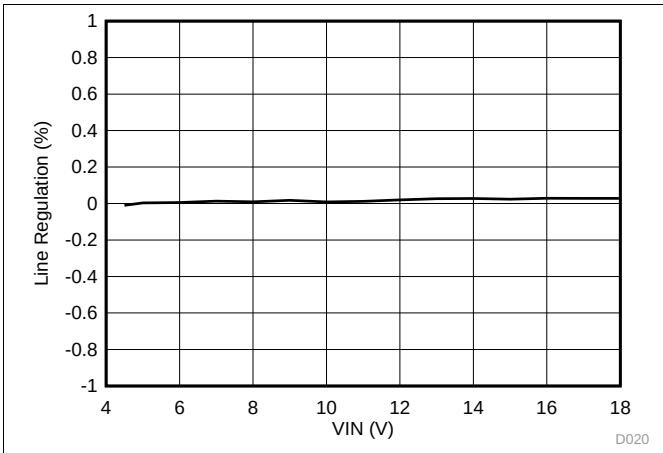


Figure 24. Line Regulation, I_{OUT} = 0.01 A

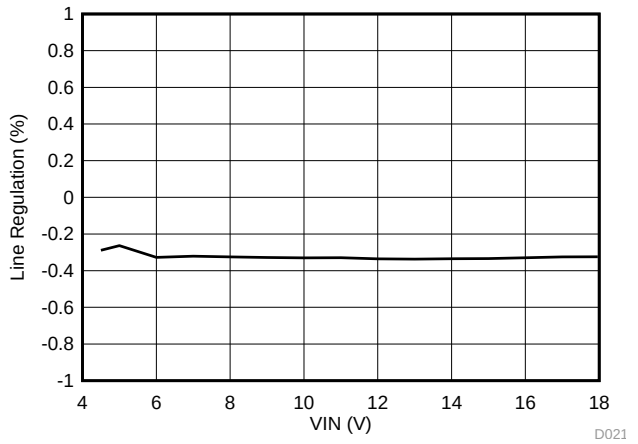


Figure 25. Line Regulation, I_{OUT} = 6 A

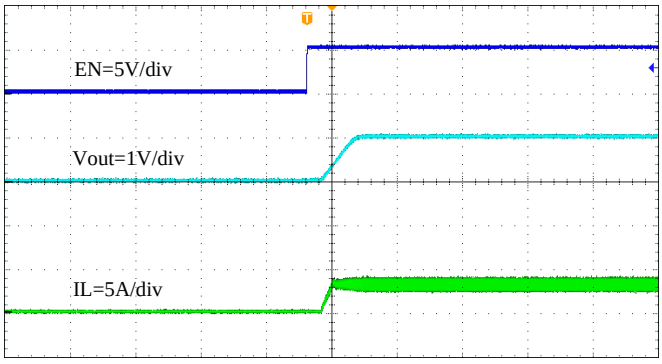


Figure 26. Start-Up Through EN, I_{OUT} = 3 A

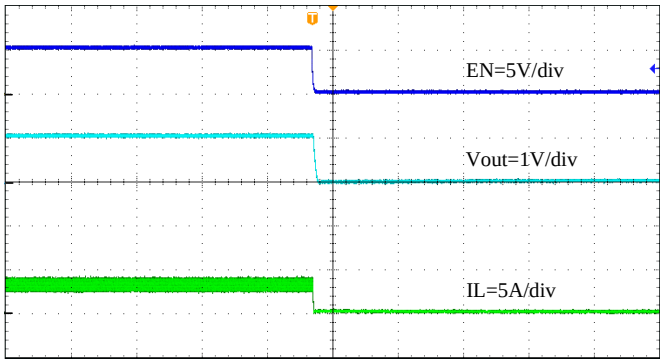


Figure 27. Shut-down Through EN, I_{OUT} = 3 A

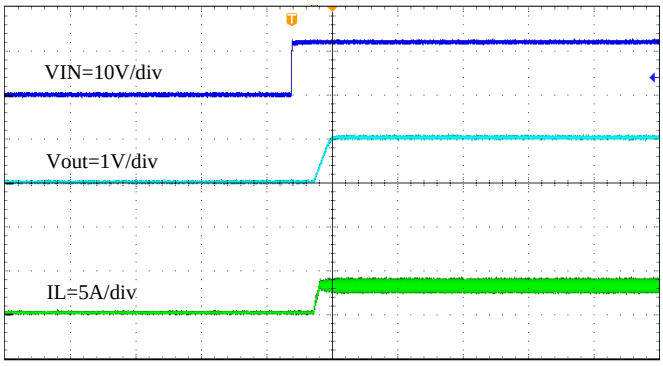


Figure 28. Start Up Relative to V_{IN} Rising, I_{OUT} = 3 A

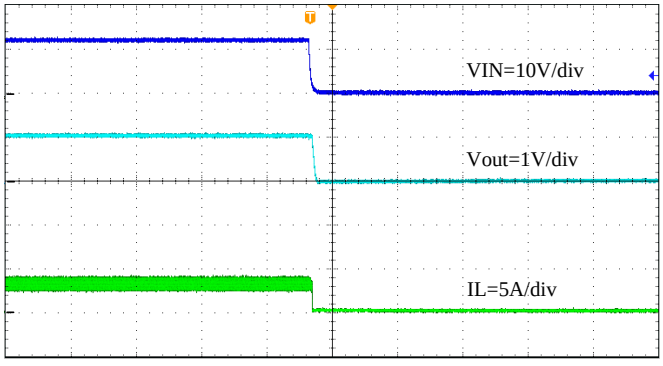


Figure 29. Start Up Relative to V_{IN} Falling, I_{OUT} = 3 A

ADVANCE INFORMATION

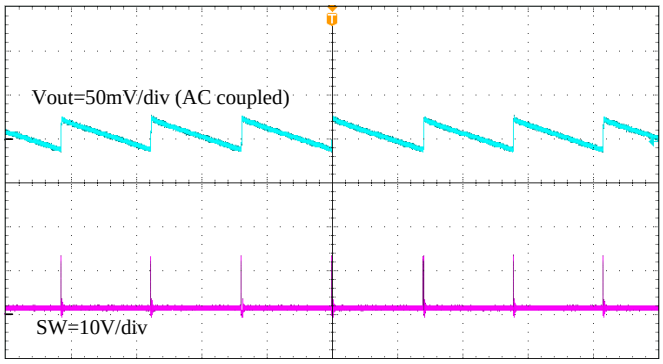


Figure 30. Output Voltage Ripple, I_{OUT} = 0.01 A

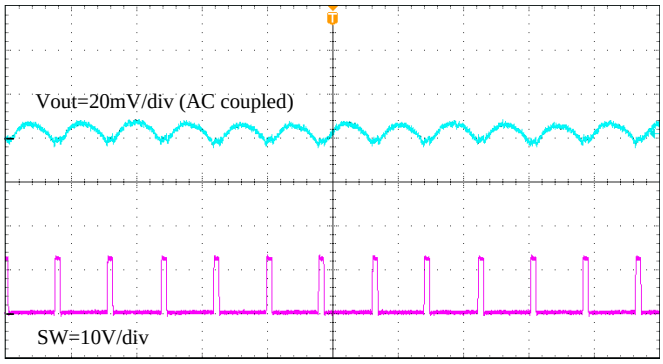


Figure 31. Output Voltage Ripple, I_{OUT} = 6 A

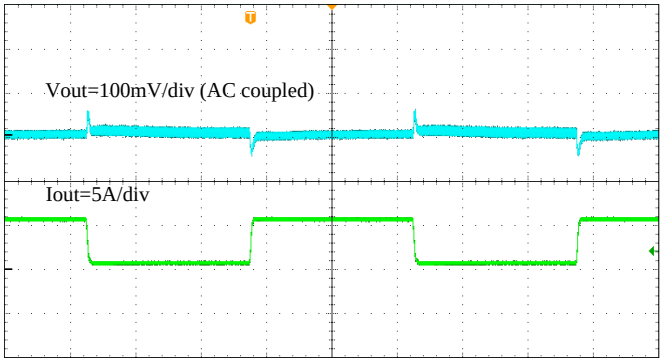


Figure 32. Transient Response, 0.6 A to 5.4 A

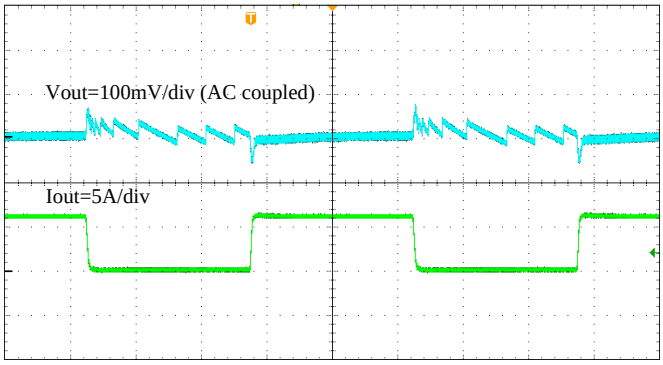


Figure 33. Transient Response, 0 A to 6 A

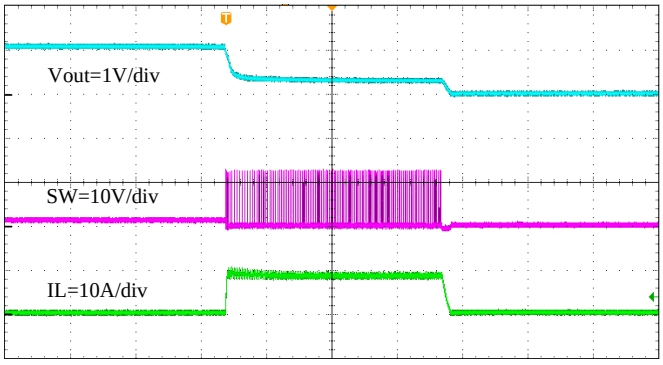


Figure 34. Normal Operation to Output Hard Short

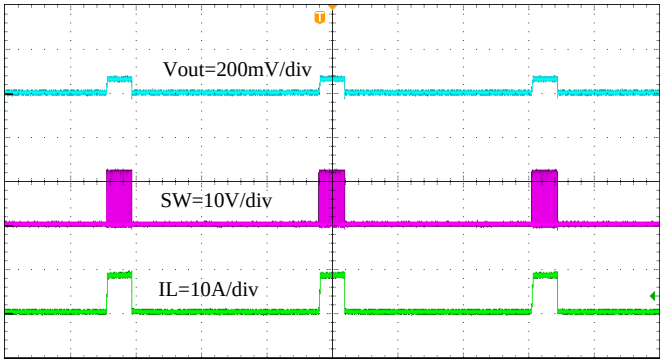


Figure 35. Output Hard Short Hiccup

ADVANCE INFORMATION

14 Power Supply Recommendations

The TPS566235 is intended to be powered by a well regulated dc voltage. The input voltage range is 4.5 V to 18 V. TPS566235 is BUCK converter, the input supply voltage must be bigger than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS566235 circuit, some additional input bulk capacitance is recommended. Typical values are 100 µF to 470 µF.

15 Layout

15.1 Layout Guidelines

When laying out the printed circuit board, the following guideline should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 36

- Recommend a four-layer PCB for good thermal performance and with maximum ground plane. 3" x 3", four-layer PCB with 2-oz. copper used as example.
- Place the decoupling capacitors right across VIN as close as possible.
- Place output inductors and capacitors with IC at the same layer, SW routing should be as short as possible to minimize EMI, and should be a wide plane to carry big current, enough vias should be added to the PGND connection of output capacitor and also as close to the output pin as possible.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane, >15 mil width trace is recommended to reduce line parasitic inductance.
- FB could be wide and must be routed away from the switching node, BST node or other high efficiency signal.
- VIN trace must be wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias near GND and near input capacitors to reduce parasitic inductance and improve thermal performance.

15.2 Layout Example

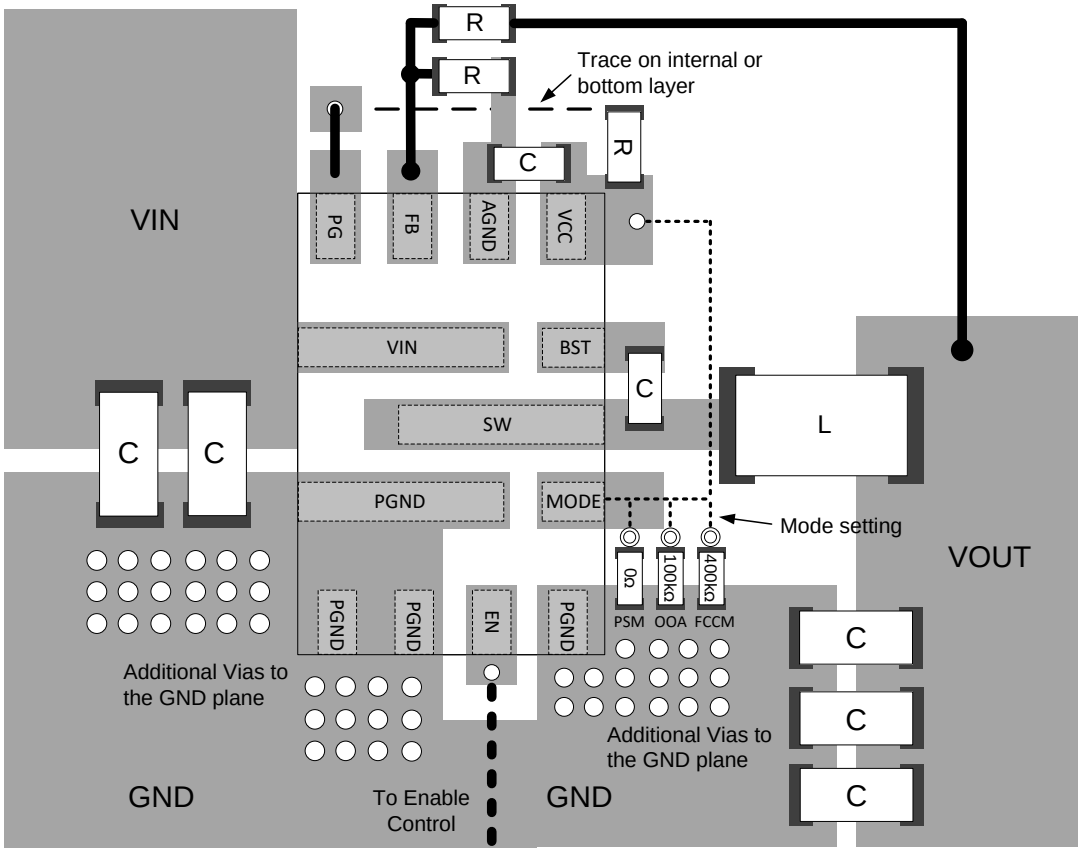


Figure 36. PCB Layout Recommendation Diagram

ADVANCE INFORMATION

16 Device and Documentation Support

16.1 Device Support

16.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

16.1.2 Development Support

16.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS566235 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

16.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

16.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

16.4 Trademarks

D-CAP3, Eco-Mode, Out-Of-Audio, HotRod, Advanced Eco-Mode, E2E are trademarks of Texas Instruments. WEBENCH is a registered trademark of Texas Instruments.

16.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ADVANCE INFORMATION

16.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

17 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS566235RJNR	PREVIEW	VQFN-HR	RJN	13	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	566235	
TPS566235RJNT	PREVIEW	VQFN-HR	RJN	13	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	566235	
XTPS566235RJNR	ACTIVE	VQFN-HR	RJN	13	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

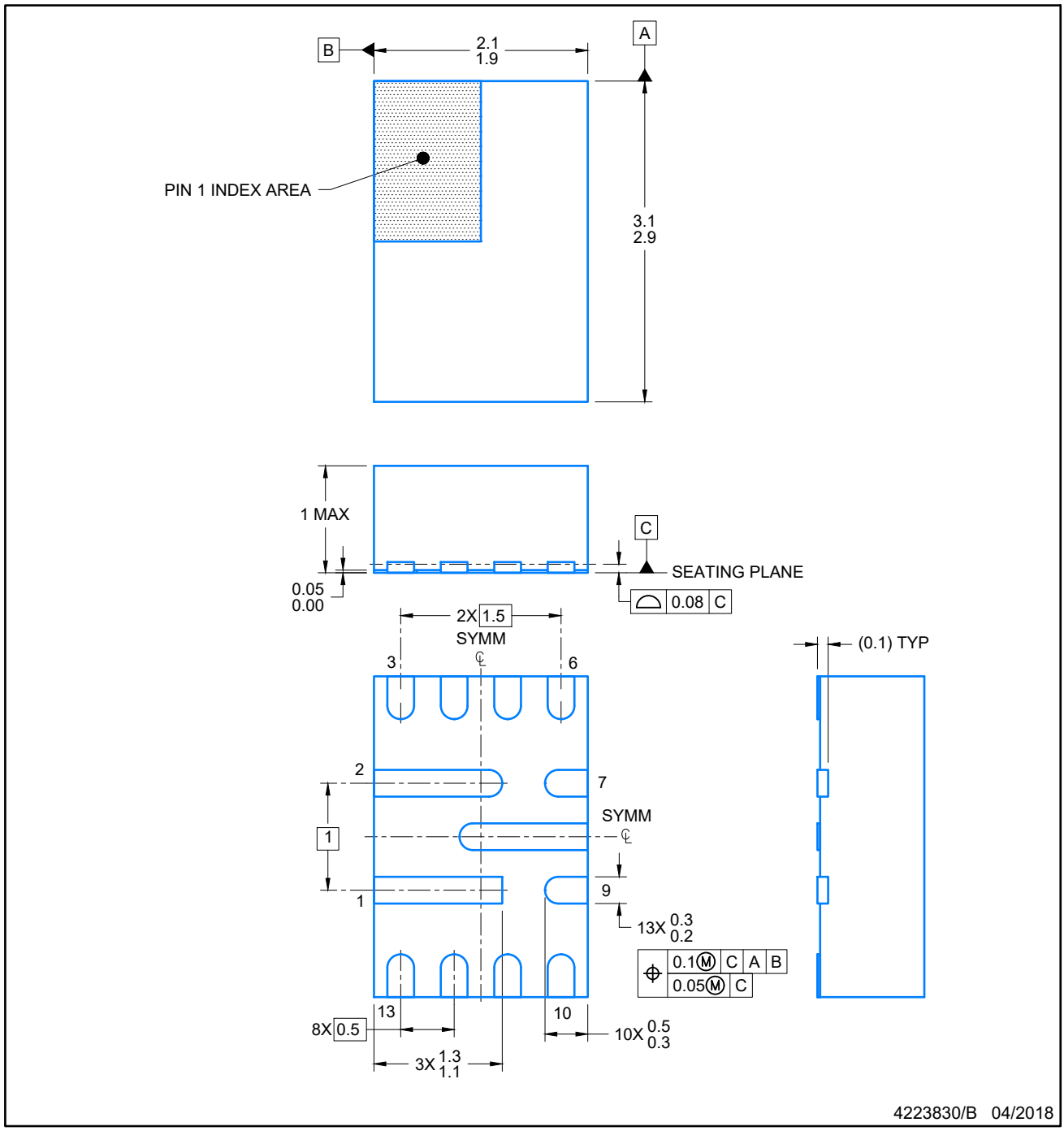
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RJN0013A

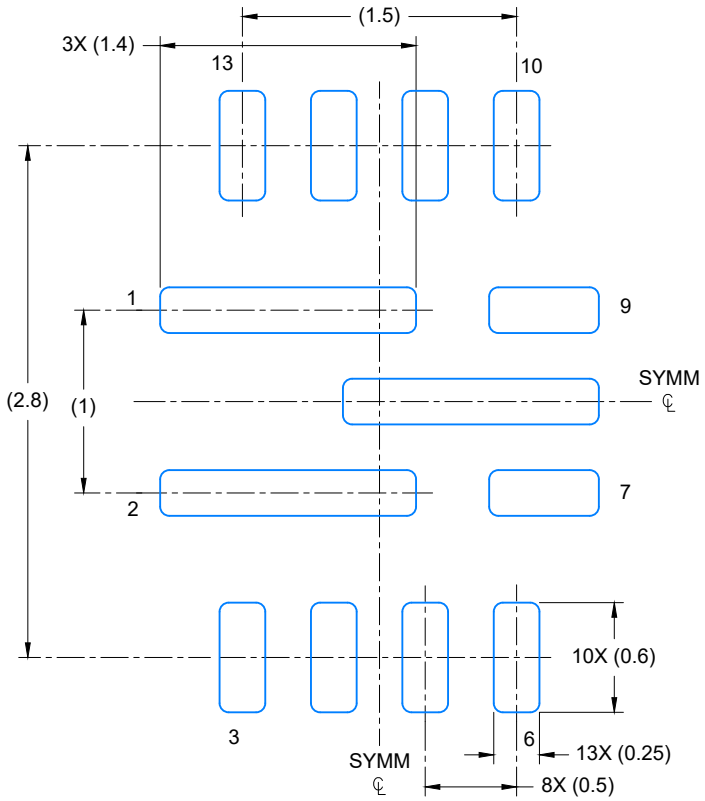
VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE- NO LEAD

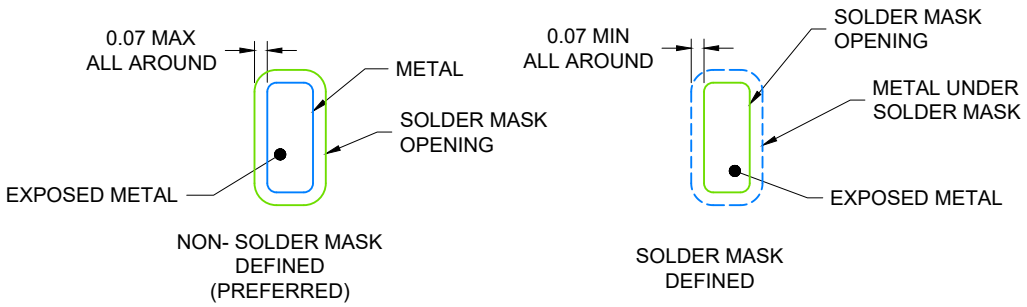


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

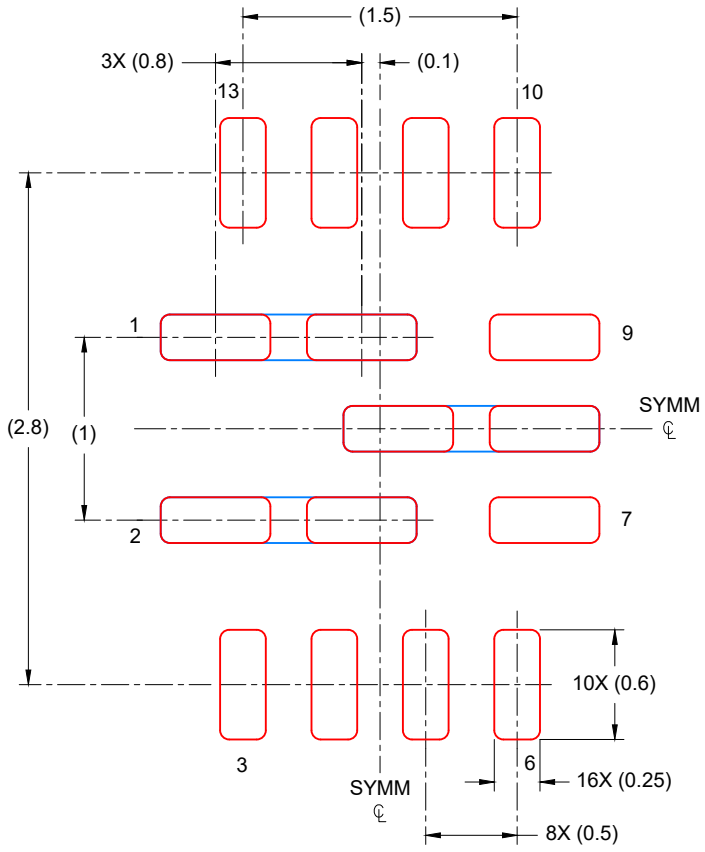


SOLDER MASK DETAILS

4223830/B 04/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
86% PRINTED COVERAGE BY AREA
SCALE: 25X

4223830/B 04/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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