HDMI 1.4b 1:2 Splitter/Demux for 3.4Gbps Data Rate with Equalization & Pre-emphasis

Features

- **Support up to 3.4Gbps TMDS Serial Link Compliant with HDMI 1.4b requirement**
- **HDMI 1-to-2 Splitter or 1-to-2 DeMux with Equalization & Pre-emphasis up to 340 MHz Clock**
- **AC or DC Coupled Differential Signaling Input**
- **Configurable TMDS Output Signal with Port Selection, Pre-emphasis, Voltage Swing, Slew Rate Control**
- **Support Squelch Mode with Built-in Clock detector**
- **Control Status Register controlled by Pin strap or I^2C mode programming**
- **ESD Protection on I/O pins to connector: 8KV Contact per IEC6100-4-2 and 2KV HBM**
- **Supply Voltage: 3.3V**
- **Industrial Temperature Range: -40°C to 85°C**
- **Packaging (Pb-free & Green): 56-contact TQFN (ZB56)**

General Description

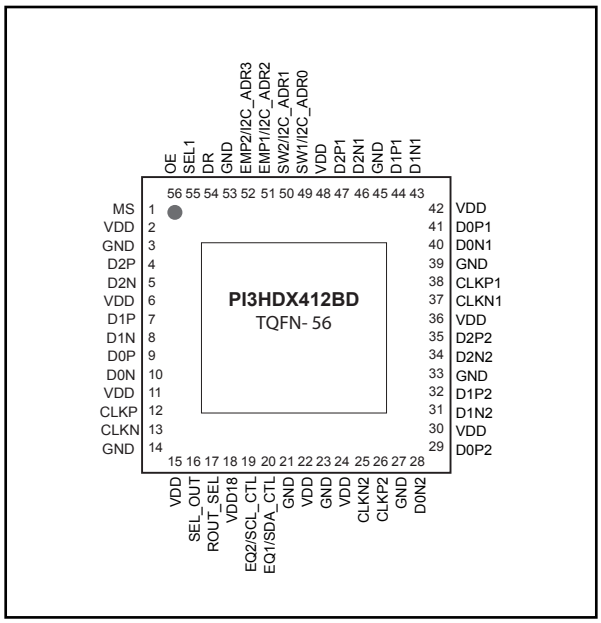
Pericom Semiconductor's PI3HDX412BD, active-drive switch solution is targeted for high-resolution video networks that are based on HDMI™/DVI standards, and TMDS signal processing.

The PI3HDX412BD is an active single TMDS channel to two TMDS channel Splitter and DeMux with Hi-Z outputs. The device drives differential signals to multiple video display units.

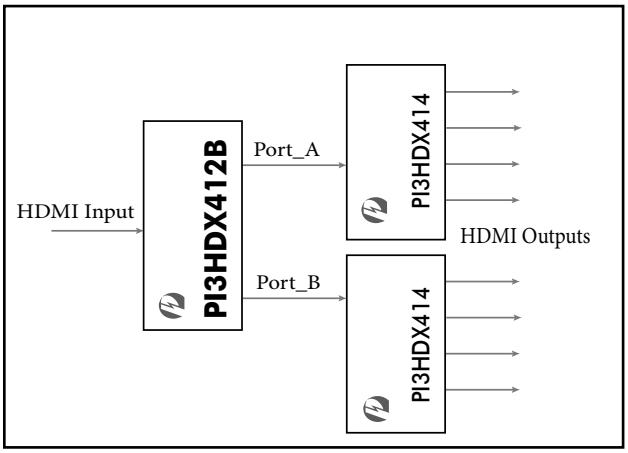
It provides controllable output swing levels that can be controlled through pin control or I2C control, depending on the mode select pin. This solution also provides a unique advanced pre-emphasis technique to increase rise and fall times.

The maximum HDMI™/DVI data rate of 3.4Gbps provides a 1920x1080 @60Hz resolution or 4K @30Hz required for 4K HDTV and PC graphics products. Due to its active unidirectional feature, this switch is designed for usage only for the video driver's side. For PC graphics application, the device sits at the driver's side to switch between multiple display units, such as PC LCD monitor, projector, TV, etc.

PI3HDX412BD ensures transmitting high bandwidth video streams from PC graphics source to end display units. It will also provide enhanced robust ESD/EOS protection, which is required by many consumer video networks today.



PI3HDX412BD Package & Pinout



Application Block Diagram

TMDS In/Out Pin Assignment

Pin #	Pin Name	Type	Description
4	D2P	I	Input Port. TMDS Clock and Data Input pins. When Input Termination Resistor (Rt = 50 Ohm) tied to VDD or GND, Rpd=200 kOhm shall be "OFF" state. I2C registers can control Rt and Rpd ON/OFF state.
5	D2N	I	
7	D1P	I	
8	D1N	I	
9	D0P	I	
10	D0N	I	
12	CLKP	I	
13	CLKN	I	
25	CLKN2	O	Output Port 1. TMDS Clock and Data Output pins. ROUT_SEL pin enables Output Termination Resistor (Rout=50 Ohm).
26	CLKP2	O	
28	D0N2	O	
29	D0P2	O	
31	D1N2	O	
32	D1P2	O	
34	D2N2	O	
35	D2P2	O	
37	CLKN1	O	Output Port 2. TMDS Clock and Data Output pins. ROUT_SEL pin enables Output Termination Resistor (Rout=50 Ohm).
38	CLKP1	O	
40	D0N1	O	
41	D0P1	O	
43	D1N1	O	
44	D1P1	O	
46	D2N1	O	
47	D2P1	O	

Note: In TMDS Data and Clock Differential Pair, the polarity +/- (or P/N) of each pair can use interchangeably. When input TMDS Input Clock polarity +/- pin swaps, output TMDS Clock of port 1 and port 2 shall swapped accordingly.

Control Pins

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>MS</td><td>I</td><td>Mode Selection Pin. Internal pull-up at 100K Ohm.

"High" : I²C Control Mode Selection
"Low" : Pin Control Mode Selection</td></tr>
<tr><td>19
20</td><td>EQ2/SCL_CTL
EQ1/SDA_CTL</td><td>IO</td><td>Shared Pin. EQ2 pin or I²C Clock pin. I²C pin is compatible with standard I²C-Bus specification, up to 400 Kbps.

Pin#1 MS sets "High" : Pin#19 assigns to SCL_CTL pin
Pin#1 MS sets "Low" : Pin#19 assigns to EQ2 pin

Internally Pull-Up at 100 Kohm and Pull-Down at 100 Kohm.

Pin Control EQ setting table is shown below. "M" is Tri-state.
<table>
<tr><th></th><th>EQ2
(Pin# 19)</th><th>EQ1
(Pin# 20)</th><th>Equalization Setting
(dB)</th></tr>
<tr><td rowspan="9">Pin#1 MS =
"Low"</td><td>0</td><td>M</td><td>2.5</td></tr>
<tr><td>0</td><td>0</td><td>5</td></tr>
<tr><td>M</td><td>0</td><td>7.5</td></tr>
<tr><td>0</td><td>1</td><td>10</td></tr>
<tr><td>M</td><td>M</td><td>12.5</td></tr>
<tr><td>1</td><td>0</td><td>15</td></tr>
<tr><td>1</td><td>M</td><td>17.5</td></tr>
<tr><td>1</td><td>1</td><td>20</td></tr>
</table></td></tr>
<tr><td>49
50
51
52</td><td>SW1/I2C_ADR0
SW2/I2C_ADR1
EMP1/I2C_ADR2
EMP2/I2C_ADR3</td><td>I</td><td>Shared Pin. SW or EMP or I2C_ADR pins.

When Pin#1 MS="High" : These Shared Pins assign to I2C_ADR[3:0]
When Pin#1 MS="Low" : These Shared Pins assign to SW1/2 and EMP1/2

These SW2 and SW1 pins control output voltage swing adjustment as following table. These SW pins have internal Pull-Up 100K Ohm.
<table>
<tr><th>SW2 (Pin#50)</th><th>SW1 (Pin#49)</th><th>Output Voltage Swing</th></tr>
<tr><td>0</td><td>0</td><td>500 mV</td></tr>
<tr><td>0</td><td>1</td><td>-10 %</td></tr>
<tr><td>1</td><td>0</td><td>+10 %</td></tr>
<tr><td>1</td><td>1</td><td>+20 %</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>49
50
51
52</td><td>(Continued)</td><td>I</td><td>EMP2 and EMP1 pins control output voltage pre-emphasis. These pins have internally Pull-Up 100 Kohm.
<table><tr><th>EMP2 (Pin#52)</th><th>EMP1 (Pin#51)</th><th>Pre-emphasis Setting (dB)</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1.5</td></tr><tr><td>1</td><td>0</td><td>2.5</td></tr><tr><td>1</td><td>1</td><td>3.5</td></tr></table></td></tr>
<tr><td>56</td><td>OE</td><td>I</td><td>Output Enable Control pin. Internally pull-up at 100 Kohm.

"High" : Output Port Enable
"Low" : Turn off Rout and Rt(termination resistor). TMDS Receiver and TMDS Output Drivers are "OFF" state.</td></tr>
<tr><td>54</td><td>DR</td><td>I</td><td>Direction Control pin

"High" : All ports are Active at same time
"Low" : Output Ports are controlled by SEL1 (Pin#55) control</td></tr>
<tr><td>55</td><td>SEL1</td><td>I</td><td>Port 1 or Port 2 Output Enable Selection pin. Internal pull-up at 100 Kohm.

"High" : Enable Output Port 2
"Low" : Enable Output Port 1</td></tr>
<tr><td>16</td><td>SEL_OUT</td><td>O</td><td>SEL_OUT pin. I^2C Register Offset 0x00 Bit[5] can control this pin status.

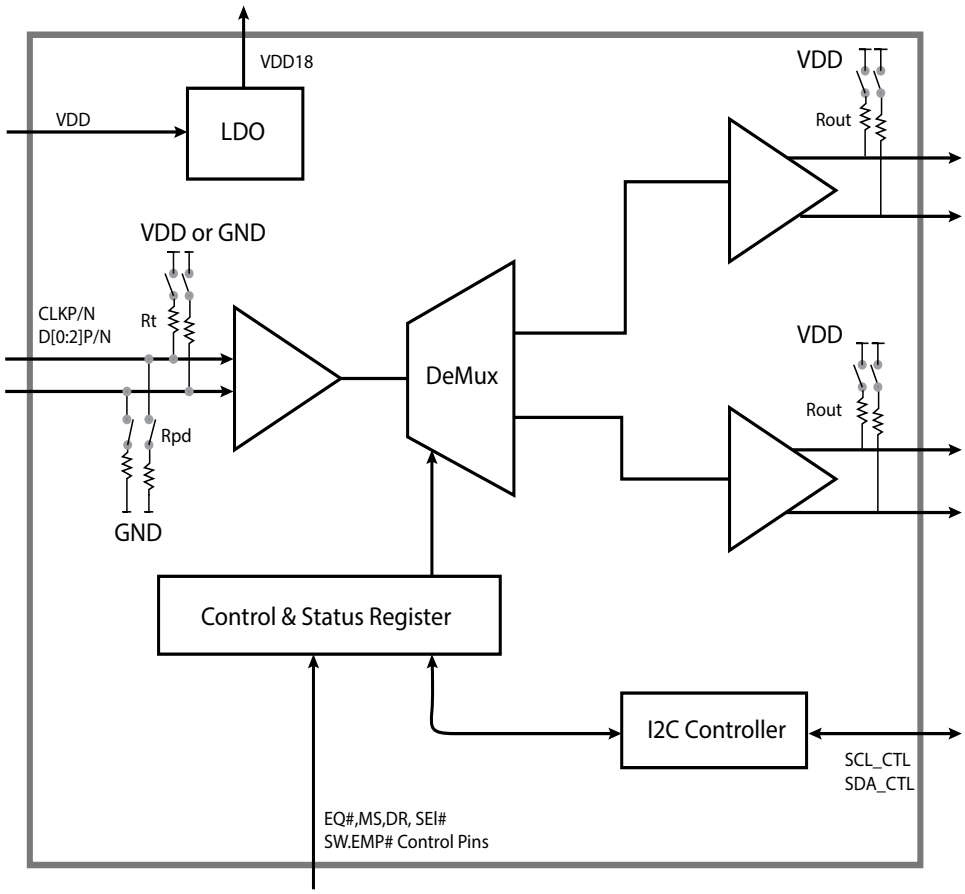
Offset 0x00 Bit[5] ="1" : Enable Output Port 1 Output
Offset 0x00 Bit[5] ="0" : Disable Output Port 1 Output</td></tr>
<tr><td>17</td><td>ROUT_SEL</td><td>I</td><td>Source termination selection pin. Internal pull-up at 100K Ohm.

"High" : Source Termination Output (Rout) Resistor is "ON", connect to VDD in Output Driver
"Low" : Source Termination Output (Rout) Resistor is "OFF". Open-Drain Output Driver is open drain</td></tr>
</table>

Power/Ground Pins

Pin #	Pin Name	Type	Description
18	VDD18	Power	LDO Output Pin for internal core supplier. Add external 4.7 uF capacitor to GND
3,14,21,23,27,33,39,45,53	GND	Ground	Ground Pins
2,6,11,15,24,30,36,42,48	VDD	Power	3.3V Power Supply

Block Diagram



Functional Description

Squelch Mode:

Output Disable (Squelch) Mode uses TMDS Clock channel signal detection. When low voltage levels on the TMDS input clock signals are detected, Squelch state enables and TMDS output port signals shall disable; when the TMDS clock input signal levels are above a pre-determined threshold voltage, output ports shall return to the normal voltage swing levels.

When enable Squelch mode, input termination resistor will be enabled together. When Squelch is disabled through I2C register programming RX_SET[1]="1" and no TMDS input signal condition, TMDS D[0:2]P/N will be undetermined status. In Squelch state, TMDS output is high impedance state or TMDS output port shall 50 Ohm pull-up at source termination output.

Function Control Table

OE	MS	DR	SEL1	HDMI Outputs
0	x	x	x	All Port Disable
Pin Cotrol Mode				
1	0	1	x	All Ports Enable
1	0	0	0	Enable Port 1
1	0	0	1	Enable Port 2
I2C Control Mode				
1	1	x	x	I2C Programming Mode

I²C Register Control Programming

I²C Register Control

Pin Name	I/O	Description
SCL_CTL	I	I2C Clock, compatible with I2C-bus specification, up to 400 kb/s
SDA_CTL	IO	I2C Data, compatible with I2C-bus specification, up to 400 kb/s
I2C_ADR[3:0]	I	I2C Control Address Setting
Byte output : 0x00 - 0x07	O	I2C Control registers output

I²C Address Byte

	b[7] MSB	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (R/W)
Address Byte	1	0	1	A3	A2	A1	A0	1/0*

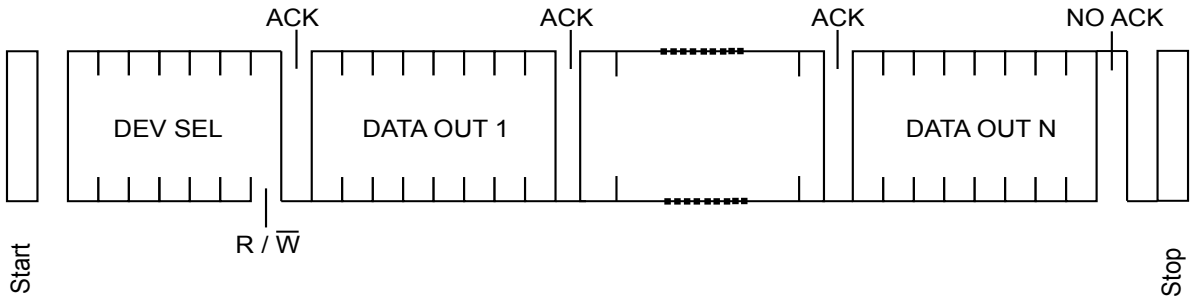
Note: Read "1", Write "0"

<table>
<tr><th>Offset</th><th>Name</th><th>Description</th><th>Power Up Condition</th><th>Type</th></tr>
<tr><td>0x00</td><td>CONFIG[7:0]</td><td>[7] Enable TMDS Standby mode.
In standby mode, TMDS equalizer and output driver shall power down.
"0": Standby mode
"1": Normal mode
[6] Reserved
[5] Output TMDS Port 1 Select
"0": Disable
"1": Enable
[4] Output TMDS Port 2 Selected
"0": Disable
"1": Enable
[3] Reserved
[2:0] Reserved</td><td>0xFF</td><td>R/W</td></tr>
<tr><td>0x01</td><td>RX_SET[7:0]</td><td>TMDS Receiver Equalization Setting Registers
[7] Disable Input Port input termination resistors
"0" : Enable Rpd connection
"1" : Disable Rpd connection
[6] TMDS Input termination V-bias selection
"0": Connect to GND
"1": Connect to VDD
[5] V-bias register selection enable
"0": bit[6] control disable
"1": bit[6] control enable
[4:2] EQ programmable setting
<table>
<tr><th>b[4:2]</th><th>EQ Setting (dB)</th></tr>
<tr><td>000</td><td>2.5</td></tr>
<tr><td>001</td><td>5</td></tr>
<tr><td>010</td><td>7.5</td></tr>
<tr><td>011</td><td>10</td></tr>
<tr><td>100</td><td>12.5</td></tr>
<tr><td>101</td><td>15</td></tr>
<tr><td>110</td><td>17.5</td></tr>
<tr><td>111</td><td>20</td></tr>
</table>
[1] Squelch Control Bit
"0": Squelch enable
"1": Squelch disable
[0] Reserved</td><td>0x00</td><td>R/W</td></tr>
<tr><td>0x02</td><td>Reserved</td><td>[7:0] Reserved</td><td>0x00</td><td>R/W</td></tr>
</table>

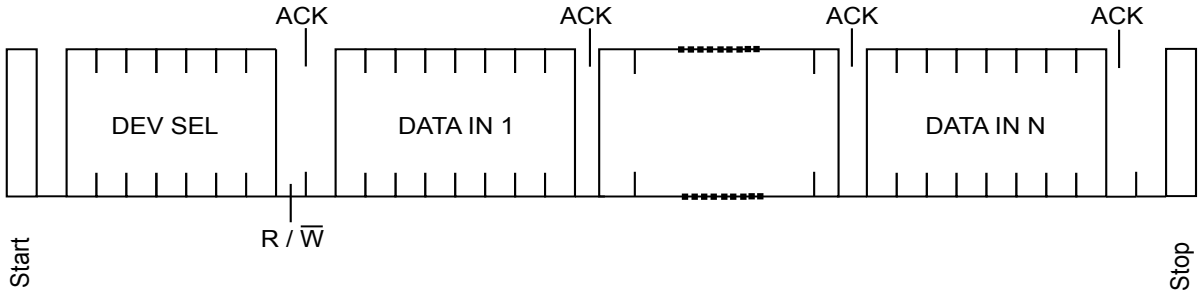
Offset	Name	Description	Power Up Condition	Type
0x03	TX_SET[7:0] for port1	TMDS Port 1 Output setting [7] TMDS output control "0": Open drain "1": Double termination [6:4] TMDS output Pre-emphasis control "000": 0 dB "001": 1.5 dB "010": 2.5 dB "011": 3.5 dB "1xx": 6 dB (750 mVpp swing) [3:2] TMDS output swing setting "00": 500 mV as default "01": -10% "10": +10% "11": +20% [1:0] TMDS output slew rate setting "00": as default "01" / "10": + 5% "11": +10%	0x00	R/W
0x04	TX_SET[7:0] for port2	TMDS Port 2 Output setting [7] TMDS output control "0": Open drain "1": Double termination [6:4] TMDS output Pre-emphasis control "000" : 0 dB "001" : 1.5 dB "010" : 2.5 dB "011" : 3.5 dB "1xx" : 6 dB (750 mVpp swing) [3:2] TMDS output swing setting "00" : 500 mV as default setting "01" : -10% "10" : +10% "11" : +20% [1:0] TMDS output slew rate setting "00" : Default setting "01" / "10" : + 5% "11" : +10%	0x00	R/W
0x05	Reserved	[7:0] Reserved	0x00	R/W
0x06	Reserved	[7:0] Reserved	0x0F	R/W
0x07	Reserved	[7:0] Reserved	0x00	R/W

I²C Data Transfer

1. Read Sequence



2. Write Sequence



Absolute Maximum Ratings

Supply Voltage to Ground Potential 4.5V
DC SIG Voltage . . . . . –0.5V to V_{DD}+0.5V
Storage Temperature. . . . . –65°C to +150°C
Operating Temperature . . . . . -40 to +85°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Thermal Characteristics

Symbol	Parameter	Ratings	Units
T_{Jmax}	Junction Temperature	125	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	24	

Electrical Characteristics T_J=25 °C unless otherwise noted

DC Specifications VDD=3.3V +/- 10%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DD}	Operation Voltage		3.0	3.3	3.6	V
I_{DD}	VDD Supply Current			250	290	mA
I_{DDQ}	VDD Quiescent Current	OE = 1, No input signal		50	80	mA
I_{STB}	Standby mode	OE = 0		1	5	mA
TMDS Differential Pins						
V_{OH}	Single-ended high level output voltage	VDD = 3.3 V, Rout=50 Ω	VDD-10		VDD+10	mV
VOL	Single-ended low level output voltage		VDD-600		VDD–400	mV
Vswing	Single-ended output swing voltage		400		600	mV
VOD(O)	Overshoot of output differential voltage				180	mV
VOD(U)	Undershoot of output differential voltage				200	mV
VOC(SS)	Change in steady-state common- mode output voltage between logic states				5	mV
IOS	Short Circuit output current		-12		12	mA
IOS	Short Circuit output current at double termination mode		-24		24	mA

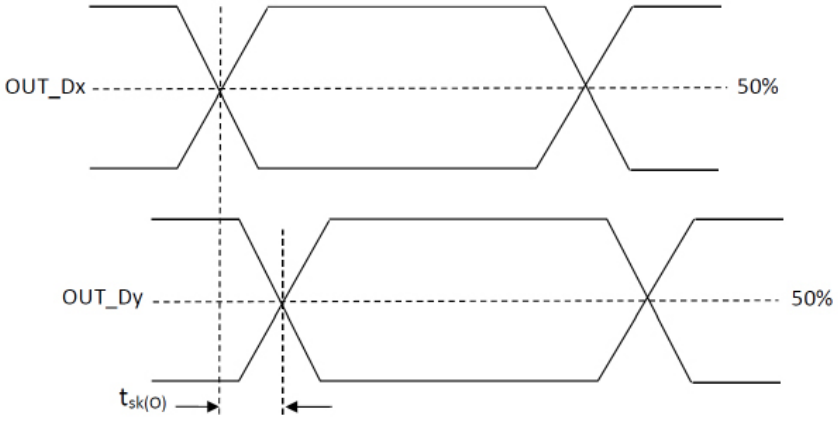
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VI(open)	Single-ended input voltage under high impedance input or open input	IL = 10 uA	VDD-10		VDD+10	mV
RT	Input termination resistance	VIN = 2.9 V	45	50	55	Ohm
IOZ	Leakage current with Hi-Z I/O	VDD = 3.6 V, OE = 0		30	100	µA
Control pins (OE, SEL1, EMP2, EMP1, SW2, SW1, MS)						
I_{IH}	High level digital input current	V_{IH} =V_{DD}	-10		10	µA
I_{IL}	Low level digital input current	V_{IL} = GND	-50		10	µA
V_{IH}	High level digital input voltage		2.4			V
V_{IL}	Low level digital input voltage		0		0.8	V

AC Specifications

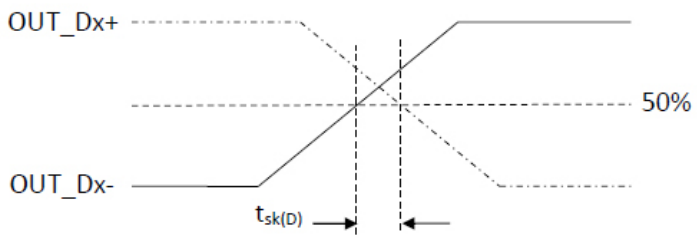
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
tpd	Propagation delay				2000	ps
t_r	Differential output signal rise time (20% - 80%), 0 dB / Open drain	VDD=3.3V, ROUT=50 ohm		117		ps
t_f	Differential output signal fall time (20% - 80%), 0 dB / Open drain			117		ps
$t_{sk(p)}$	Pulse skew			15	50	ps
$t_{sk(D)}$	Intra-pair differential skew			25	50	ps
$t_{sk(O)}$	Inter-pair differential skew				100	ps
t_{sx}	Select to switch output				550	ns
t_{en}	Enable time			1	10	us
t_{dis}	Disable time				50	ns
tjit_clk(pp)	Peak-to-peak output jitter CLK residual jitter	Data: 3.4 Gbps data pattern Clock: 340 MHz		10		ps
tjit_data(pp)	Peak-to-peak output jitter Date residual jitter			28		ps

Note:
1. Overshoot of output differential voltage $V_{OD(O)}$ = ($V_{SWING(MAX)}$ *2) * 15%
2. Undershoot of output differential voltage $V_{OD(O)}$ = ($V_{SWING(MIN)}$ *2) * 25%

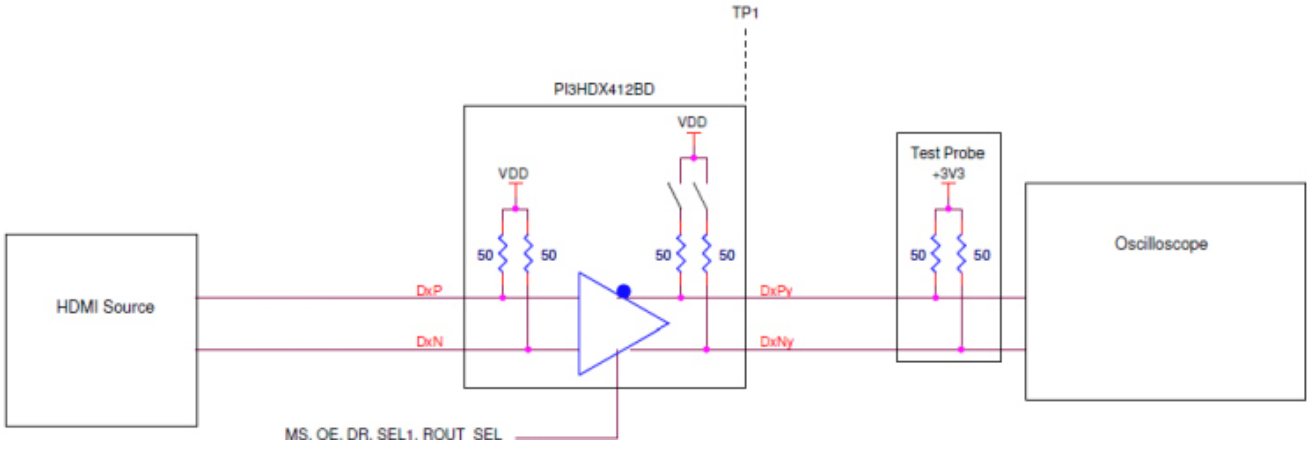
Inter-pair Skew Definition



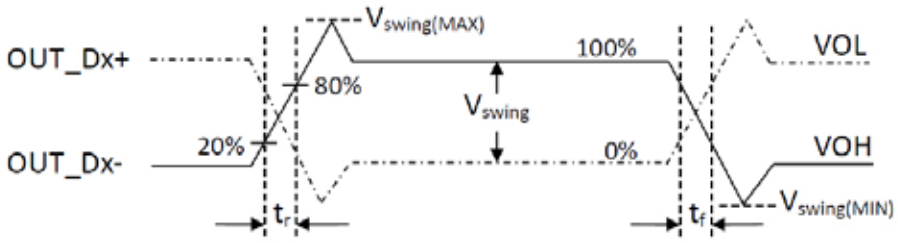
Intra-pair Skew Definition



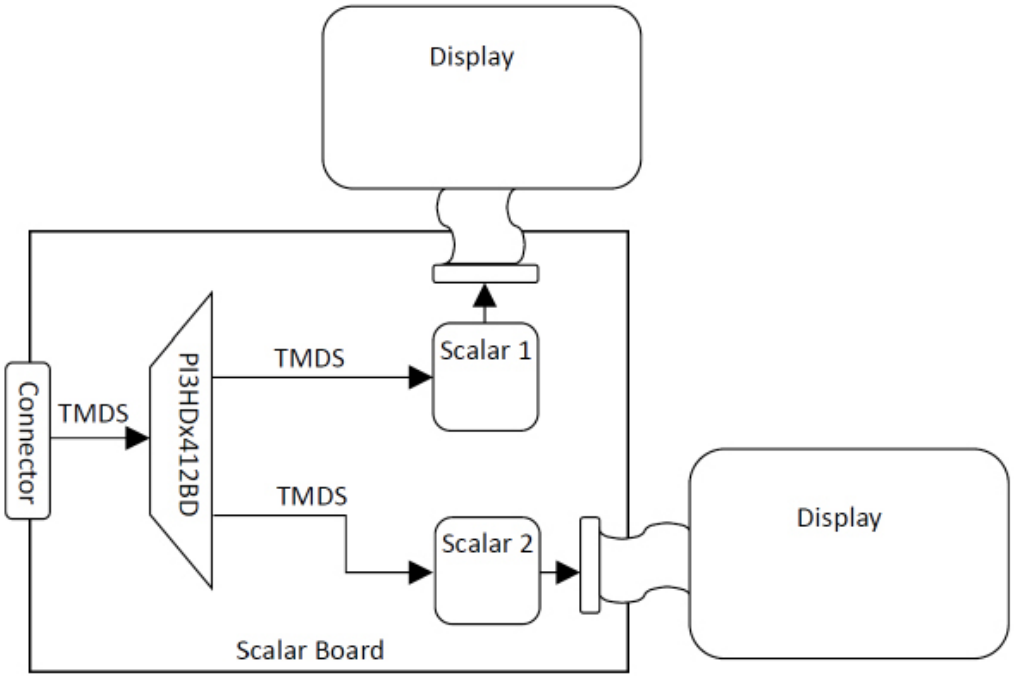
Test Setup of DC-coupled TMDS Input Measurement



Rise/Fall Time and Single-ended Swing Voltage

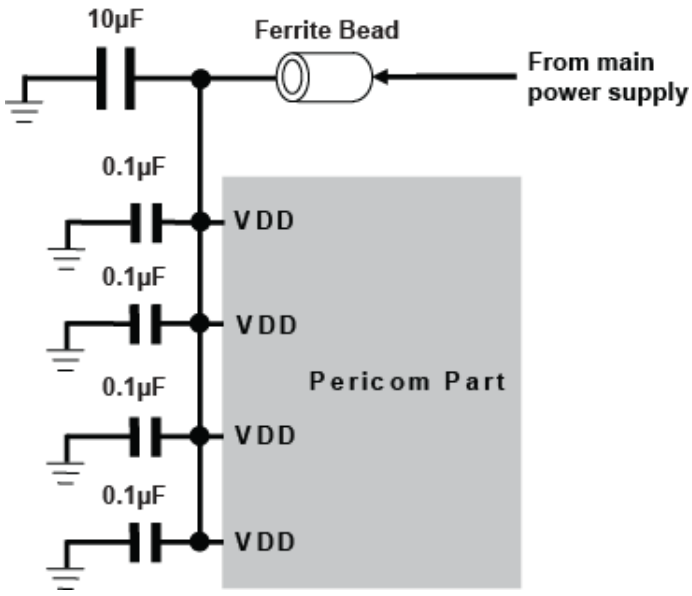


Typical Splitter Application



Power Supply Decoupling Circuit

It is recommended to put 0.1 µF decoupling capacitors on each VDD pins of our part, there are four 0.1 µF decoupling capacitors are put in Figure 1 with an assumption of only four VDD pins on our part, if there is more or less VDD pins on our Pericom parts, the number of 0.1 µF decoupling capacitors should be adjusted according to the actual number of VDD pins. On top of 0.1 µF decoupling capacitors on each VDD pins, it is recommended to put a 10 µF decoupling capacitor near our part's VDD, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.



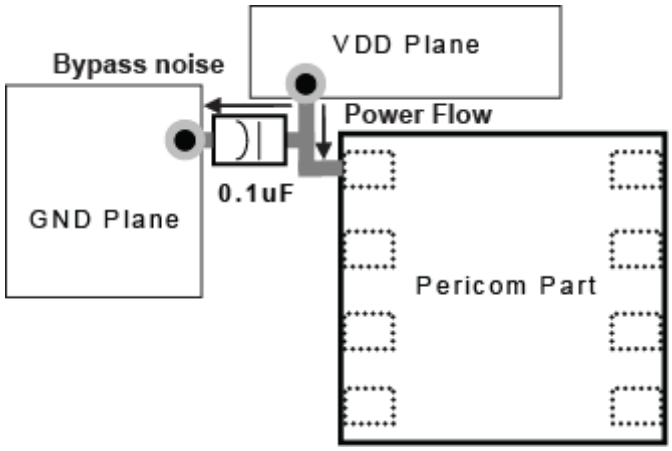
Recommended Power Supply Decoupling Capacitor Diagram

Requirements on the De-coupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

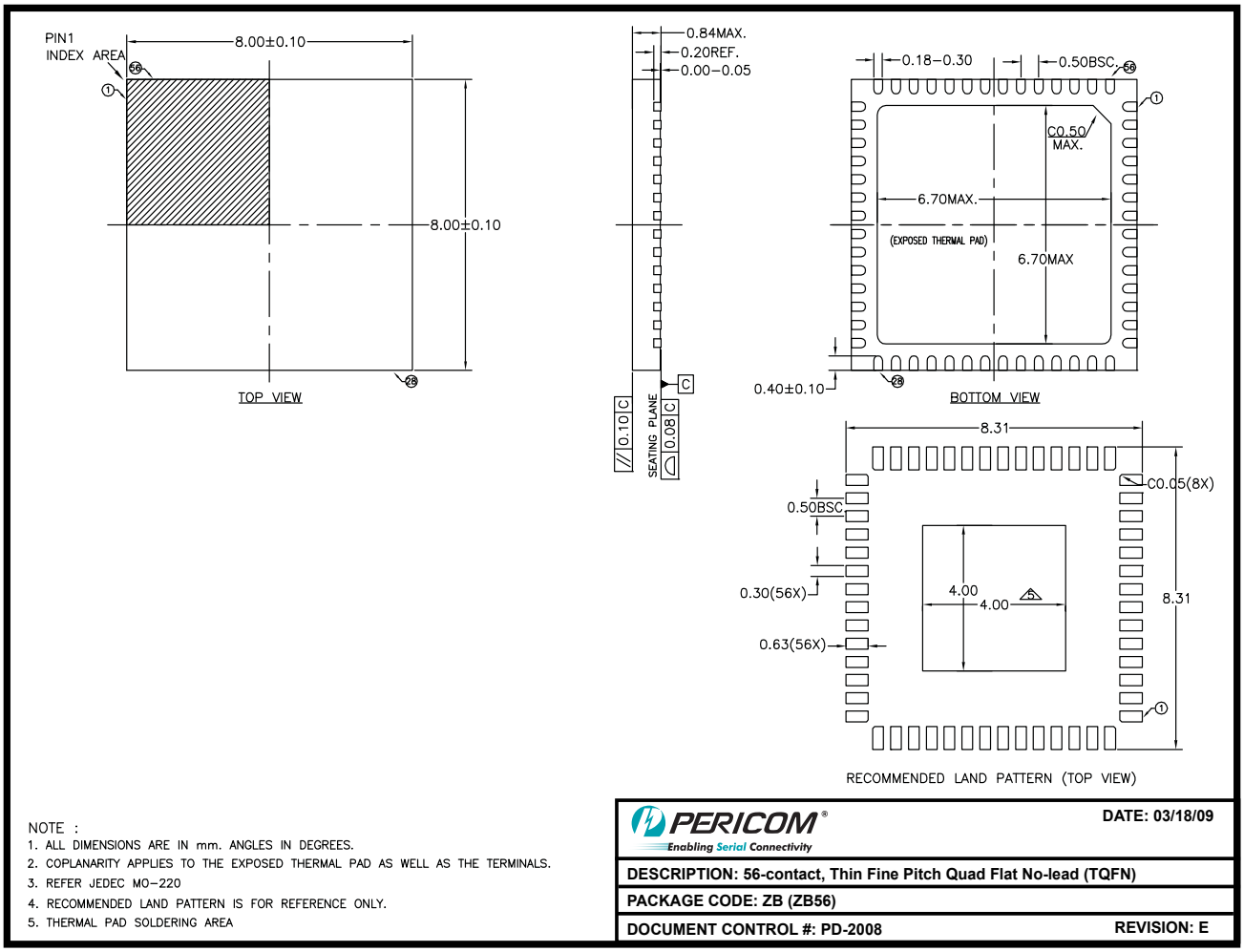
Layout and Decoupling Capacitor Placement Consideration

- Each 0.1 µF decoupling capacitor should be placed as close as possible to each VDD pin.
- VDD and GND planes should be used to provide a low impedance path for power and ground.
- Via holes should be placed to connect to VDD and GND planes directly.
- Trace should be as wide as possible
- Trace should be as short as possible.
- The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- 10 µF Capacitor should also be placed closed to our part and should be placed in the middle location of 0.1 µF capacitors.
- Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.



Decoupling Capacitor Placement Diagram

Package Mechanical: 56-pin TQFN (ZB56)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

PERICOM Enabling Serial Connectivity

DATE: 03/18/09

DESCRIPTION: 56-contact, Thin Fine Pitch Quad Flat No-lead (TQFN)

PACKAGE CODE: ZB (ZB56)

DOCUMENT CONTROL #: PD-2008 REVISION: E

Note:
For latest package info, please check: http://www.pericom.com/products/packaging

Ordering Information

Ordering Code	Package Code	Package Description
PI3HDX412BDZBE	ZB	56-pin, Pb-free & Green TQFN, Source Termination Type

Notes:
Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
PI3HDX412B : Root Part Number
-D/E : D= Source Termination TMDS Top Mount Type, E = Source Termination TMDS Bottom Mount Type
-ZB = 56-pin TQFN Package Type
-E = Pb-free and Green
Adding an -X Suffix = Tape/Reel Type

Related Products Information

Part Number	Product Description
PI3HDX414	HDMI 1.4b 3.4Gbps Splitter 1:4 with Signal Conditioning
PI3HDX1204	HDMI 2.0 Redriver for 6Gbps Application
PI3HDS20412	Wide Voltage Range DisplayPort & HDMI 2.0 Video Switch
PI3HDX511A	HDMI 1.4b 3.4Gbps Redriver and DP++ Level Shifter
PI3EQXDP1201	DisplayPort 1.2 Re-driver with Built-in AUX Listener
PI3VDP1430	Dual Mode DisplayPort to HDMI Level Shifter and Re-driver
PI3VDP3212	2-Lane DisplayPort1.2 Compliant Passive Switch
PI3VDP12412	4-Lane DisplayPort1.2 Compliant Passive Switch
PI3HDMI521	HDMI 1.4b 3.4Gbps 2:1 Switch/Re-driver with built-in ARC and Fast Switching support
PI3HDMI336	Active HDMI 3:1 Switch/Re-driver with I^2C control and ARC Transmitter

DISCLAIMER

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH PERICOM PRODUCT. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN PERICOM'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

Pericom may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Pericom reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specification. Current characterized errata are available on request.

Contact your local Pericom Sales office or your distributor to obtain the latest specifications and before placing your product order.

PRODUCT STATUS DEFINITIONS

Datasheet Identification	Product Status	Definition
Advanced Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Pericom Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Pericom Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Pericom Semiconductor. The datasheet is for reference information only.