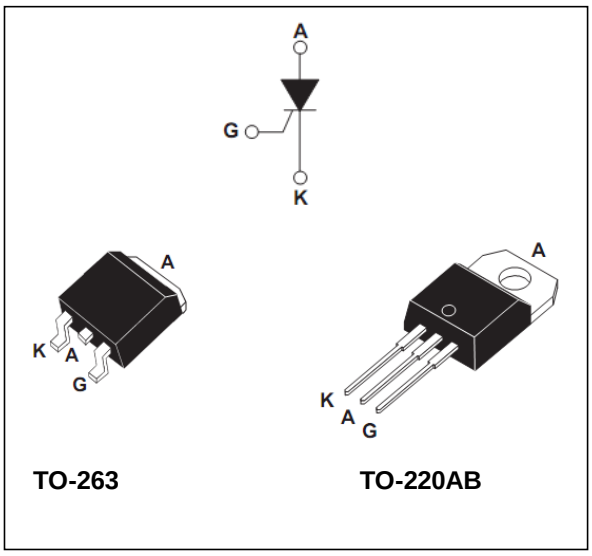
TYN625

25A SCR



Description

The TYN625 SCR Series is suitable for general purpose applications.

Using clip assembly technology, they provide a superior performance in surge current apabilities

Symbol	Value	Unit
$I_{T(RMS)}$	25	A
V_{DRM}/V_{RRM}	600 to 1000	V
I_{GT}	40	mA

Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)	T_c=100°C		25	A
$T_{(AV)}$	Average on-state current (180° conduction angle)	T_c=100°C		16	A
I_{TSM}	Non repetitive surge peak on-state current	t_p = 8.3 ms	T_j = 25°C	314	A
		t_p = 10 ms		300	A
I^2t	I^2t Value for fusing	t_p = 10 ms	T_j = 25°C	450	A^2s
dI/dt	Critical rate of rise of on-state current I_G=2 x I_{GT} , tr≤100 ns	F= 60 Hz	T_j = 125°C	50	$A/\mu s$
I_{GM}	Peak gate current	t_p =20 µs	T_j = 125°C	4	A
$P_{G(AV)}$	Average gate power dissipation	T_j = 125°C		1	W
T_{stg}	Storage junction temperature range			-40 to+150	°C
T_j	Operating junction temperature range			-40 to+125	
V_{RGM}	Maximum peak reverse gate voltage			5	V

Electrical Characteristics (Tj=25℃, unless otherwise specified)

Symbol	Test Conditions			Value	Unit
I_{GT}	V_D=12 V R_L=33 Ω		MIN.	4	mA
			MAX.	40	
V_{GT}			MAX.	1.3	V
V_{GD}	V_D=V_{DRM} R_L=3.3 kΩ	T_j=125°C	MIN.	0.2	V
I_H	I_T=500mA Gate open		MAX.	50	mA
I_L	I_G=1.2 I_{GT}		MAX.	90	mA
dV/dt	V_D=67 % V_{DRM} Gate open	Tj=125°C	MIN.	1000	V/µs
V_{TM}	I_{TM} =50A t_p =380 µs	Tj=25°C	MAX.	1.6	V
Vto	Threshold voltage	Tj=125°C	MAX.	0.77	V
R_d	Dynamic resistance	Tj=125°C	MAX.	14	mΩ
I_{DRM}	V_{DRM}=V_{RRM}	Tj=25°C	MAX.	5	µA
I_{RRM}		Tj=125°C		4	mA

Thermal resitances

Symbol	Conditions		Value	Unit
$R_{th(j-c)}$	Junction to case (DC)		1.0	°C /W
$R_{th(j-a)}$	Junction to ambient (DC)	TO-220AB	60	°C /W
		TO-263 S = 1 cm^2	45	

S = Copper surface under tab

Fig. 1: Maximum average power dissipation versus average on-state current.

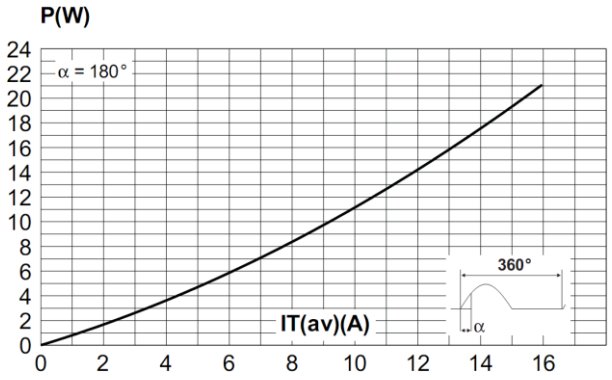


Fig. 2-1: Average and D.C. on-state current versus case temperature.

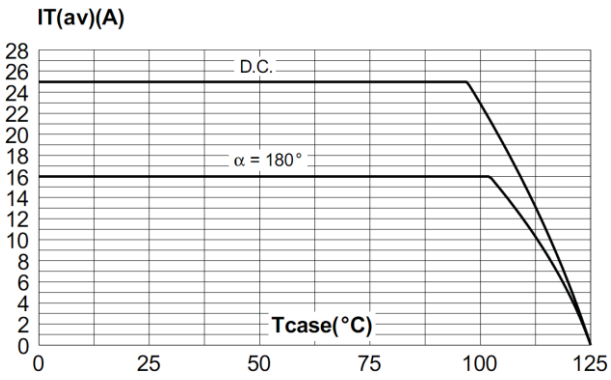


Fig. 2-2: Average and D.C. on-state current versus ambient temperature (copper surface under tab: S = 1cm2 (for D2PAK).

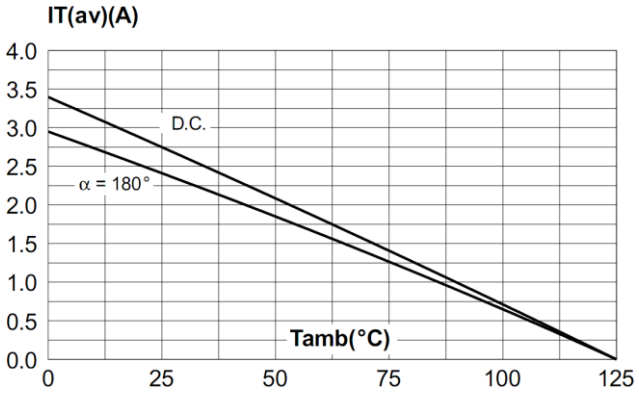


Fig. 3: Relative variation of thermal impedance versus pulse duration.

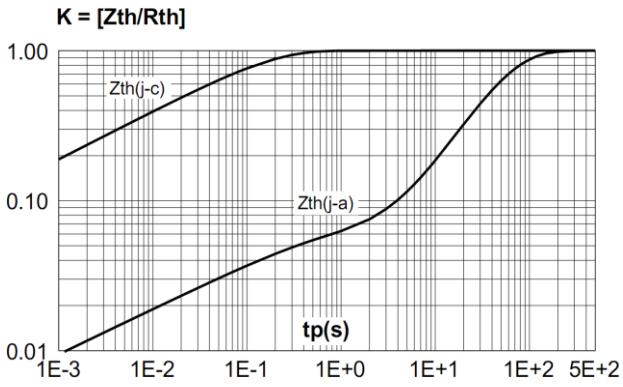


Fig. 4: Relative variation of gate trigger current, holding current and latching current versus junction temperature.

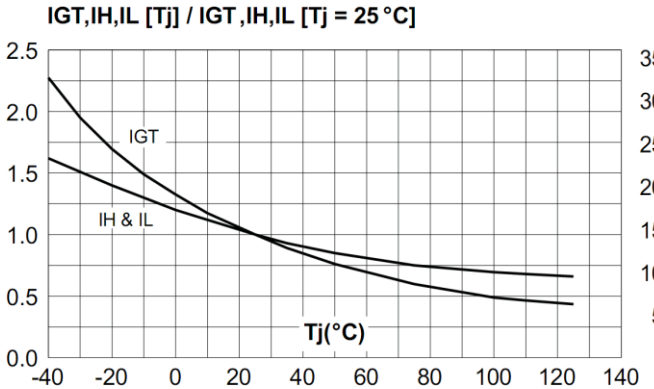


Fig. 5: Surge peak on-state current versus number of cycles.

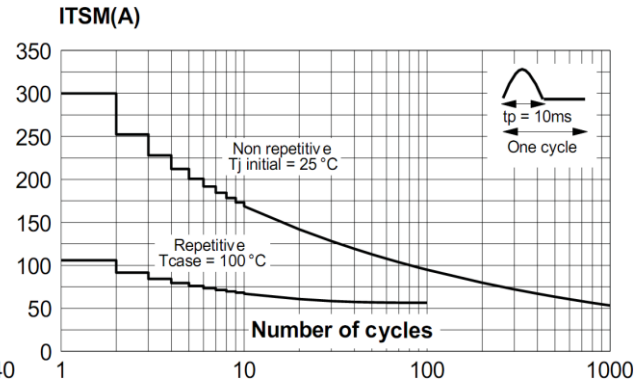


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp\<10ms, and corresponding values of I2t.

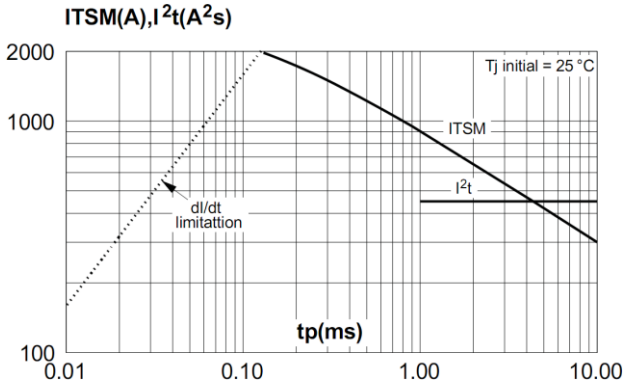


Fig. 7: On-state characteristics (maximum values).

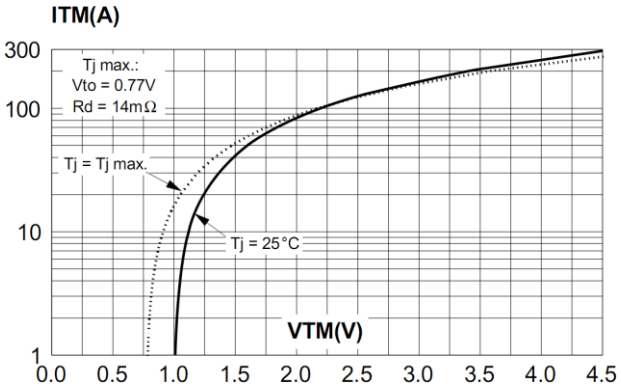


Fig. 8: Thermal resistance junction to ambient versus copper surface under tab (Epoxy printed circuit board FR4, copper thickness: 35µm)