



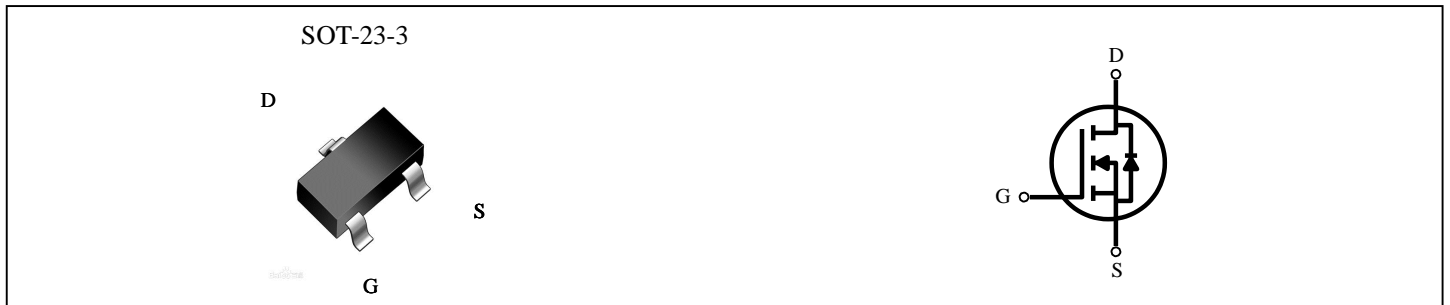
N-Channel High Density Trench MOSFET

PRODUCT SUMMARY

V _{DSS}	I _D	R _{DS(on)} (m-ohm) Max
20V	3.0	65 @ V _{GS} = 4.5V
	2.0	90 @ V _{GS} = 2.5V

FEATURES

- Super high dense cell trench design for low R_{DS(on)}.
- Rugged and reliable.
- Surface Mount package.



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±12	V
Drain Current-Continuous ^a @ T _A = 25 °C -Pulse ^b	I _D	3	A
	I _{DM}	9	A
Drain-Source Diode Forward Current ^a	I _S	1	A
Maximum Power Dissipation ^a	P _D	T _A =25 °C	1.25
		T _A =75 °C	0.75
Operating Junction and Storage Temperature Range	T _J , T _{STG}	- 55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	R _{thJA}	100	°C/W
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Note

a. Surface Mounted on FR4 Board , t ≤ 10sec .

b. Pulse width limited by maximum junction temperature.



ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V , I _D = 250uA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V , V _{GS} = 0V			1	uA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±8V , V _{DS} = 0V			±10	uA
ON CHARACTERISTICS^b						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	0.5	0.7	1	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 4.5V , I _D = 2.8A		50	65	m-ohm
		V _{GS} = 2.5V , I _D = 2.0A		65	90	
Forward Transconductance	g _{fs}	V _{DS} = 5V , I _D = 4A		10.7		S
DRAIN-SOURCE DIODE CHARACTERISTICS^b						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V , I _S = 1.7A			1.2	V
DYNAMIC CHARACTERISTICS^c						
Input Capacitance	C _{ISS}	V _{DS} = 6V , V _{GS} = 0V f = 1.0MHz		457		pF
Output Capacitance	C _{OSS}			119		pF
Reverse Transfer Capacitance	C _{RSS}			93		pF
SWITCHING CHARACTERISTICS^c						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 6V , I _D = 1A V _{GEN} = 4.5V R _L = 6 ohm R _{GEN} = 6 ohm		4	8	ns
Rise Time	t _r			14	26	ns
Turn-Off Delay Time	t _{D(OFF)}			21	39	ns
Fall Time	t _f			7.2		ns
Total Gate Charge	Q _g	V _{DS} = 6V		13		nC
Gate-Source Charge	Q _{gs}	I _D = 2.8A		4.1		nC
Gate-Drain Charge	Q _{gd}	V _{GS} = 4.5V		2.9		nC

Note
b. Pulse Test Pulse width ≤ 300us , Duty Cycle ≤ 2% .
c. Guaranteed by design , not subject to production testing .

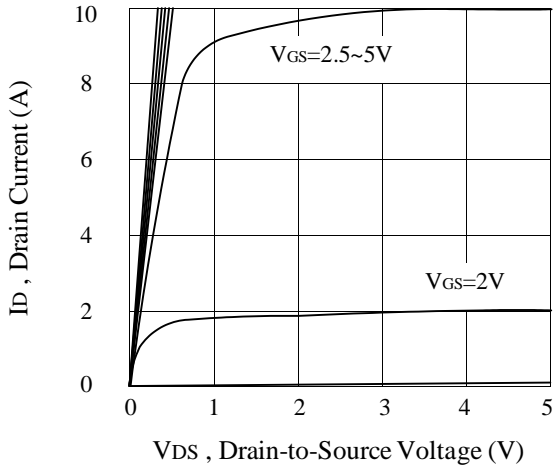


Figure 1. Output Characteristics

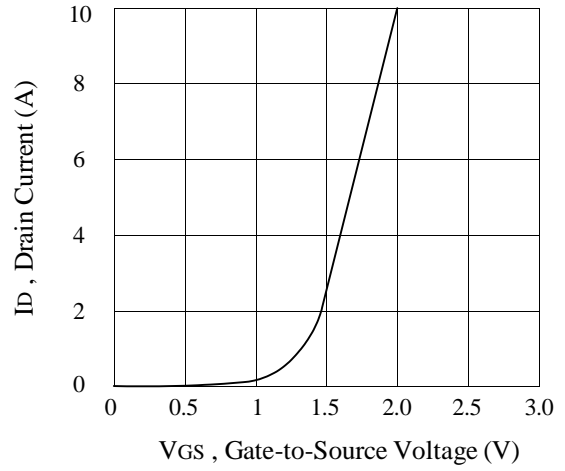


Figure 2. Transfer Characteristics

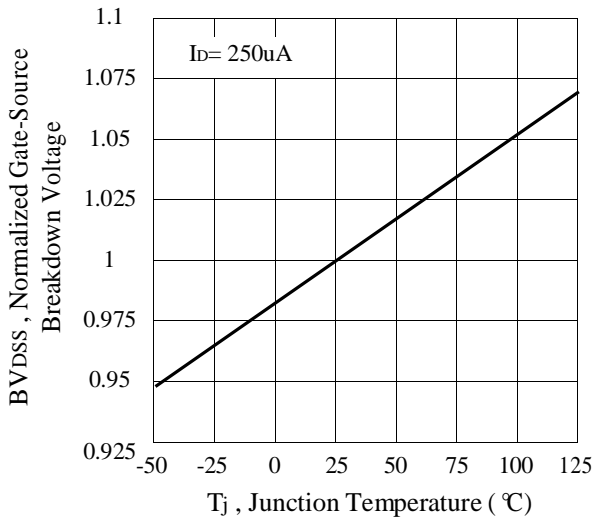


Figure 3. Breakdown Voltage Variation with Temperature

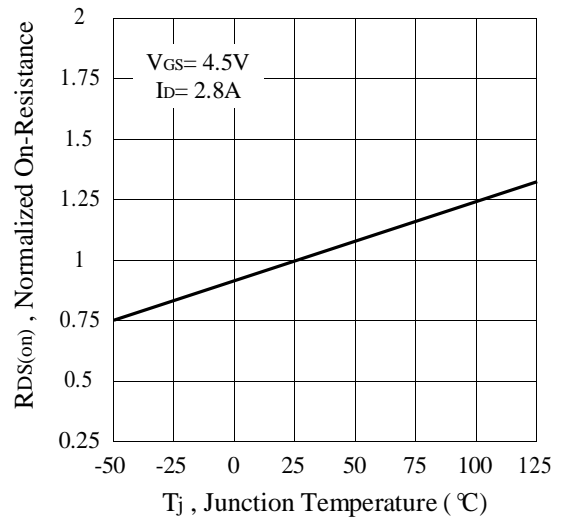


Figure 4. On-Resistance Variation with Temperature

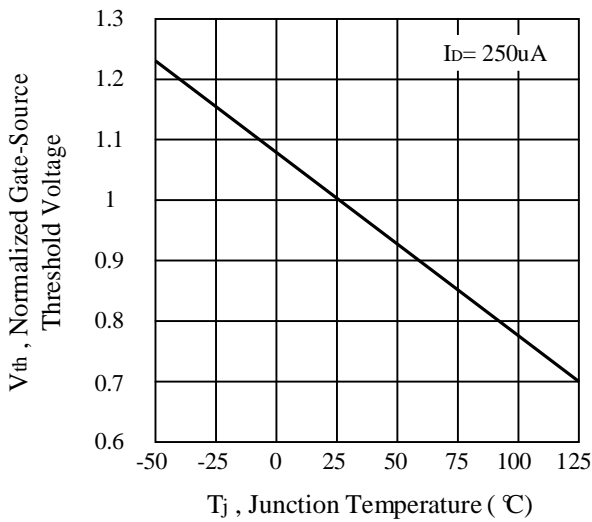


Figure 5. Gate Threshold Variation with Temperature

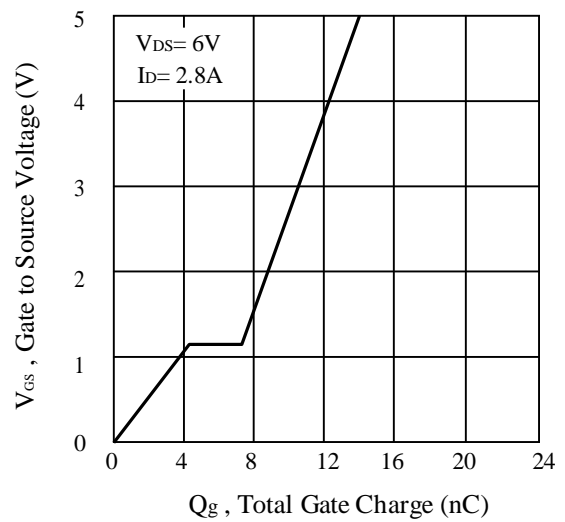


Figure 6. Gate Charge

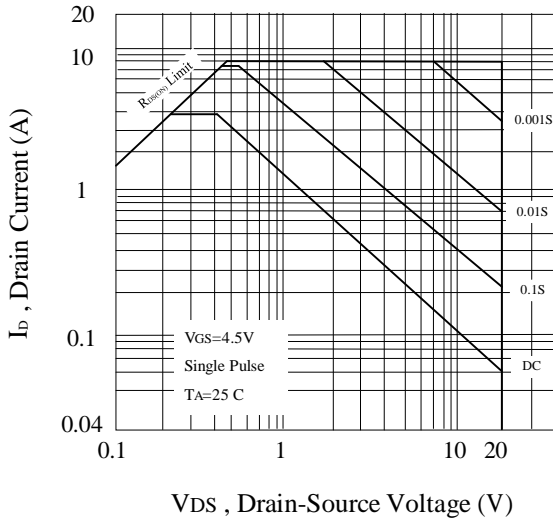


Figure 7. Maximum Safe Operating Area

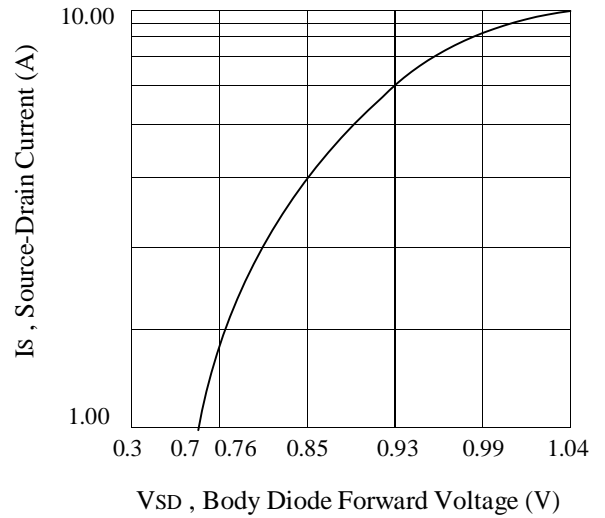


Figure 8. Body Diode Forward Voltage Variation with Source Current

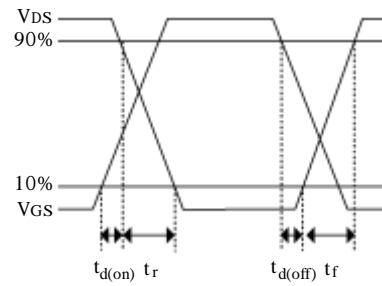
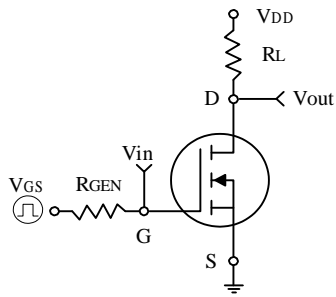


Figure 9. Switching Test Circuit and Switching Waveforms

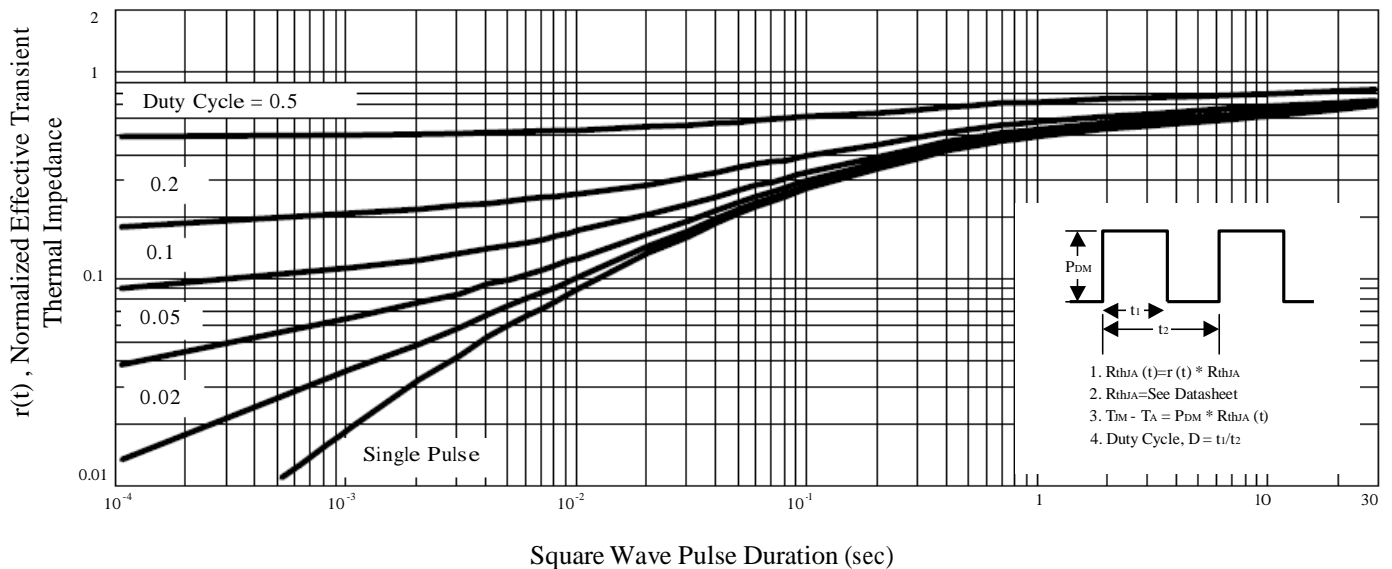


Figure 10. Normalized Thermal Transient Impedance Curve