21V,2A, 600KHz Synchronous Step-Down DC/DC Converter

Description

The PL5920 is a synchronous step-down DC/DC converter that provides wide 4.5V to 21V input voltage range and 2A continuous load current capability.

The PL5920 fault protection includes cycle-by-cycle current limit, UVLO, output overvoltage protection and thermal shutdown. The adjustable soft-start function prevents inrush current at turn-on. This device uses current mode control scheme which provides fast transient response. Internal Compensation function reduces external compensation components and simplifies the design process. In shutdown mode, the supply current is less than 1μA.

The PL5920 is available in a SOT-23-6 package, provides good thermal conductance.

Features

- High Efficiency up to 94%
- Low Rds(on) Integrated Power MOSFET
- Internal Compensation Function
- Wide Input Voltage Range: 4.5V to 21V
- Adjustable Output Voltage from 0.8V to 17.85V
- 2A Output Current
- Fixed 600KHz Switching Frequency
- Current Mode Operation
- Cycle-by-Cycle Current Limit
- Over-Temperature Protection with Auto Recovery
- Output Overvoltage Protection
- Under Voltage Lockout
- <1μA Shutdown Current
- SOT-23-6 Package

Applications

- STB (Set-Top-Box)
- LCD Displays, TVs
- Distributed Power Systems
- Networking, XDSL Modems

DC-DC Synchronous Step Down	VIN	VOUT	Iout(MAX)	Efficiency (%)	Oscillation Frequency	Compact Package
PL5900A	2.5V-5.5V	ADJ	1.2A (VIN=4.2V/5V, Vout=3.3V)	86%	1.5MHZ	SOT23-5
PL5902	2.5V-5.5V	ADJ	2.0A (VIN=4.2V/5V, Vout=3.3V)	88%	1MHZ	SOT23-5
PL5903	2.7V-5.5V	ADJ	3.0A (VIN=4.2V/5V, Vout=3.3V)	89%	1MHZ	SOT23-6
PL5920	4.5V-21V	ADJ	2A	94%	600KHZ	SOT23-6
……						
LDO Low Dropout Regulator	VIN	VOUT	Iout(MAX)	Accuracy	Quiescent Current	Compact Package
PL3501	2.7V-5.5V	1.2V,1.8V,2.8V 3.0V,3.3V	150MA	±1.5%	1μA	DFN-4L (EN Pin)
PL3502	2.0V-5.5V	1.2V,1.8V,2.8V 3.0V,3.3V	300MA	±2%	35μA	SOT23-5 (EN Pin)

Typical Application Circuit

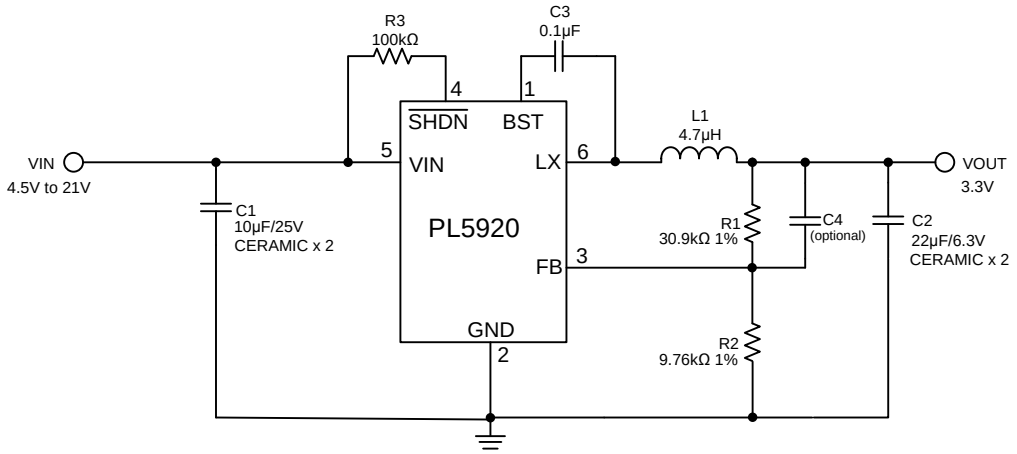


Figure 2. C_{IN} /C_{OUT} use Ceramic Capacitors Application Circuit

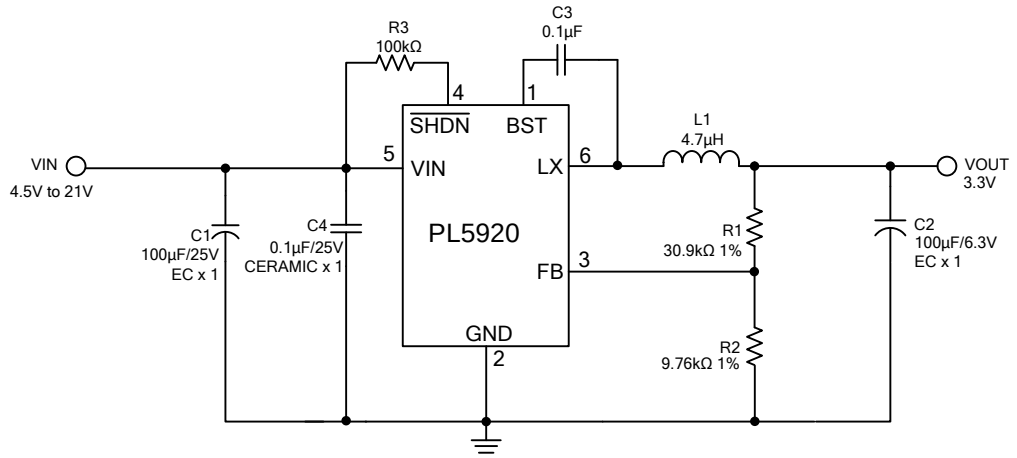


Figure 3. C_{IN} /C_{OUT} use Electrolytic Capacitors Application Circuit

V_{OUT}	R1	R2	C4	L1	C_{OUT}
1.2V	4.99kΩ	10kΩ	10pF~1nF	2.2μH	22μF MLCC x2
1.8V	4.99kΩ	3.92kΩ	10pF~1nF	2.2μH	22μF MLCC x2
2.5V	4.99kΩ	2.32kΩ	10pF~1nF	4.7μH	22μF MLCC x2
3.3V	30.9kΩ	9.76kΩ	10pF~1nF	4.7μH	22μF MLCC x2
5V	30.9kΩ	5.76kΩ	10pF~1nF	4.7μH	22μF MLCC x2
1.2V	4.99kΩ	10kΩ	--	2.2μH	100μF EC x1
1.8V	4.99kΩ	3.92kΩ	--	2.2μH	100μF EC x1
2.5V	4.99kΩ	2.32kΩ	--	4.7μH	100μF EC x1
3.3V	30.9kΩ	9.76kΩ	--	4.7μH	100μF EC x1
5V	30.9kΩ	5.76kΩ	--	4.7μH	100μF EC x1

Table 1. Recommended Component Values

Pin Assignments

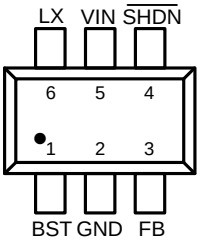


Figure 1. Pin Assignment of PL5920

PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. Multi-layer PCB design is recommended.

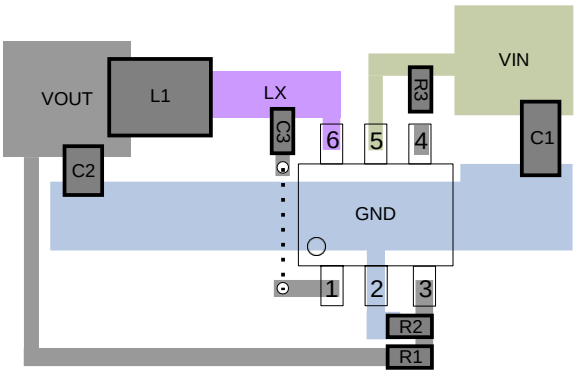


Figure 25. PL5920 Recommended Layout Diagram

Functional Pin Description

Functional Pin Description

Pin Name	Pin No.	Pin Function
FB	**3**	Voltage Feedback Input Pin. Connect FB and VOUT with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.8V.
VIN	**5**	Power Supply Input Pin. Drive VIN pin by 4.5V to 21V voltage to power on the chip.
$\overline{\text{SHDN}}$	**4**	Enable Input Pin. This pin is a digital control input which turns the converter on or off. Connect to VIN with a 100kΩ resistor for self-startup.
GND	**2**	Ground Pin.
LX	**6**	Power Switching Output. LX is the output of the internal high side NMOS switch.
BST	**1**	High Side Gate Drive Boost Pin. A capacitor rating between 10nF~100nF must be connected from this pin to LX. It can boost the gate drive to fully turn on the internal high side NMOS.

Block Diagram

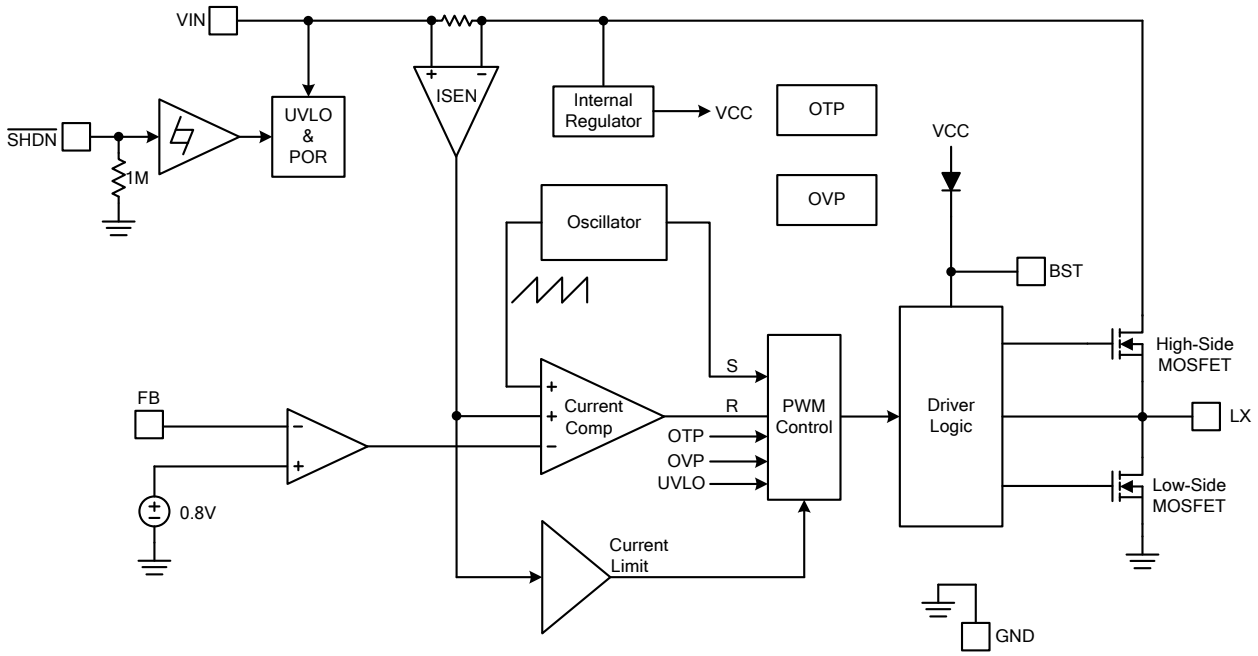


Figure 4. Block Diagram of PL5920

Absolute Maximum Ratings (Note 1)

- Supply Voltage V_{IN} ---------- -0.3V to +23V
- Enable Voltage $V_{\overline{SHDN}}$ ---------- -0.3V to +23V
- LX Voltage V_{LX}(50ns) ---------- -1V to V_{IN}+0.3V
- BST Pin Voltage V_{BST} ---------- V_{LX}-0.3V to V_{LX}+6V
- All Other Pins Voltage ---------- -0.3V to +6V
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Package Thermal Resistance, (θ_{JA})

  SOT-23-6 ---------- +250°C/W
- Package Thermal Resistance, (θ_{JC})

  SOT-23-6 ---------- +110°C/W

Note 1：Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage V_{IN} ---------- +4.5V to +21V
- Operation Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(V_{IN}=12V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{IN} Input Supply Voltage	V_{IN}		4.5		21	V
V_{IN} Quiescent Current	I_{DDQ}	$V_{\overline{SHDN}}$=1.8V, V_{FB}=1.0V		2.5		mA
V_{IN} Shutdown Supply Current	I_{SD}	$V_{\overline{SHDN}}$=0V			1	μA
Feedback Voltage	V_{FB}	4.5V≦V_{IN}≦21V	0.78	0.8	0.82	V
Feedback OVP Threshold Voltage	V_{OVP}			1.4		V
High-Side MOSFET $R_{DS(ON)}$ (Note 2)	$R_{DS(ON)}$			120		mΩ
Low-Side MOSFET $R_{DS(ON)}$ (Note 2)	$R_{DS(ON)}$			110		mΩ
High-Side MOSFET Leakage Current	$I_{LX(leak)}$	$V_{\overline{SHDN}}$=0V, V_{LX}=0V			10	μA
High-Side MOSFET Current Limit (Note 2)	$I_{LIMIT(HS)}$	Minimum Duty	2.5	3		A
Low-Side MOSFET Current Limit (Note 2)	$I_{LIMIT(LS)}$	From Drain to Source		1.5		A
Error Amplifier Voltage Gain (Note 2)				400		V/V
Oscillation Frequency	F_{OSC}		480	600	720	KHz
Short Circuit Oscillation Frequency	$F_{OSC(short)}$	V_{FB}=0V		160		KHz
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.6V		85		%
Minimum On Time (Note 2)	T_{MIN}			100		ns
Input UVLO Threshold	$V_{UVLO(Vth)}$	V_{IN} Rising		4.3		V
Under Voltage Lockout Threshold Hysteresis	$V_{UVLO(HYS)}$			400		mV
$\overline{SHDN}$ Input Low Voltage	$V_{\overline{SHDN}(L)}$				0.4	V
$\overline{SHDN}$ Input High Voltage	$V_{\overline{SHDN}(H)}$		2			V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$	V_{IN} =2V		2		μA
Thermal Shutdown Threshold (Note 2)	T_{SD}			160		°C

Note 2：Not production tested.

Typical Performance Curves

V_{IN}=12V, V_{OUT}=3.3V, C1=10μF x 2, C2=22μF x 2, L1=4.7μH, TA=+25°C, unless otherwise noted.

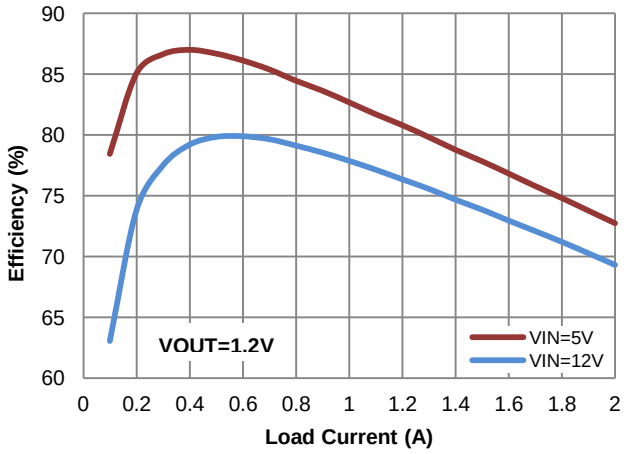


Figure 5. Efficiency vs. Load Current

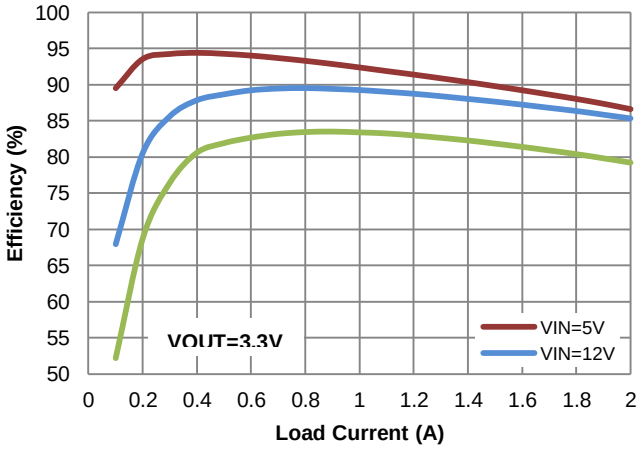


Figure 6. Efficiency vs. Load Current

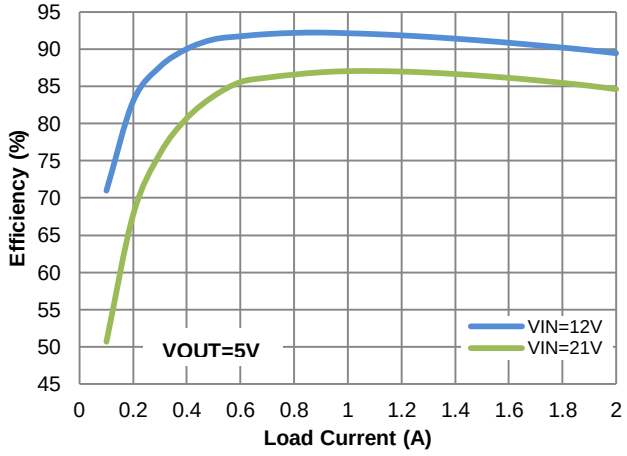


Figure 7. Efficiency vs. Load Current

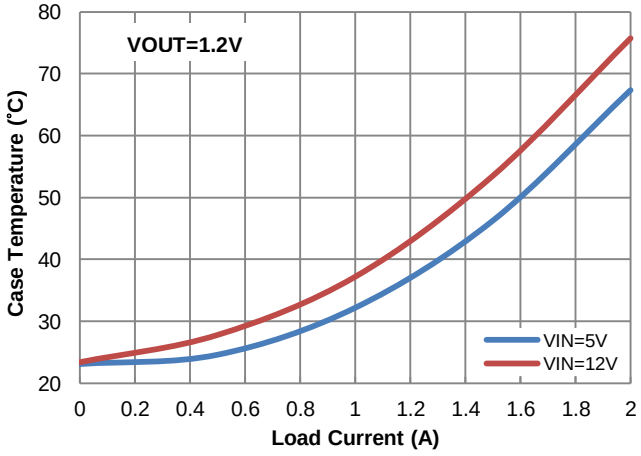


Figure 8. Case Temperature vs. Load Current

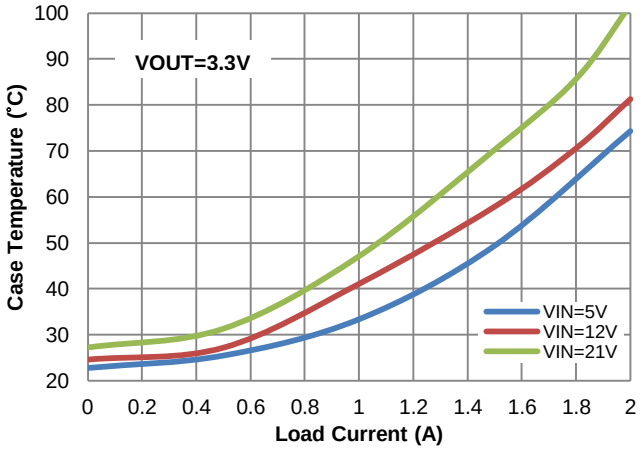


Figure 9. Case Temperature vs. Load Current

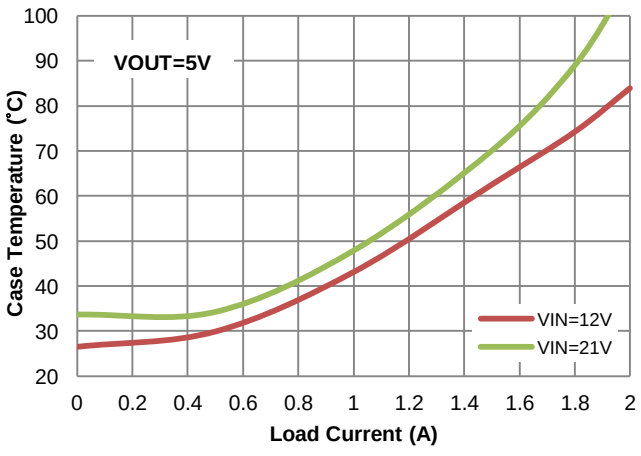


Figure 10. Case Temperature vs. Load Current

Typical Performance Curves (Continued)

V_{IN}=12V, V_{OUT}=3.3V, C1=10μF x 2, C2=22μF x 2, L1=4.7μH, TA=+25°C, unless otherwise noted.

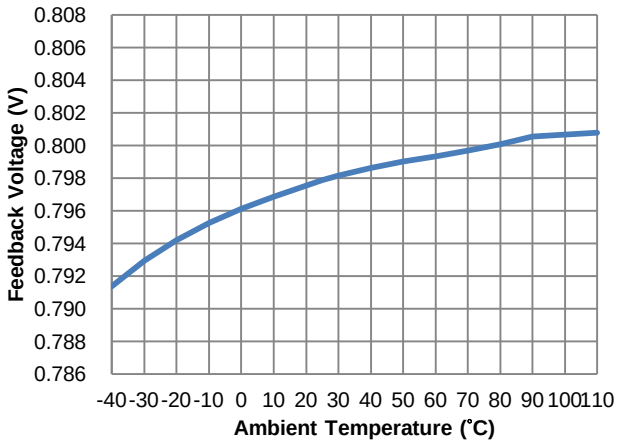


Figure 11. Feedback Voltage vs. Temperature

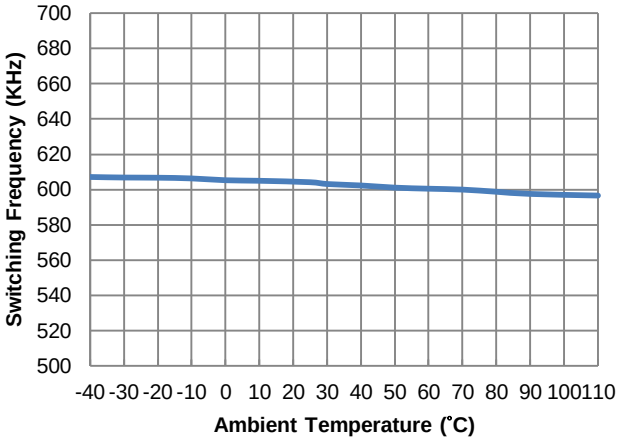
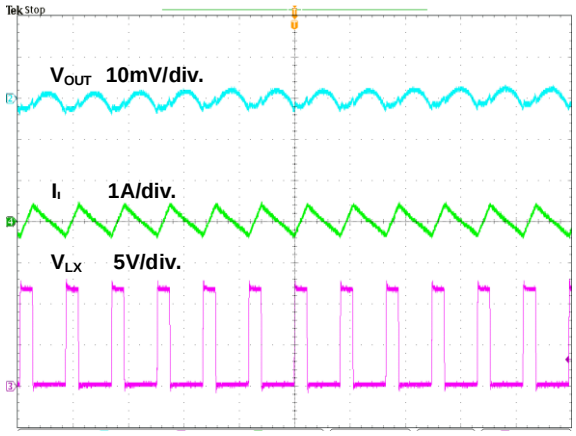


Figure 12. Switching Frequency vs. Temperature

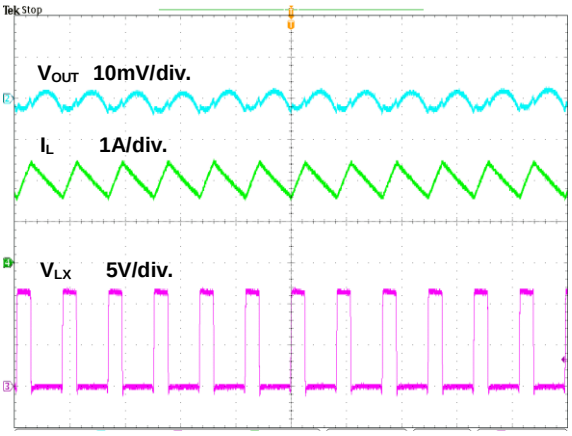
I_{OUT}=0A



2μs/div.

Figure 13. Steady State Waveform

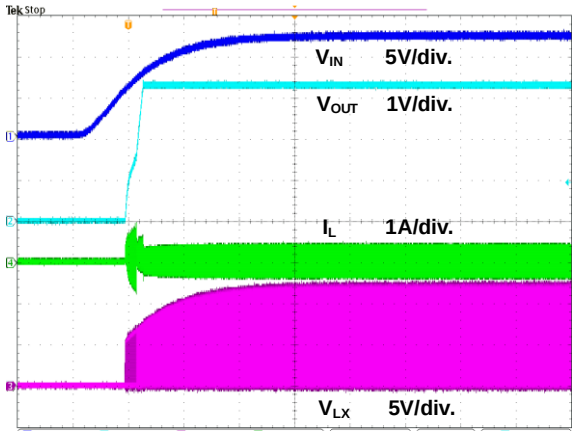
I_{OUT}=2A



2μs/div.

Figure 14. Steady State Waveform

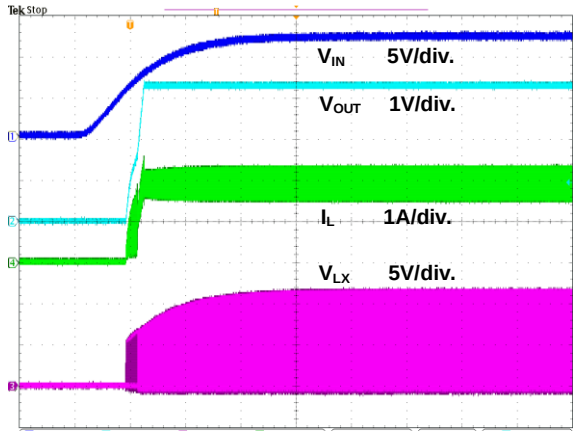
I_{OUT}=0A



4ms/div.

Figure 15. Power On through VIN Waveform

I_{OUT}=2A



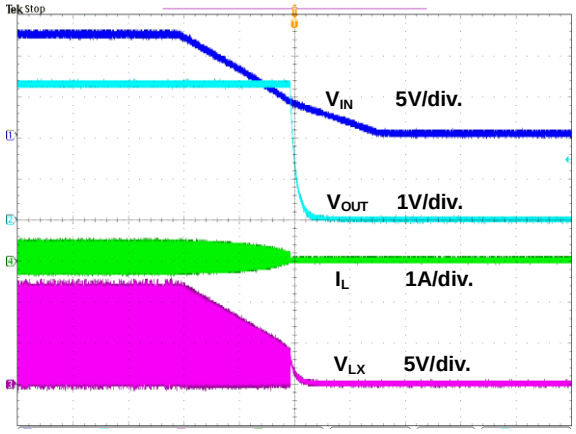
4ms/div.

Figure 16. Power On through VIN Waveform

Typical Performance Curves (Continued)

V_{IN}=12V, V_{OUT}=3.3V, C1=10μF x 2, C2=22μF x 2, L1=4.7μH, TA=+25°C, unless otherwise noted.

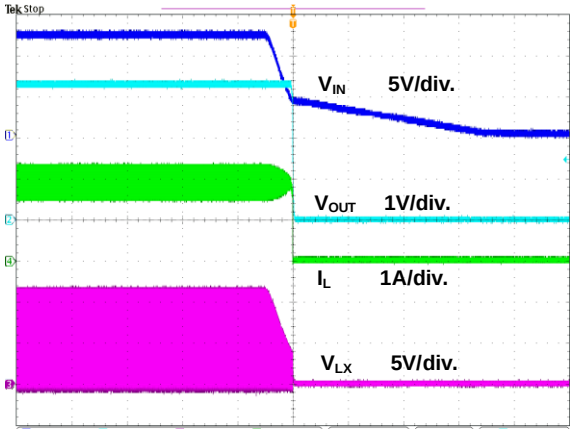
I_{OUT}=0A



20ms/div.

Figure 17. Power Off through VIN Waveform

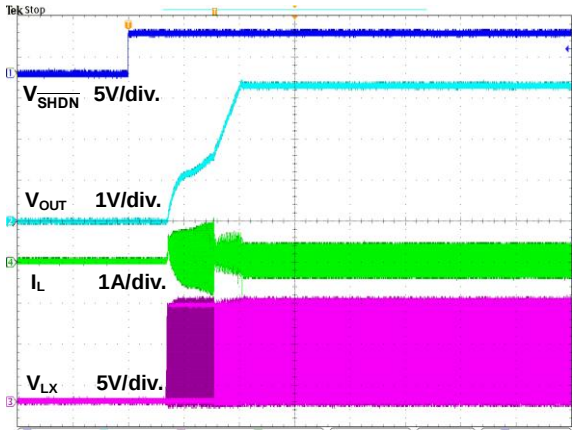
I_{OUT}=2A



10ms/div.

Figure 18. Power Off through VIN Waveform

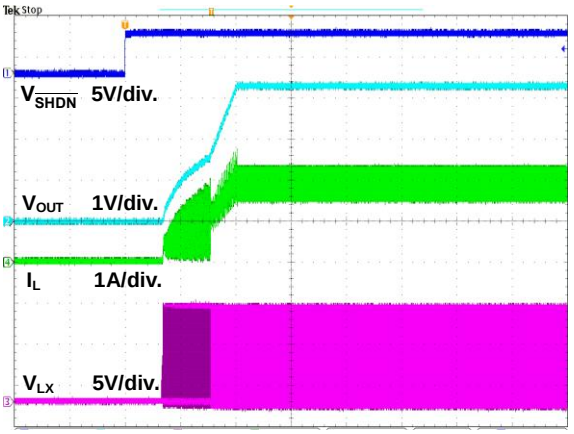
I_{OUT}=0A



1ms/div.

Figure 19. Power On through $\overline{SHDN}$ Waveform

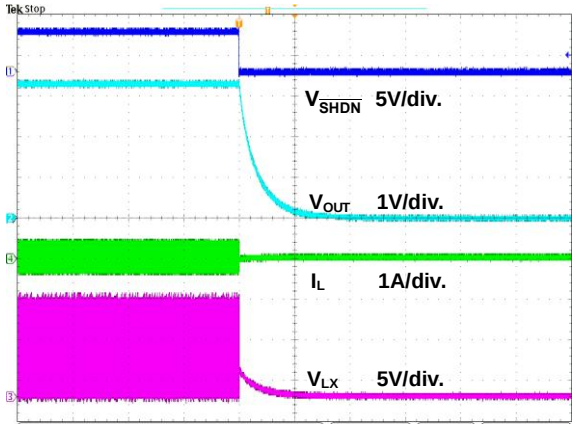
I_{OUT}=2A



1ms/div.

Figure 20. Power On through $\overline{SHDN}$ Waveform

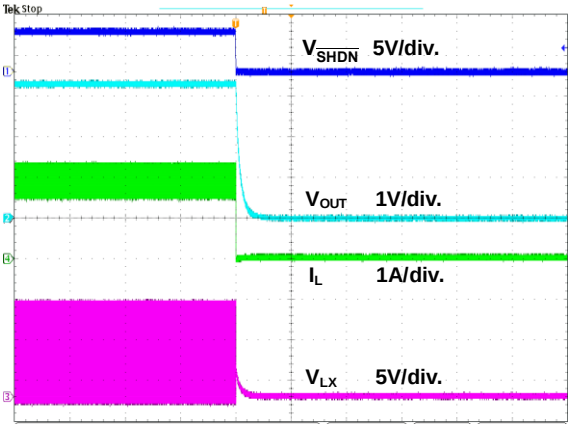
I_{OUT}=0A



10ms/div.

Figure 21. Power Off through $\overline{SHDN}$ Waveform

I_{OUT}=2A



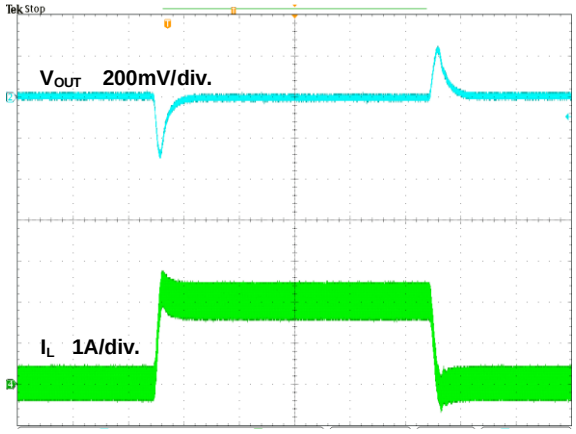
1ms/div.

Figure 22. Power Off through $\overline{SHDN}$ Waveform

Typical Performance Curves (Continued)

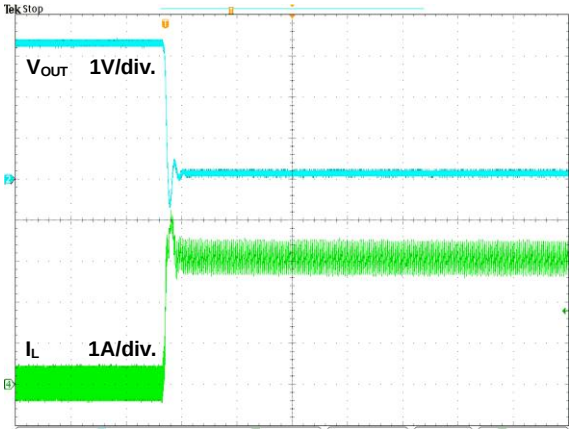
V_{IN}=12V, V_{OUT}=3.3V, C1=10μF x 2, C2=22μF x 2, L1=4.7μH, TA=+25°C, unless otherwise noted.

I_{OUT}=0A to 2A



200μs/div.

Figure 23. Load Transient Waveform



200μs/div.

Figure 24. Short Circuit Test

Function Description

The PL5920 is a high efficiency, internal compensation and constant frequency current mode synchronous step-down DC/DC converter. It regulates input voltage from 4.5V to 21V and down to output voltage as low as 0.8V.

Control Loop

Under normal operation, the output voltage is sensed by FB pin through a resistive voltage divider and amplified through the error amplifier. The voltage of error amplifier output is compared to the switch current to control the RS latch. At the beginning of each clock cycle, the high-side NMOS turns on when the oscillator sets the RS latch, and turns off when current comparator resets the RS latch. Then the low-side NMOS will turn on until the clock period ends.

Enable

The PL5902 $\overline{\text{SHDN}}$ pin provides digital control to turn on/off the regulator. When the voltage of $\overline{\text{SHDN}}$ exceeds the threshold voltage, the regulator will start the soft start function. If the $\overline{\text{SHDN}}$ pin voltage is below the shutdown threshold voltage, the regulator will turn into the shutdown mode and the shutdown current will be smaller than 1μA. For auto start-up operation, connect $\overline{\text{SHDN}}$ to VIN through a 100KΩ resistor.

Soft Start

The PL5920 employs internal soft start function to reduce input inrush current during start up. The typical value of internal soft start time is 1ms.

Output Over Voltage Protection

When the FB pin voltage exceeds 1.4V, the output over voltage protection function will be triggered and turn off the high-side/low-side MOSFET.

Input Under Voltage Lockout

When the PL5920 is power on, the internal circuits will be held inactive until V_{IN} voltage exceeds the input UVLO threshold voltage. And the regulator will be disabled when V_{IN} is below the input UVLO threshold voltage. The hysteretic of the UVLO comparator is 400mV (typ).

Short Circuit Protection

The PL5920 provides short circuit protection function to prevent the device damaged from short condition. When the short condition occurs and the feedback voltage drops lower than 0.4V, the oscillator frequency will be reduced to 160KHz to prevent the inductor current increasing beyond the current limit. In the meantime, the current limit will also be reduced to lower the short current. Once the short condition is removed, the frequency and current limit will return to normal.

Over Current Protection

The PL5920 over current protection function is implemented by using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side MOSFET series sense resistor voltage. When the load current increases, the inductor current will also increase. When the peak inductor current reaches the current limit threshold, the output voltage will start to drop. When the over current condition is removed, the output voltage will return to the regulated value.

Over Temperature Protection

The PL5920 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 60°C (typ).

Internal Compensation Function

The stability of the feedback circuit is controlled by internal compensation circuits. This internal compensation function is optimized for most applications, and this function can reduce external R, C components.

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set by using a resistive divider from the output to FB. The FB pin regulated voltage is 0.8V. Thus the output voltage is:

$$V_{OUT}=0.8V\times\left(1+\frac{R1}{R2}\right)$$

Table 2 lists recommended values of R1 and R2 for most used output voltage.

Table 2 Recommended Resistance Values

V_{OUT}	R1	R2
5V	30.9kΩ	5.76kΩ
3.3V	30.9kΩ	9.76kΩ
2.5V	4.99kΩ	2.32kΩ
1.8V	4.99kΩ	3.92kΩ
1.2V	4.99kΩ	10kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

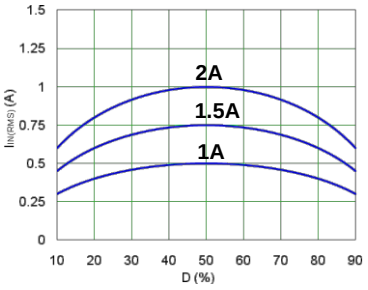
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)}$$

$$D=\frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1μF ceramic capacitor should be placed as close to the IC as possible.

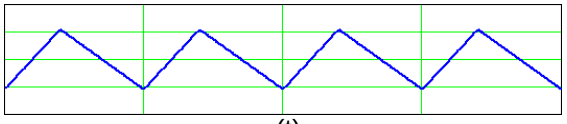
Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t)=V_{RIPPLE(C)}(t)+V_{RIPPLE(ESR)}(t)+V_{RIPPLE(ESL)}(t)+V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.

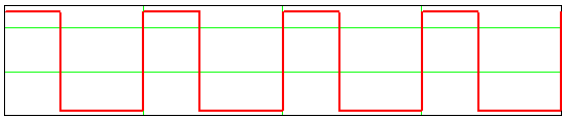
$V_{RIPPLE(ESR)}(t)$



(t)

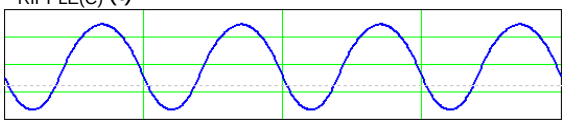
+

$V_{RIPPLE(ESL)}(t)$



+ (t)

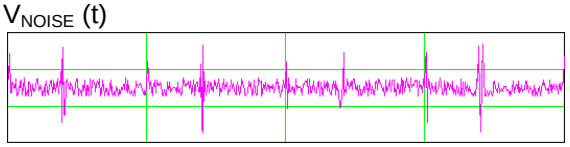
$V_{RIPPLE(C)}(t)$



(t)

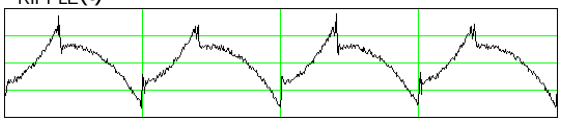
+

$V_{NOISE}(t)$



=

$V_{RIPPLE}(t)$



(t)

Application Information (Continued)

$$V_{RIPPLE(ESR,\ p\text{-}p)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR$$

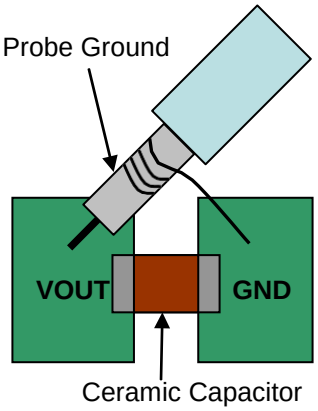
$$V_{RIPPLE(ESL,\ p\text{-}p)}=\frac{ESL}{L+ESL}\times V_{IN}$$

$$V_{RIPPLE(C,\ p\text{-}p)}=\frac{V_{OUT}}{8\times F_{OSC}^2\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirement. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Removing the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminating noise.



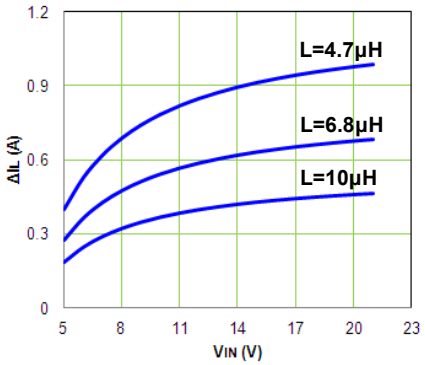
Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode.

That will lower ripple current and result in lower output ripple voltage. The Δ_L is inductor peak-to-peak ripple current:

$$\Delta I_L=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The following diagram is an example to graphically represent Δ_L equation.



V_{OUT}=3.3V, F_{OSC}=600KHz

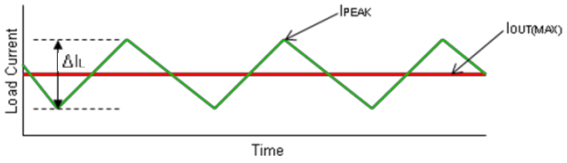
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current Δ_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current Δ_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L=0.3\times I_{OUT(MAX)}$$

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times F_{OSC}\times\Delta I_L}$$

To guarantee sufficient output current, peak inductor current must be lower than the PL5920 high-side MOSFET current limit. The peak inductor current is shown as below:

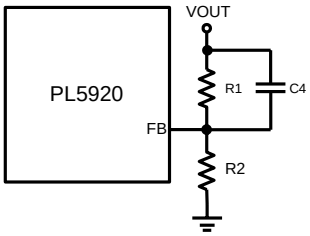
$$I_{PEAK}=I_{OUT(MAX)}+\frac{\Delta I_L}{2}$$



Application Information (Continued)

Feedforward Capacitor Selection

Internal compensation function allows users saving time in design and saving cost by reducing the number of external components. The use of a feedforward capacitor C4 in the feedback network is recommended to improve the transient response or higher phase margin.



For optimizing the feedforward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feedforward capacitor identified, the value of feedforward capacitor C4 can be calculated with the following equation:

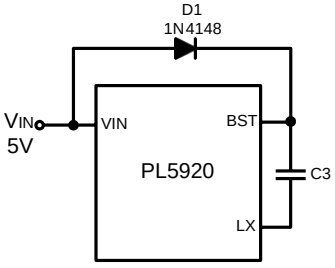
$$C4=\frac{1}{2\pi\times F_{CROSS}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feedforward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and causes more ringing. In the other hand, if more phase margin is desired, the feedforward capacitor value can be decreased to push the cross frequency to lower region. In general, the feedforward capacitor range is between 10pF to 1nF.

External Boost Diode Selection

For 5V input applications, it is recommended to add an external boost diode. This helps improving the efficiency. The boost diode can be a low cost one such as 1N4148.



PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. Multi-layer PCB design is recommended.

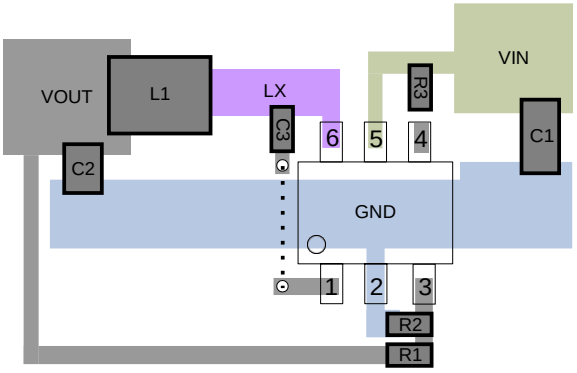
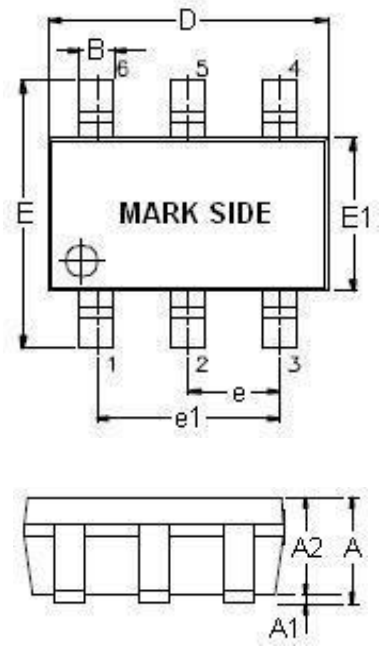
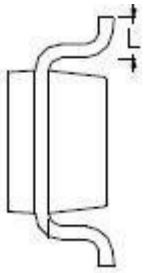


Figure 25. PL5920 Recommended Layout Diagram

Outline Information

SOT-23-6 Package (Unit: mm)

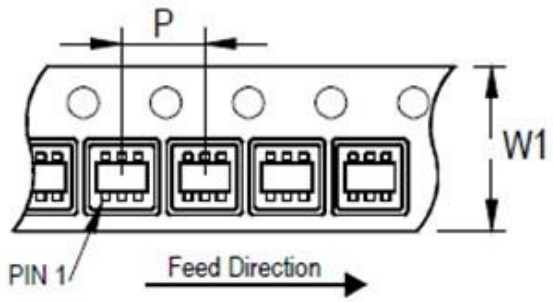


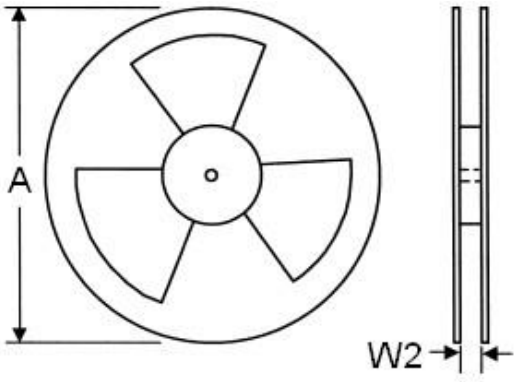


SYMBOLS UNIT	DIMENSION IN MILLIME ER	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60

Note：Followed From JEDEC MO-178-C.

Carrier dimensions





Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000