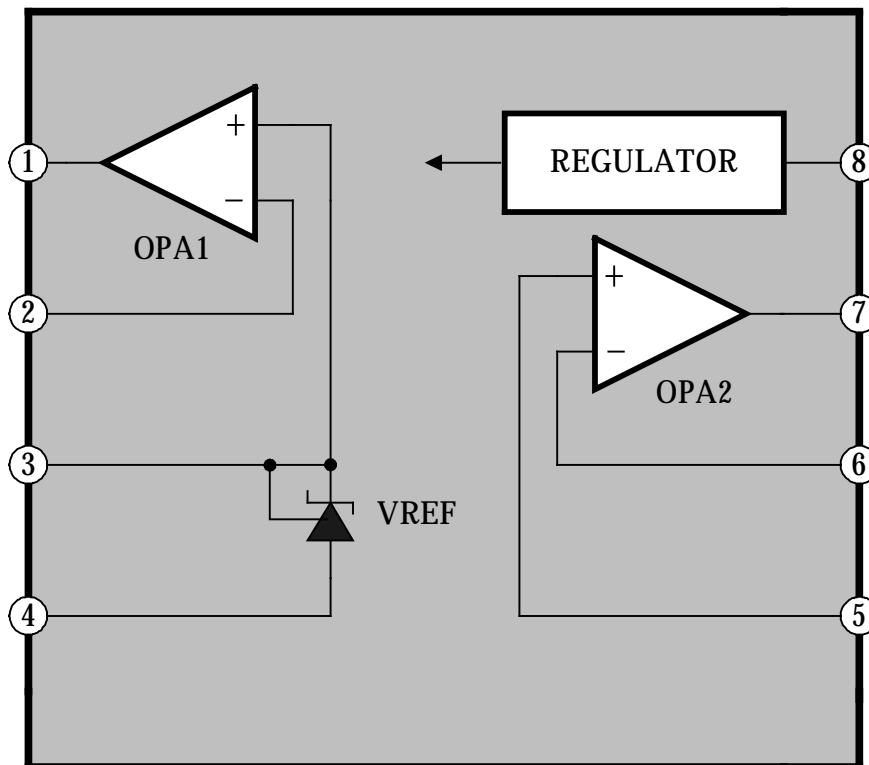
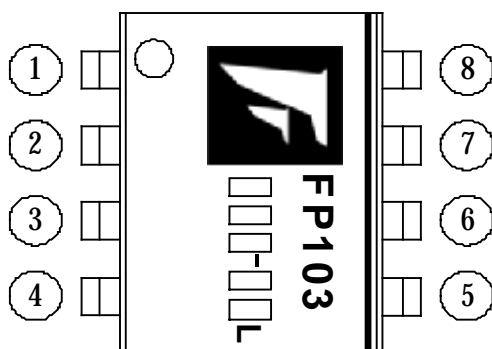


FUNCTIONAL BLOCK DIAGRAM



MARK VIEW

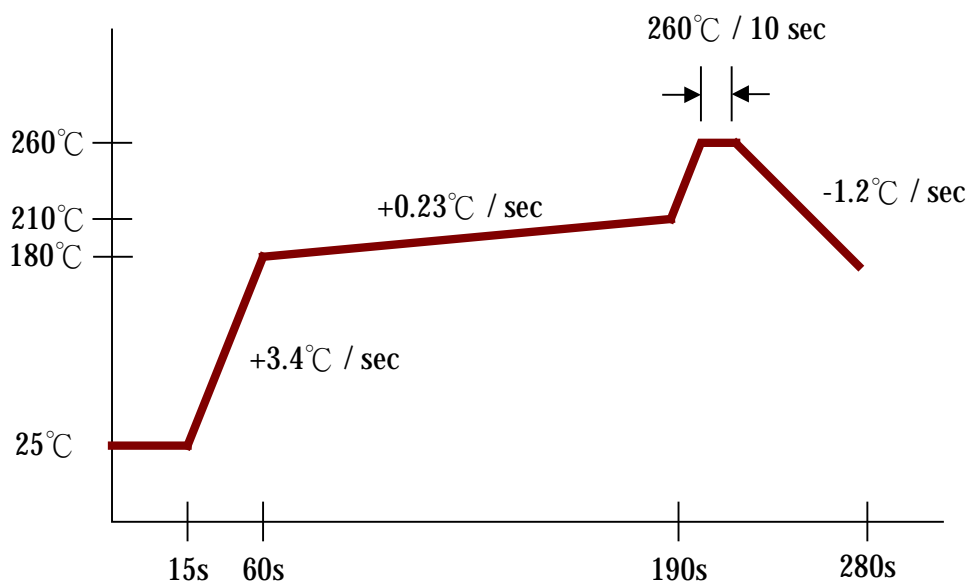


PIN DESCRIPTION

NAME	NO.	STATUS	DESCRIPTION
VO1	1	O	OPA1 Output
VI1	2	I	OPA1 Inverting Input
VNI1	3	I	OPA1 Non-inverting Input
VEE	4	P	IC Ground or Negative Supply Voltage
VNI2	5	I	OPA2 Non-inverting Input
VI2	6	I	OPA2 Inverting Input
VO2	7	O	OPA2 Output
VCC	8	P	Positive Supply Voltage

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{cc})	-----	+ 3.6 V
Differential Input Voltage (V _{id})	-----	+ 3.6 V
Input Voltage (V _i)	-----	-0.3 ~+36V
Maximum Junction Temperature (T _j)	-----	150 °C
Thermal Resistance Junction to Ambient (SOP package)	-----	175 °C/W
(PDIP package)	-----	100 °C/W
Power Dissipation (SOP8 package)		
Ta=25 °C	-----	650mW
Ta=70 °C	-----	550mW
Operating Temperature Range (T _{min} ~T _{max} .)	-----	-20 °C ~ 85 °C
Storage Temperature Range	-----	- 65 °C ~ 150 °C
SOP8 Lead Temperature (soldering, 10 sec)	-----	+260 °C
PDIP8 Lead Temperature (soldering, 20 sec)	-----	+260 °C



IR-REFLOW

DC ELECTRICAL CHARACTERISTICS

Operating Amplifier1

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{io}	FP103, $T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$		1	4 5	mV
Input Offset Voltage Drift	DV_{io}	$T_{amb}=25^{\circ}C$		7		$\mu V/^{\circ}C$
Input Bias Current (negative input)	I_{ib}	$T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$		20		nA
Large Signal Voltage Gain	A_{vd}	$V_{icm}=0V$ $V_{CC}=15V, R_L=2K$		100		V/mV
Supply Voltage Rejection Ratio	SVR	$V_{icm}=0V$ $V_{CC}=5V$ to 30V	65	100		dB
Output Current Source	I_{source}	$V_{CC}=+15V$ $V_O=2V, V_{id}=+1V$	30	50		mA
Short Circuit to Ground	I_o	$V_{CC}=+15V$		50	70	mA
Output Current Sink	I_{sink}	$V_{id}=-1V$ $V_{CC}=+15V, V_O=2V$	8	10		mA
High Level Output Voltage	V_{OH}	$V_{CC}^+=30V$ $T_{amb}=25^{\circ}C, R_L=10K$ $T_{min} \leq T_{amb} \leq T_{max}$	27 27	28		V
Low Level Output Voltage	V_{OL}	$R_L=10K$ $T_{min} \leq T_{amb} \leq T_{max}$		3	20 20	mV
Slew Rate at Unity Gain	SR	$V_i=0.5$ to 2V, $V_{CC}=15V$ $R_L=2K, C_L=100pF$ Unity Gain	0.2	0.4		$V/\mu S$
Gain Bandwidth Product	GBP	$V_{CC}=30V, R_L=2K$ $C_L=100pF, f=100kHz,$ $V_{in}=10$ mV	0.5	0.9		MHz
Total Harmonic Distortion	THD	$f=1kHz, A_V=20dB$ $R_L=2K, V_{CC}=30V$ $C_L=100pF, V_O=2V_{PP}$		0.02		%

DC ELECTRICAL CHARACTERISTICS (Cont.)

Operating Amplifier2

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{io}	FP103, $T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$.		1	4 5	mV
Input Offset Voltage Drift	DV_{io}	$T_{amb}=25^{\circ}C$		7		$\mu V/^{\circ}C$
Input Offset Current	I_{io}	$T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$		2	30 50	nA
Input Bias Current	I_{ib}	$T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$		20	150 200	nA
Large Signal Voltage Gain	A_{vd}	$V_{CC}=15V, R_L=2K,$ $V_O=1.4V$ to $11.4V$ $T_{min} \leq T_{amb} \leq T_{max}$	50 25	100		V/mV
Supply Voltage Rejection Ratio	SVR	$V_{CC}=5V$ to $30V$	65	100		dB
Input Common Mode Voltage Range	V_{icm}	$V_{CC}=+30V$ $T_{min} \leq T_{amb} \leq T_{max}$	0 0		$(V_{CC}^+)-1.5$ $(V_{CC}^+)-2$	V
Common Mode Rejection Ratio	CMRR	$T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	70 60	85		dB
Output Current Source	I_{source}	$V_{CC}=+15V,$ $V_O=2V, V_{id}=+1V$	30	50		mA
Short Circuit to Ground	I_o	$V_{CC}=+15V,$		50	70	mA
Output Current Sink	I_{sink}	$V_{id}=-1V,$ $V_{CC}=+15V, V_O=2V$	7	10		mA
High Level Output Voltage	V_{OH}	$V_{CC}^+=30V$ $T_{amb}=25^{\circ}C, R_L=10K$ $T_{min} \leq T_{amb} \leq T_{max}$	27 27	28		V
Low Level Output Voltage	V_{OL}	$R_L=10K$ $T_{min} \leq T_{amb} \leq T_{max}$		3	20 20	mV
Slew Rate at Unity Gain	SR	$V_i=0.5$ to $3V, V_{CC}=15V$ $R_L=2K, C_L=100pF,$ Unity Gain	0.2	0.4		$V/\mu S$
Gain Bandwidth Product	GBP	$V_{CC}=30V, R_L=2K$ $C_L=100pF, f=100kHz,$ $V_{in}=10mV$	0.5	0.9		MHz
Total Harmonic Distortion	THD	$f=1kHz, A_v=20dB$ $R_L=2K, V_{CC}=30V$ $C_L=100pF, V_O=2V_{PP}$		0.02		%

DC ELECTRICAL CHARACTERISTICS (Cont.)

Voltage Reference

PARAMETER	SYMBOL	VALUE	UNIT
Cathode Current	I_k	1 to 100	mA

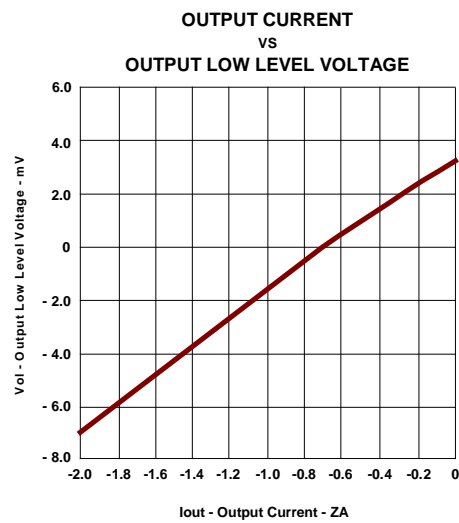
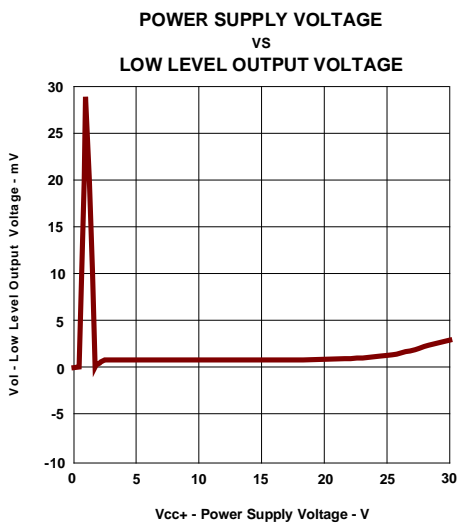
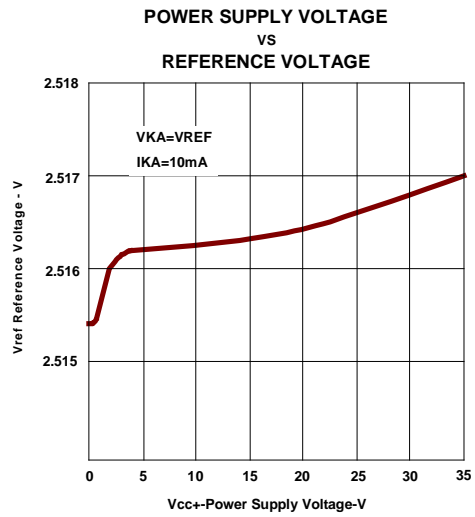
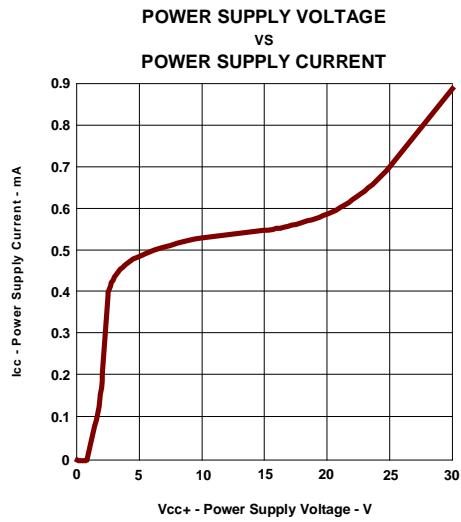
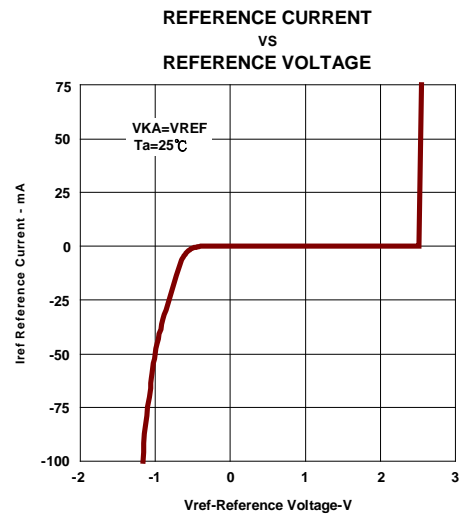
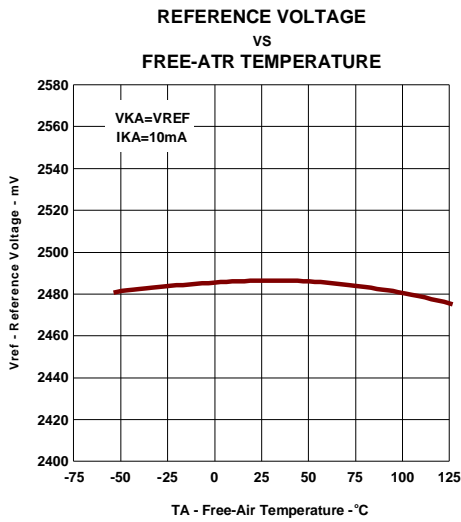
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Input Voltage	V_{ref}	FP103, $T_{amb}=25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	2.475 2.450	2.5	2.525 2.550	V
Reference Input Voltage Deviation Over Temperature Range	ΔV_{ref}	$V_{KA}=V_{ref}; I_K=10mA$ $T_{min} \leq T_{amb} \leq T_{max}$		7	30	mV
Minimum Cathode Current for Regulation	I_{min}	$V_{KA}=V_{ref}$		0.2	1	mA
Dynamic Impedance (note 1)	$ Z_{KA} $	$V_{KA}=V_{ref}, \Delta I_K=1 \text{ to } 100mA,$ $f < 1KHz, \text{note1}$		0.2	0.5	Ω

1. The dynamic impedance is defined as $Z_{KA} = \Delta V_{KA} / \Delta I_K$

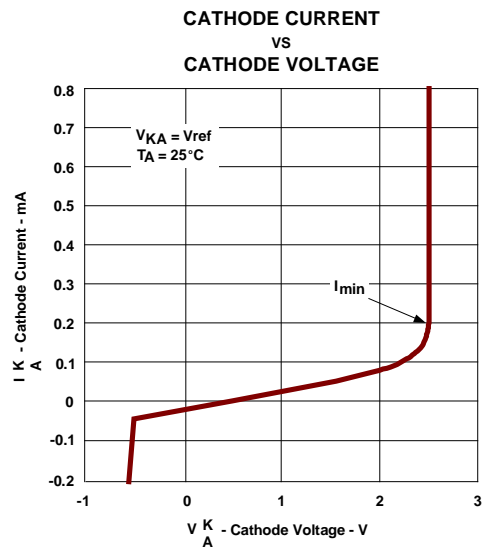
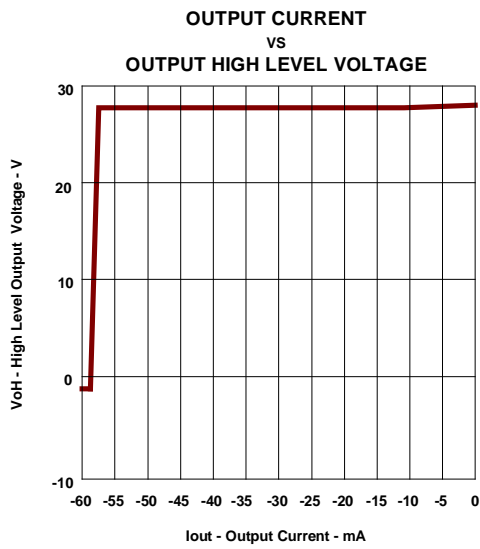
Total Supply Current

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total Supply Current, excluding Current in the Voltage Reference	I_{CC}	$V_{CC}=+5V, \text{no load}$ $T_{min} < T_{amb} < T_{max}$ $V_{CC}=+30V, \text{no load}$ $T_{min} < T_{amb} < T_{max}$		0.7	1.2 2	mA

TYPICAL CHARACTERISTICS

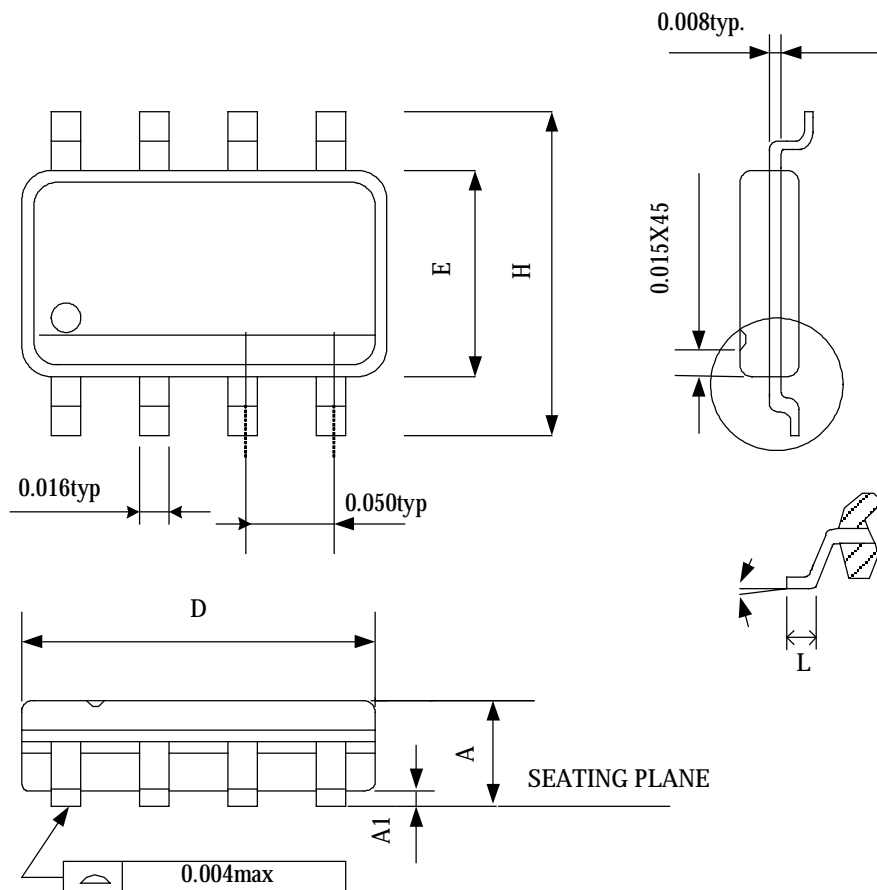


TYPICAL CHARACTERISTICS (Cont.)



PACKAGE OUTLINE

SOP 8



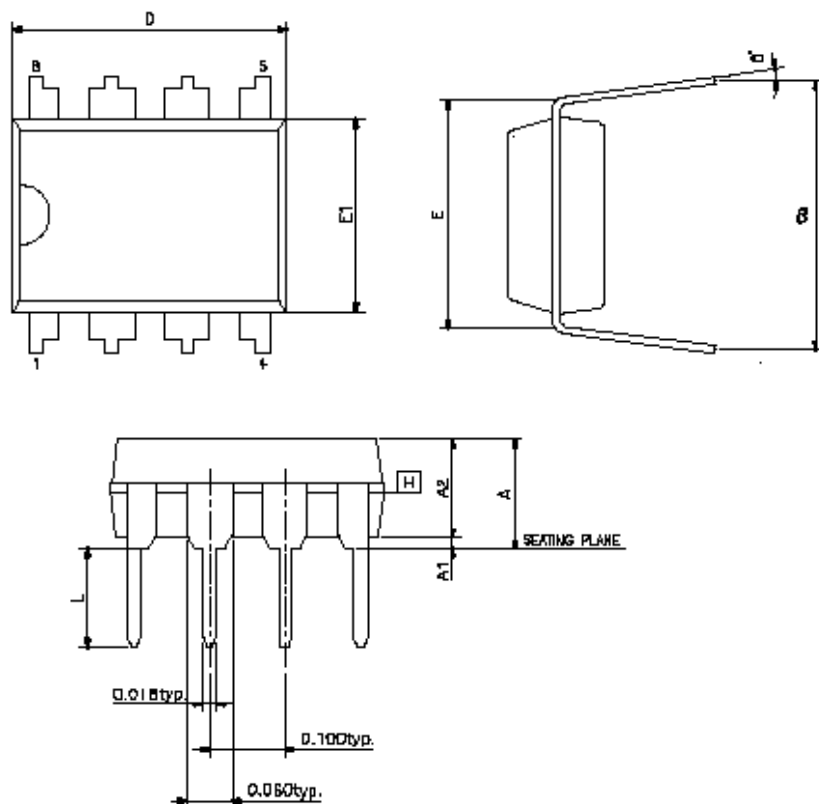
SYMBOLS	MIN	MAX
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT:INCH

NOTE:

1. JEDEC OUTLINE:MS-012 AA
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH,PROTRUSIONS OR GATE BURRS.MOLD FLASH,PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.06in) PER SIDE
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH,OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.0.10in) PER SIDE.

PDIP 8



SYMBOLS	MIN	NOR	MAX
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E	0.300BSC		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e _⊕	0.335	0.355	0.375
θ°	0	7	15

UNIT:INCH

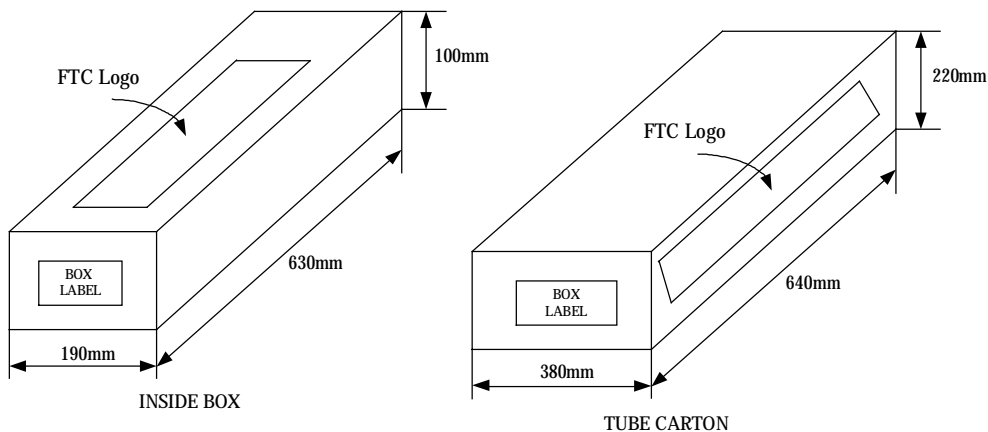
Note:

4. JEDEC OUTLINE:MS-001 BA
5. "D""E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH
6. e_⊕ IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION
7. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM
8. DATUM PLANE H COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

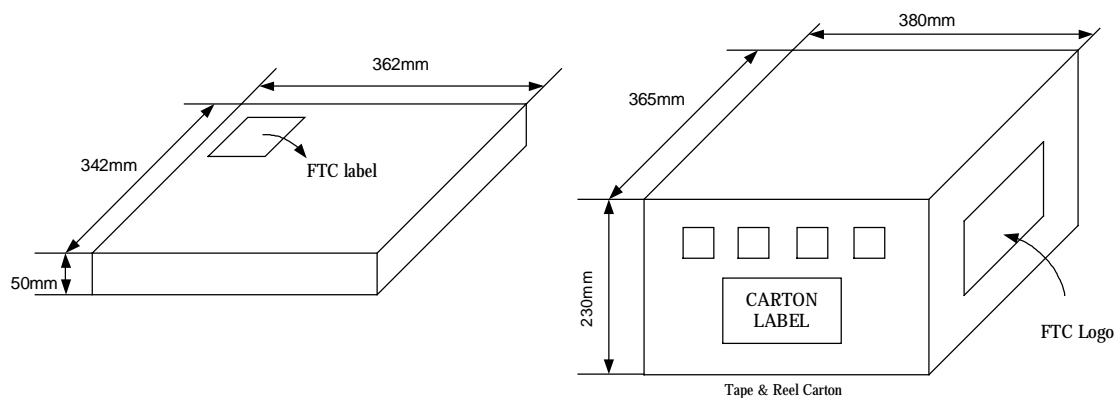
PACKING SPECIFICATIONS

BOX DIMENSION

TUBE INSIDE BOX AND CARTON



TAPE & REEL INSIDE BOX AND CARTON



PACKING QUANTITY SPECIFICATIONS

100 EA / TUBE	2500 EA / REEL
100 TUBES / INSIDE BOX	4 INSIDE BOXES / CARTON
4 INSIDE BOXES / CARTON	

LABEL SPECIFICATIONS

TAPPING & REEL

Feeling Technology Corp.	
Product	FP103
Lot No	A3311C62
D/C	4Xx-XXL
Q'ty	◎~◎
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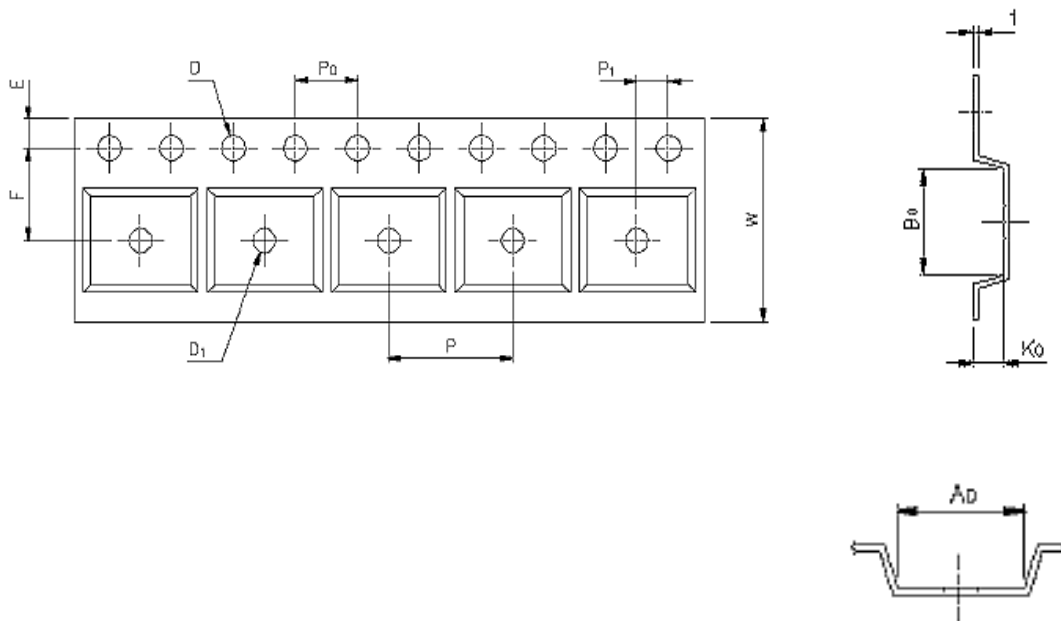
CARTON

Feeling Technology Corp.	
Product Type:	FP103
Lot No:	A3311C62
Date Code:	4Xx-XXL
Package Type:	SOP-8L
Marking Type:	Laser
Total Q'ty:	10,000
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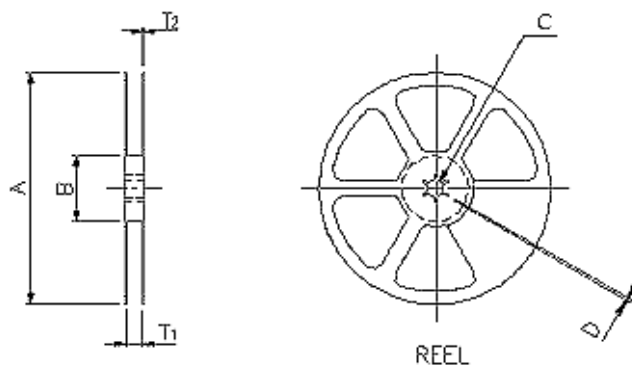
CARRIER TAPE DIMENSIONS

APPLICATION	W	P	E	F	D	D ₁
SOP8	12.0 ^{+0.3} _{-0.1}	8.0±0.1	1.75±0.1	5.5±0.1	1.55±0.1	1.5 ^{+0.25}

APPLICATION	P ₀	P ₁	A ₀	B ₀	K ₀	t
SOP8	4.0±0.1	2.0±0.1	6.4±0.1	5.20±0.1	2.1±0.10	0.30±0.013



REEL DIMENSIONS



APPLICATION	MATERIAL	A	B	C	D	T ₁	T ₂
SOP8	PLASTIC REEL	330±0.1	62±1.5	12.75±0.15	2±0.6	12.4±0.2	2.0±0.2