LD9174

05/09/2019

PWM+QR Multi-mode Controller with Primary Side Regulation

REV. 02

General Description

In order to enhance the efficiency performance, the LD9174 integrates the multi-mode PWM controller, which consists of Quasi-Resonant (QR) PWM control for light load condition and Continue Conduction Mode (CCM) for heavy load condition. Moreover, the QR controller gains the system performance, but also brings the worse EMI capability, especially at boundary mode in heavy load. While the frequency swapping function of LD9174 can reduce the EMI emission of SMPS and helps the power circuit designers to simply deal with EMI filter and saves several component and developing time.

The LD9174 is implemented in SOP-8 and SOP-7 package, and includes the comprehensive protection function, such as Over Load Protection (OLP), Over Voltage Protection (OVP), Output Short Circuit Protection (OSCP) and internal Over Temperature Protection (OTP). Furthermore, the programmable brown-in/out protection is built-in.

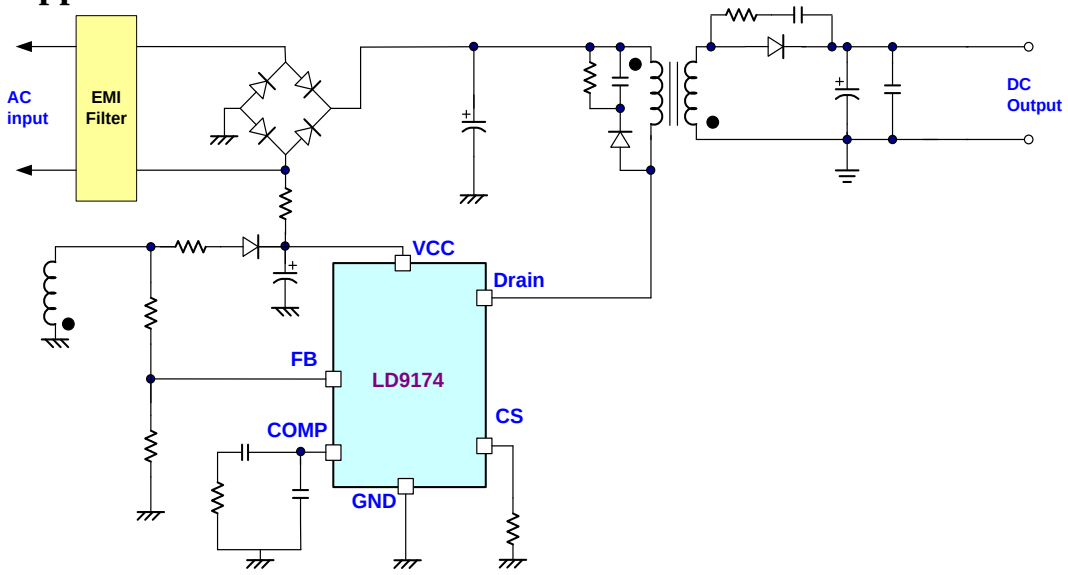
Features

- PSR CCM+QR Multi-Mode Control.
- Frequency Swapping for better EMI performance
- Low Startup Current (<1.5μA)
- Built-in load regulation compensation
- 75 kHz PWM switching frequency at Low Line
- Current mode control with cycle-by-cycle current limit
- UVLO (Under Voltage Lock Out)
- LEB (Leading-Edge Blanking) on CS pin
- VCC & FB OVP (Over Voltage Protection)
- SDSP (Secondary Diode Short Protection)
- Low line ripple compensation on FB pin
- Internal OTP (Over Temperature Protection)

Applications

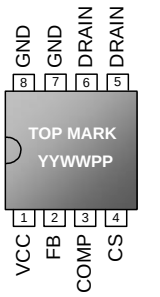
- Networking power supply
- Lower Power AC/DC Adaptor

Typical Application



Pin Configuration

SOP-8 (Top View)



YY: Year code
WW: Week code
PP: Production code

SOP-7 (Top View)

YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package	TOP MARK	Shipping
LD9174 GS	SOP-8	LD9174GS	2500 /tape & reel
LD9174 GR	SOP-7	LD9174GR	2500 /tape & reel

The LD9174 is ROHS compliant/ green packaged.

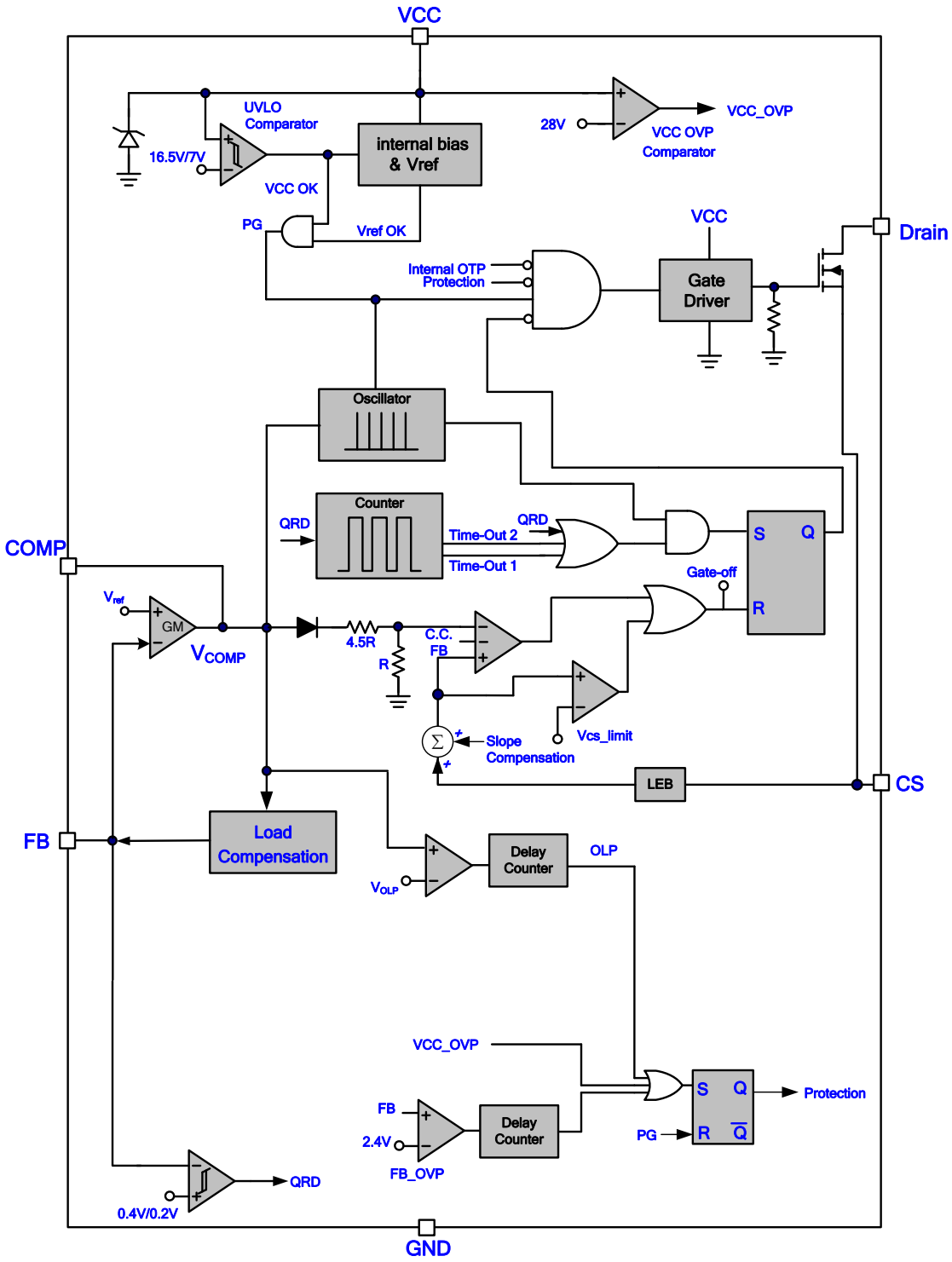
Protection Mode

Part number	Switching Frequency	VCC_OVP	FB_OVP	FB_O/S	OLP	SDSP
LD9174	75kHz@ Low Line	Auto recovery	Auto recovery	Auto recovery	Auto recovery	Auto recovery

Pin Descriptions

NAME	PIN (SOP-8)	PIN (SOP-7)	FUNCTION
VCC	1	1	Voltage supply pin
FB	2	2	Auxiliary voltage sense and quasi-resonant detection
COMP	3	3	Output of the error amplifier for voltage compensation.
CS	4	4	Current sense pin
DRAIN	5,6	5,6	The drain of internal power MOSFET
GND	7,8	8	Ground

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	32V
DRAIN	-0.3V~650V
FB, CS, COMP	-0.3V~6.0V
Maximum Junction Temperature	150°C
Continuous drain current (Tc=25℃)	2.5A
Pulsed drain current (Tc=25℃)	4A
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8/SOP-7, θ_{JA})	106°C/W
Package Thermal Resistance (SOP-8/SOP-7, θ_{JC})	20°C /W
Power Dissipation (SOP-8/SOP-7, Ta = 85°C)	377mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (DRAIN pin is exclusive)	2.5 KV
ESD Voltage Protection, Machine Model (DRAIN pin is exclusive)	250 V

Note1: The value of θ_{JA} is measured with the device mounted on 1oz one layer FR-4 board, in a still air environment with TA = 25°C. The value in any given application depends on the user's specific board design.

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
VCC voltage	12	16	V
VCC capacitor	4.7	10	μF
COMP Capacitor	680	2200	pF
Start-up resistor Value (AC Side, Half Wave)	400K	2M	Ω

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=12.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)						
Startup Current	VCC=UVLO-ON-0.05V*	I_{CC_ST}			1.5	μA
Operating Current	V_{COMP}=0V*	I_{CC_OP}		0.35	0.7	mA
	V_{COMP}=3.5V	I_{CC_OP2}	0.75	1.5	2.25	mA
	Auto current protection	I_{CC_OPA1}	0.4	0.8	1.2	mA
UVLO (OFF)		V_{CC_OFF}	6.5	7.0	7.5	V
UVLO (ON)		V_{CC_ON}	15.5	16.5	17.5	V
VCC OVP Level		V_{CC_OVP}	26.5	28	29.5	V
VCC OVP de-bounce time	*	N_{VCC_OVP}		6		Cycle
QRD (Quasi Resonant Detection, FB Pin)						
Reference Voltage, V_{REF}		V_{REF}	1.98	2.00	2.02	V
Load Compensation Current		I_{LOAD_COMP}	8.1	9	9.9	μA
Low line ripple compensation current level	The compensation starts, When i_{FB}< i_{FB_LLRC}*	i_{FB_LLRC}		96		μA
Current Sense (CS Pin)						
Maximum Input Voltage	Low Line	V_{CS_MAX}	0.9	1	1.1	V
Maximum Input Voltage	High Line*	V_{CS_MAX}		0.8		V
Minimum V_{CS}-off	Low Line	$V_{CS\_MIN\_L}$	0.12	0.145	0.17	V
Leading Edge Blanking Time	*	t_{LEB}		450		ns
Internal Slope Compensation	T_{ON}>1.5μs to T_{ON_MAX}. (Linearly increase)*	V_{SLP_L}		225		mV
Oscillator for Switching Frequency						
CCM Frequency	Low Line	F_{CCM}	67	75	83	kHz
Minimum Frequency		F_{S_MIN}	300	350	400	Hz
Maximum On Time	*	T_{ON_MAX}	10	12	14	μs
Soft Start						
Soft Start Time	Vcs-off from 0.5V to $V_{CS\_MAX(OFF)}$*	t_{SS}		5		ms
FB OVP (Feedback Over Voltage Protection)						
FB Over Voltage Protection	*	V_{FB_OVP}		2.4		V

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Open Loop Protection						
OLP Trip Level	*	V_{OLP}		4.5		V
OLP delay time	After soft-start*	T_{D_OLP}		65		ms
SDSP (Secondary Diode Short Protection)						
SDSP CS Pin Level	Secondary diode short*	V_{CS_SDSP}		1.2		V
De-bounce Cycle	*	T_{D_SDSP}		4		Cycle
Internal OTP (Over Temperature)						
OTP Level	*	T_{OTP}		145		°C
OTP Hysteresis	*	T_{OTP_HYS}		22		°C
MOSFET Drain (DRAIN Pin)						
Breakdown Voltage		V_{DS}	650			V
On Resistance		R_{DS_ON}		1.4	1.82	Ω

*: Guaranteed by design.

Typical Performance Characteristics

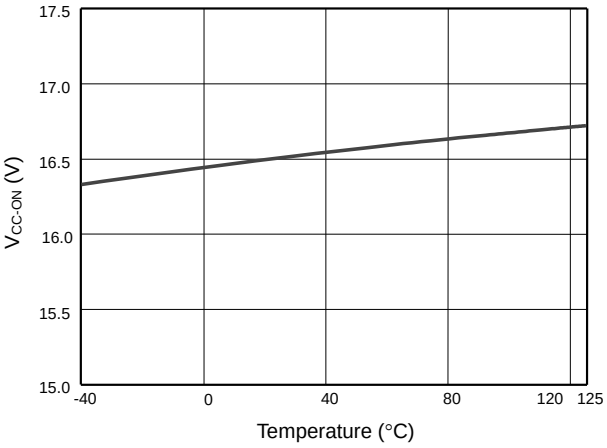


Fig. 1 UVLO (on) vs. Temperature

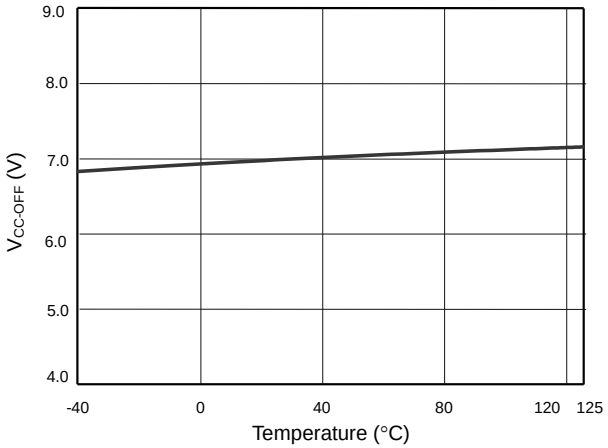


Fig. 2 UVLO (off) vs. Temperature

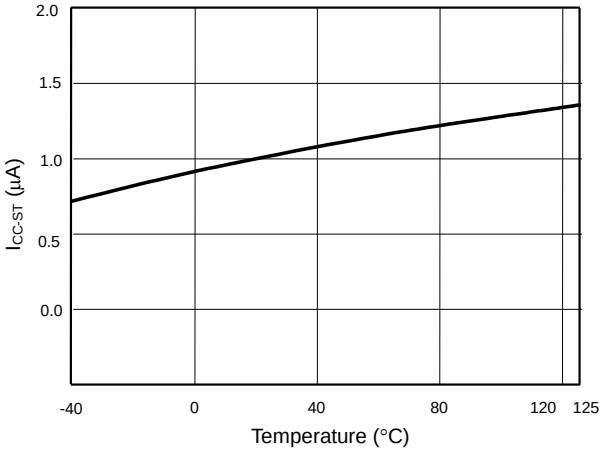


Fig. 3 Startup Current vs. Temperature

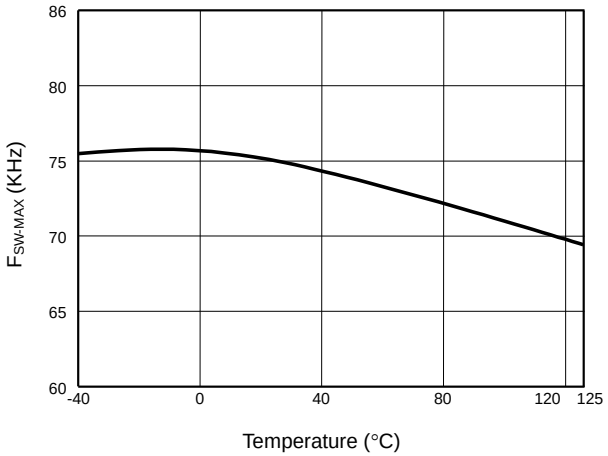


Fig. 4 Max Frequency vs. Temperature

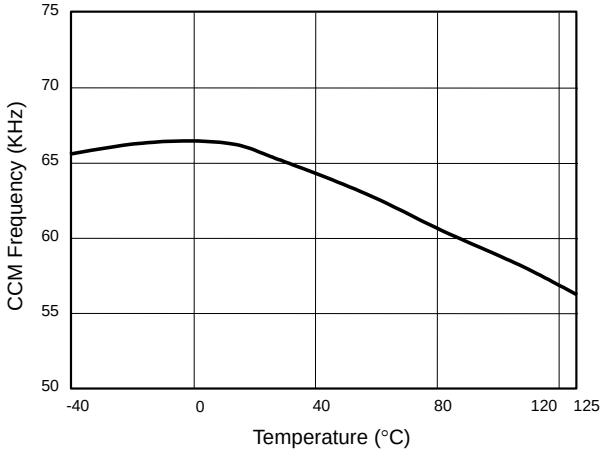


Fig. 5 CCM Frequency vs. Temperature

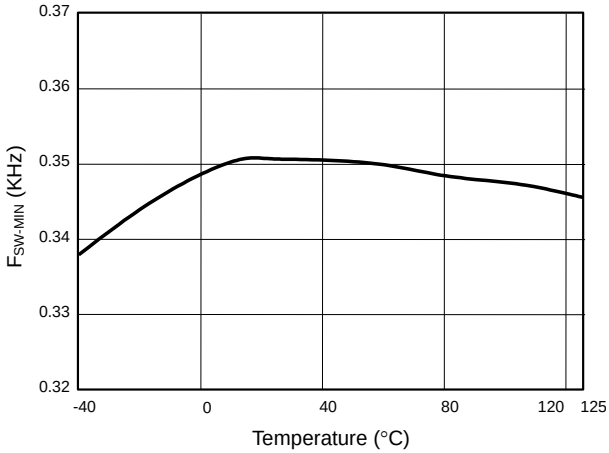


Fig. 6 Min Frequency vs. Temperature

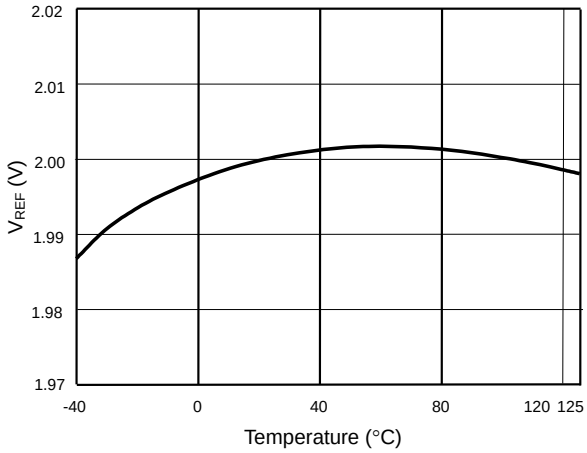


Fig. 7 Reference Voltage vs. Temperature

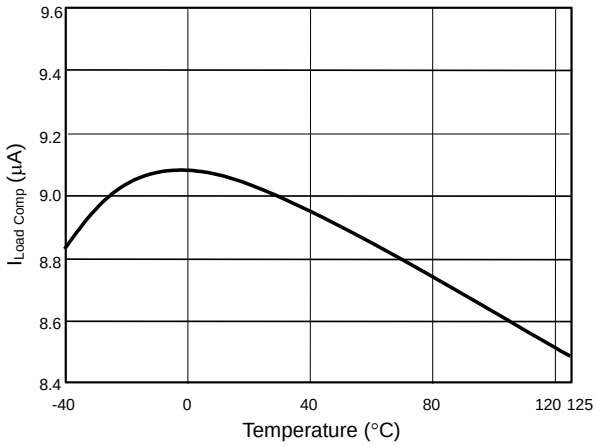


Fig. 8 Load Compensation vs. Temperature

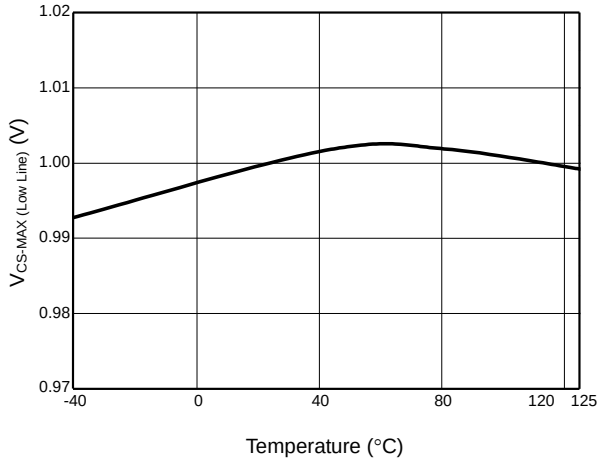


Fig. 9 V_{CSMAX} (Low Line) vs. Temperature

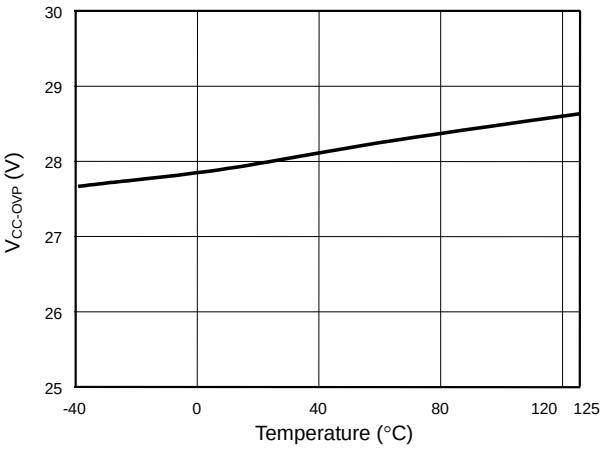


Fig. 10 VCC OVP vs. Temperature

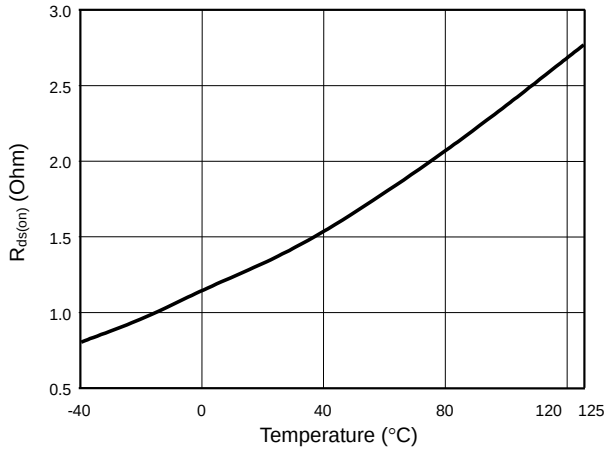


Fig. 11 $R_{ds(on)}$ vs. Temperature

Application Information

Operation Overview

The LD9174 is an excellent primary side feedback controller with quasi-resonant operation to provide high efficiency. The LD9174 removes the need for secondary feedback circuits while achieving excellent line and load regulation. It meets the green-power requirement and is intended for the use in those modern switching power suppliers and linear adaptors that demand higher power efficiency and power-saving. It integrates with more functions to reduce the external components counts and the size. Major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage across VCC pin. It would assure the supply voltage enough to turn on the LD9174 and further to drive the power MOS. As shown in Fig. 12, a hysteresis is built in to prevent shutdown from voltage dip during startup.

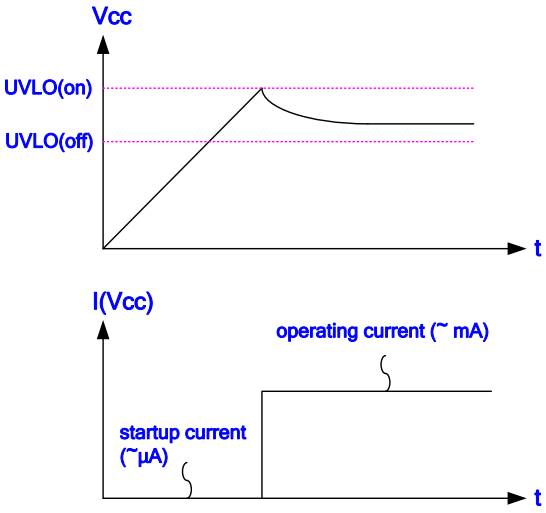


Fig. 12

Startup Current and Startup Circuit

The typical startup circuit to generate VCC of the LD9174 is shown in Fig. 13. At startup transient, the VCC is below the UVLO(ON) threshold, so there's no pulse delivered out from LD9174 to drive the power MOS. Therefore, the current through R_{START} will be used to charge the capacitor C1. Until the VCC is fully charged to deliver the drive-out signal, the auxiliary winding of the transformer will provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R_{START} and then reduce the power consumption on R_{START}. By using CMOS process and some unique circuit design, the LD9174 requires only 1.5μA max to start up. Higher resistance of R_{START} will spend much more time to start up. The user is recommended to select proper value of R_{START} and C1 to optimize the power consumption and startup time.

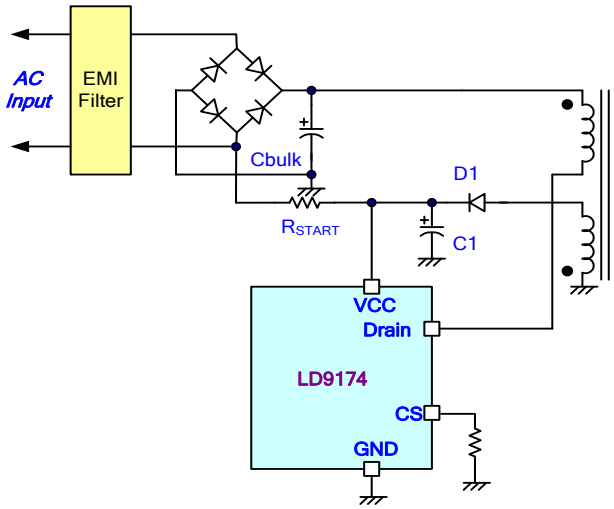


Fig. 13

Principle of CV Operation

In this primary side regulation converter, it can sense the output voltage from auxiliary winding. LD9174 samples the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig. 14. The voltage induced in the auxiliary winding is a reflection of the secondary winding voltage while the MOS is in off state. Via a resistor divider connected between the auxiliary winding and FB pin, the auxiliary voltage is sampled after the sample delay time which is defined as 34~42% of

secondary current discharge time from previous cycle. And will be hold until the next sampling period. The sampled voltage is compared with an internal reference V_{REF} (2.00V) and the error will be amplified. The error amplifier output COMP reflects the load condition and controls the duty cycle to regulate the output voltage, thus constant output voltage can be achieved. The output voltage is given as:

$$V_{OUT} = 2.00V(1+\frac{Ra}{Rb})(\frac{N_S}{N_a}) - V_F$$

Where V_F indicates the drop voltage of the output diode, Ra and Rb are top and bottom feedback resistor value, Ns and Na are the turns of transformer secondary and auxiliary.

In case that the output voltage is sensed through the auxiliary winding; the leakage inductance will induce ringing to affect output regulation. To optimize the collector voltage clamp circuit will minimize the high frequency ringing and achieve the best regulation. Fig. 15 shows the voltage waveform of drain to source in compare to those with large undershoot due to leakage inductance induced ring (Fig. 16). The ringing may make the sample error and cause poor performance for output voltage regulation. A proper selection for resistor R_S which in series to the clamp diode, may reduce any large undershoot, as shown in Fig. 14.

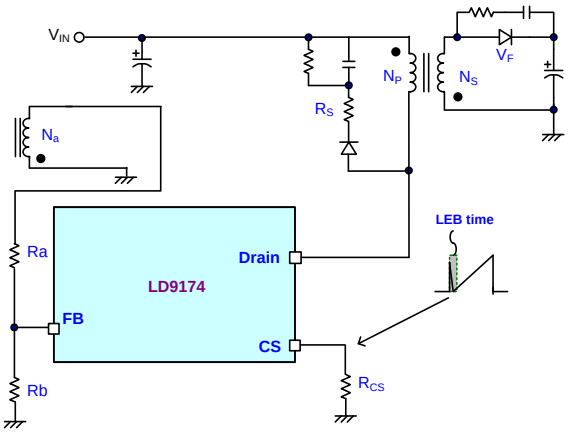


Fig. 14

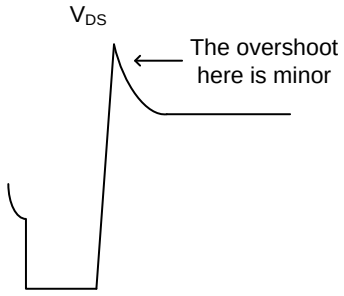


Fig. 15

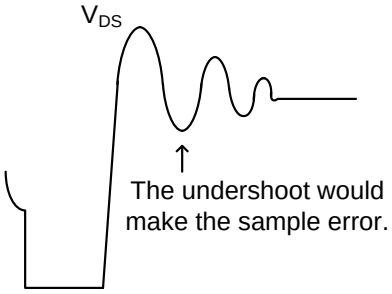


Fig. 16

Load Regulation Compensation

LD9174 is implemented with load regulation compensation to compensate the cable voltage drop and to achieve a better voltage regulation. The offset voltage across FB is produced by the internal sink current source during the sampling period. The internal sink current source is proportional to the value of over load current to compensate the cable loss as shown in Fig. 17. So, the offset voltage will decrease linearly and smoothly as the output current decreases from full-load to no-load. It is programmable by adjusting the resistance of the voltage divider to compensate the drop for cable lines used in various conditions. The equation of internal sink current is shown as:

$$I_{LOAD\_COMP} = 9 \times \frac{I_{RATED}}{I_{OLP}} (\mu A)$$

where

The I_{RATED} means the output current in rated.

The I_{LC} is calculated current of load compensation.

The I_{OLP} means the over load protection current.

For Networking used to set the I_{OLP}=130%~150%×I_O

The compensation current versus I_O is shown as:

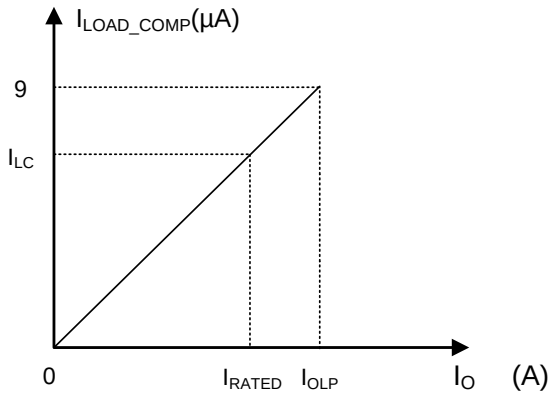


Fig. 17

Oscillator and Switching Frequency

The LD9174 is implemented with frequency swapping function which helps the power supply designers to both optimize EMI performance and lower system cost.

Quasi-Resonant Mode Detection

The LD9174 employs quasi-resonant (QR) switching scheme to switch in valley-mode either in CV or CC operation. This will greatly reduce the switching loss and the ratio dv/dt in the entire operating range for the power supply. Fig. 18 shows the typical QR detection block. The QR detection will detect auxiliary winding signal to drive MOS as FB pin voltage drops to 0.2V. The QR comparator will not activate if FB pin voltage remains above 0.4V.

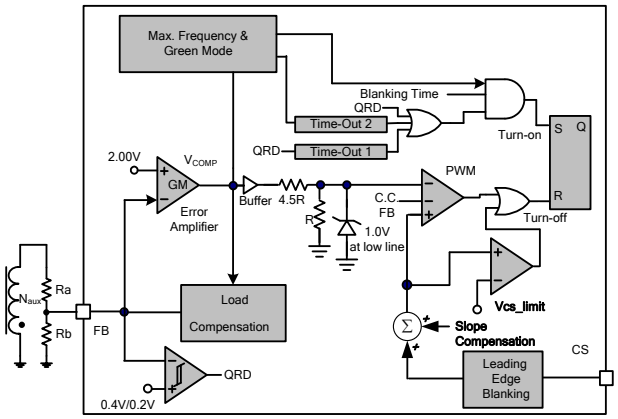


Fig. 18

Multi-Mode Operation

The LD9174 is a QR+CCM controller operating in multi-modes. The controller changes operation modes according to line voltage and load conditions. At heavy-load, there might be two situations to meet. If the system AC input is in low line, for better performance in low line ripple and decrease primary side peak current, the LD9174 will turn on in CCM-Mode with CCM frequency 75 kHz. If in high line, the switching frequency will decrease to 65 kHz, in this state, the controller will work in QR mode or skip the first valley to turn on in 2nd, 3rd….valley. The switching frequency would vary depending on the line voltage and the load conditions when the system is operated in multi-mode. The most specially is the switching frequency would rise to up to 100 kHz due to the low line ripple.

At medium load conditions (operation frequency about 25 kHz ~ 75 kHz in low line), the frequency is clamped between green mode frequency and maximum frequency. However, the characteristic in valley switching behaves will without problem in this condition. The LD9174 will turn on in 4th, 5th…. Valley. That is, when the load decreases, the system will automatically skip some valleys and the switching frequency is therefore reduced. A smooth frequency fold-back and high power efficiency are then

achieved. Also the light load condition, makes the switching frequency decreases to 25 kHz, the better efficiency is achieved equally.

At zero load or very light load conditions, the system operates in minimum frequency for power saving. The system modulates the frequency according to the load conditions.

Current Sensing and Leading-Edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 14, the LD9174 detects the primary MOS current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 1.0V in low line, 0.8V in high line. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{1.0V}{R_{CS}} \quad \text{At Low Line}$$

$$I_{PEAK(MAX)} = \frac{0.8V}{R_{CS}} \quad \text{At High Line}$$

A leading-edge blanking (LEB) time about 450ns is included in the input of CS pin to prevent the false-trigger from the turn-on current spike.

High/Low Line Detection

LD9174 has setting the high/low line detect voltage through (Ra), assume that V_{HL_H} is the boundary voltage between high/low line detect level. The equation of Ra is shown as:

$$R_a = \frac{V_{HL\_H} \times \sqrt{2} \times \frac{N_a}{N_P}}{220\mu A}$$

The low line current as 200μA, according to the Ra value the C.C. compensation will adjust at different lines voltage.

Principle of C.C. Operation

The primary side control scheme is applied to eliminate secondary feedback circuit or opto-coupler, which will reduce the system cost. The switching waveforms are shown in Fig. 19. The output current "Io" can be expressed as:

$$I_O(A) = \frac{i_{S,M} \times T_{DIS}}{T_S} = \frac{N_P}{N_S} \times i_{P,M} \times \frac{T_{DIS}}{T_S} = \frac{N_P}{N_S} \times \frac{V_{CSM}}{R_{CS}} \times \frac{T_{DIS}}{T_S}$$

The primary mean current ($i_{P,M}$), The secondary mean current ($i_{P,M}$), inductor current discharge time (T_{DIS}) and switching period (T_S) can be detected by the IC. The ratio of $V_{CSM}*T_{DIS}/T_S$ will be modulated as a constant ($V_{CSM}*T_{DIS}/T_S = I_{CC}=1/4$), so that I_O can be obtained as

$$I_O(A) = \frac{N_P}{N_S} \times \frac{V_{CSM}}{R_{CS}} \times \frac{T_{DIS}}{T_S} = \frac{N_P}{N_S} \times \frac{I_{CC}}{R_{CS}}$$

However this is an approximate equation. The user may fine-tune it according to the experiment result.

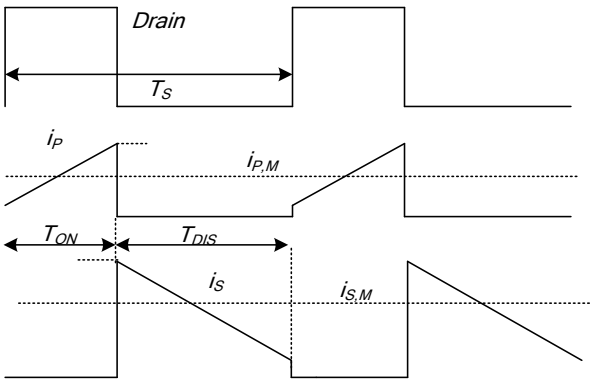


Fig. 19

OVP (Over Voltage Protection) on VCC – Auto Recovery

LD9174 is implemented with OVP function through VCC. As the VCC voltage rises over the OVP threshold voltage, the output drive circuit will be shut off simultaneously thus to stop the switching of the power MOS until the next UVLO (ON) arrives. The VCC OVP function of LD9174 is an auto-recovery type protection. The Fig. 20 shows its operation. That is, if the OVP condition is removed, it will resume to normal output voltage and VCC level in normal condition.

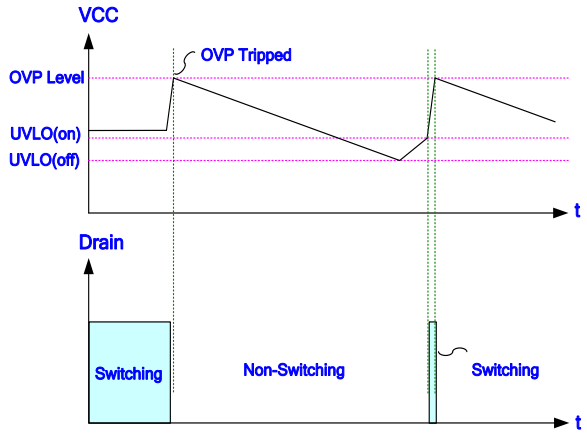


Fig. 20

Over Load Protection (OLP) & FB Short Circuit Protection – Auto Recovery

LD9174 is implemented with OLP function. LD9174 features auto recovery function of it. In the example of the fault condition, the feedback system will force the voltage loop enter toward the saturation. As the built in V_{COMP} tripped pull high level and stay for more than the OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit. The OLP delay time is set by internal high frequency counter. It is to prevent the false triggering from the power-on and turn-off transient. In soft start period, the Fig. 21 shows the operation. While FB is short to GND, FB pin keeps in zero voltage level. If FB cannot detect any voltage signal over 0.2V in the beginning of soft start period, then the soft start will turn to generate a driving signal and keep auto recovery until FB short remove.

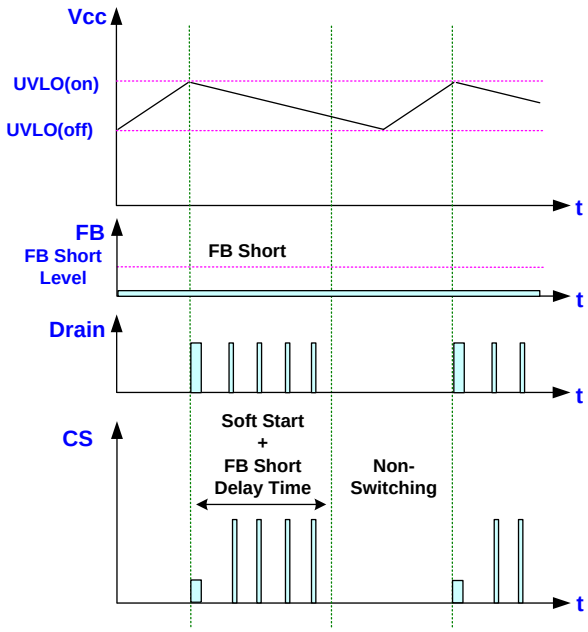


Fig. 21

Over Voltage Protection on FB Pin (FB OVP) – Auto Recovery

An output overvoltage protection is implemented in the LD9174. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R_b, refereeing to Fig. 22. If V_{FB} overs the FB OVP trip level, the internal counter starts counting 6 cycles, and then LD9174 goes to auto-recovery protection mode till the FB OVP status is defused.

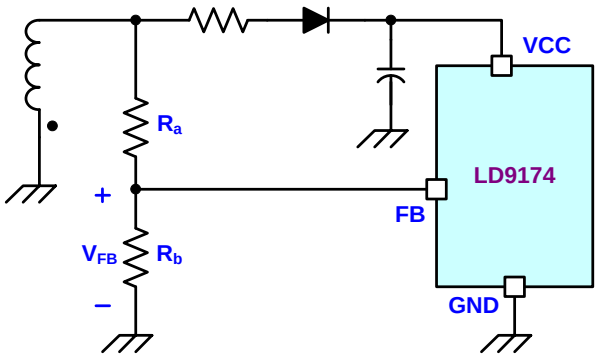


Fig. 22

Secondary Diode Short Protection (SDSP) – Auto Recovery

The logic of SDSP is described briefly as follows. If VCS is higher than 1.2V, the count is up to 4 times in 20ms. Its gate will be turned-off, shown as Fig. 23.

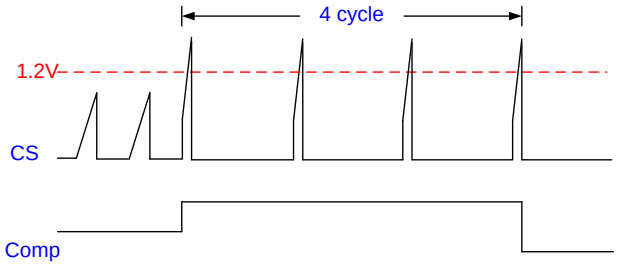


Fig. 23

PCB Layout Guideline – Power GND & Signal GND

As shown in Fig. 24. The orange power ground path should be wide enough and keep away from low voltage path. The ground of auxiliary winding through FB resistor ground and a low voltage signal as COMP loop should return IC ground to avoid antenna effect, and makes the loop as small as possible. The trace between GND of VCC capacitor and the bulk capacitor ground should be as wide and short as possible. The snubber circuit needs to shorten the loop and tries to avoid getting close to the low voltage loop, which is presented in blue line. Finally, the VCC ground is back to bulk cap ground as shown in green line.

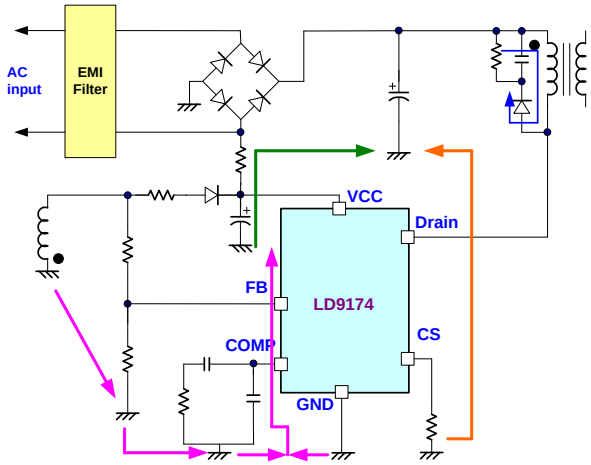


Fig. 24

Low Line Ripple Compensation

According to the bulk voltage is not steady dc level, it waves with ac frequency. The bulk valley voltage shows up when output in heavy load and voltage will also affect by bulk capacitor tolerance. The voltage get lower when more tolerance or lower ac frequency. These will let the output ripple noise become waving; therefore the LD9174 built in low line ripple compensation function. that shown as Fig 25, in turn time use iFB current as a input voltage variation information, in turn off time offer more iFB from FB pin to compensates the Vbulk valley, when low line ripple noise becomes obviously, we could adjust Ra to change compensation level and reduce ripple noise.

$$V_{LLRC} = R_a \times iFB_{LLRC}$$

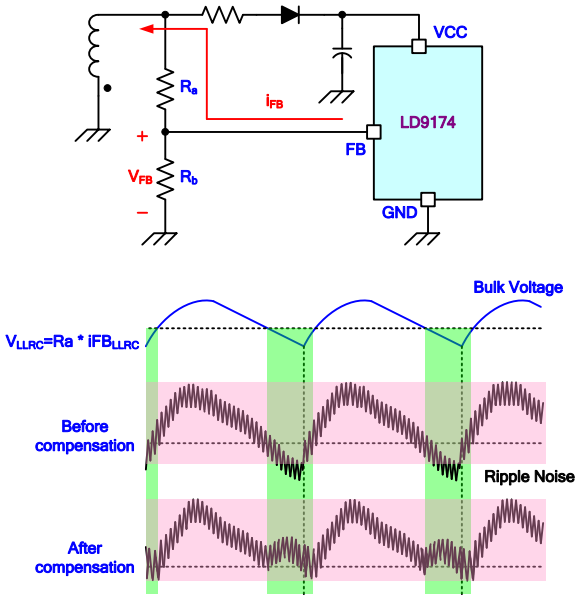
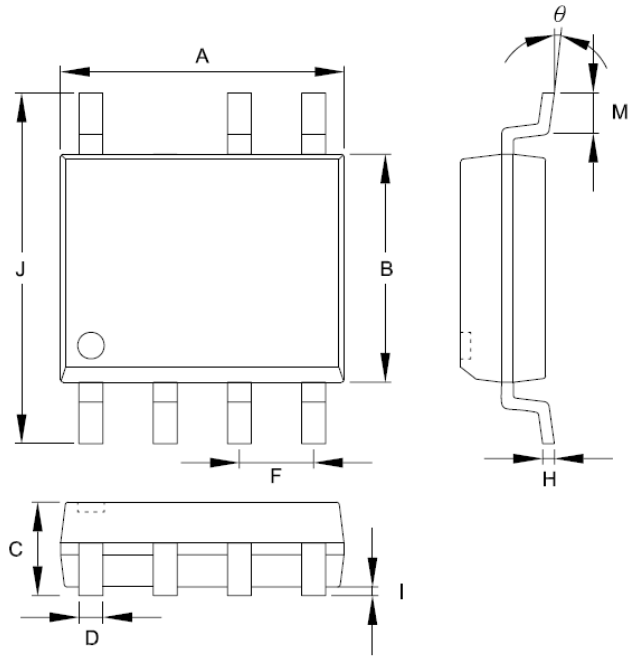

VCC
Ra
iFB
LD9174
FB
+
VFB
Rb
–
GND
Bulk Voltage
VLLRC=Ra * iFBLLRC
Before compensation
Ripple Noise
After compensation

Fig. 25

Package Information

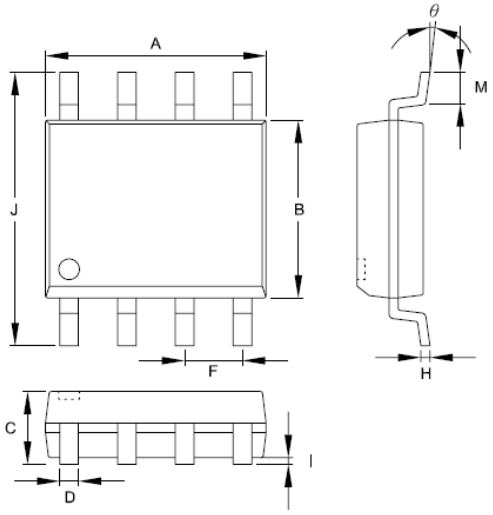
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
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H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

REV.	Date	Change Notice
00	11/01/2016	Original Specification
01	10/17/2018	Add $R_{DS(ON)}$ =1.82Ω.
02	05/09/2019	1. Revise the internal OTP from 150℃ to 145℃, and add application note of low line ripple compensation. 2. Revise maximum on time lower limit from 10.8μs to 10μs, upper limit from 13.2μs to 14μs.