Transition-Mode PFC and Quasi-Resonant Current Mode PWM Controller

REV: 00

General Description

The LD7792S is the enhancement version of the LD7790, the audible noise produced during start-up & light load is greatly reduced and the THDi is also further improved. LD7792S features transition mode Power Factor Correction (PFC) controller and Quasi-Resonant (QR) current mode controller for cost effective and fewer external components design of high power application.

The intelligent PFC switching on/off, zero current detection (ZCD) and frequency limitation mechanism enable a better efficiency under any load conditions.

The device is also integrated several functions of protection, such as X-CAP discharge, brown-in/out protection, Over Load protection (OLP), Over Temperature Protection (OTP), Over Voltage Protection (OVP) and Over Current Protection (OCP) with high / low line compensation. Therefore it can protect the system from damage due to occasional failure.

The LD7792S is available in a SOP-16 package.

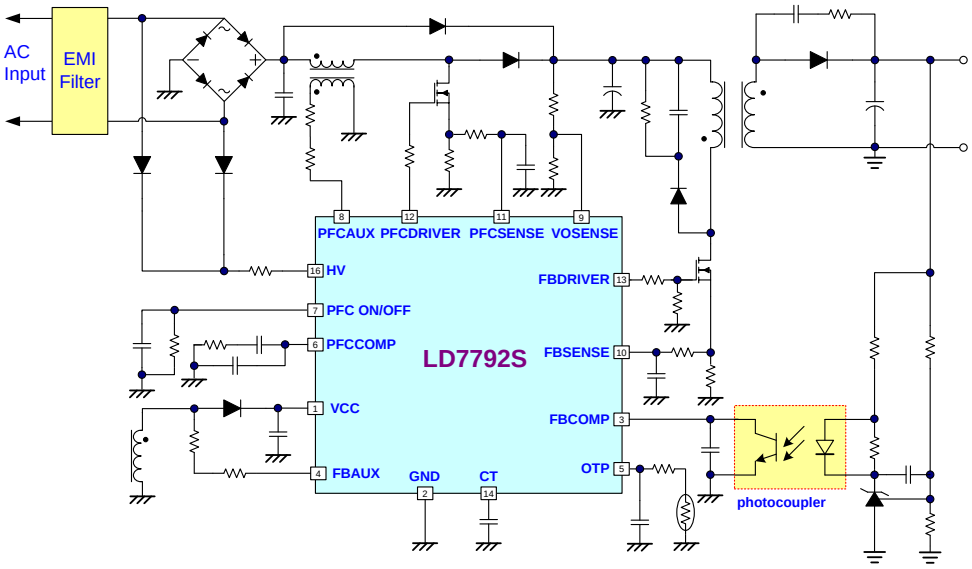
Features

- Integrated PFC and QR or PWM Flyback Controller
- Transition mode operation for PFC
- Quasi-resonant operation for Flyback
- Built-in X-CAP discharging
- Brown in/out protection
- Internal soft start function
- Adjustment OLP debounce time
- PFC light load turn-off control
- OVP (Over voltage protection)
- OCP (Cycle by cycle current limiting)
- 500/-1000mA driving capability
- Internal OTP function
- External OTP protection

Applications

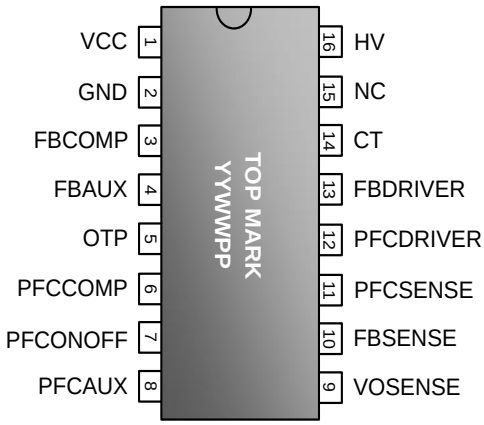
- LED lighting

Typical Application



Pin Configuration

SOP-16 (TOP VIEW)



YY： Year code
WW： Week code
PP： Production code

Ordering Information

Part number	Package	Top Mark	Shipping
LD7792S GS	SOP-16	LD7792S GS	2500 /tape & reel

The LD7792S is ROHS compliant/ green packaged.

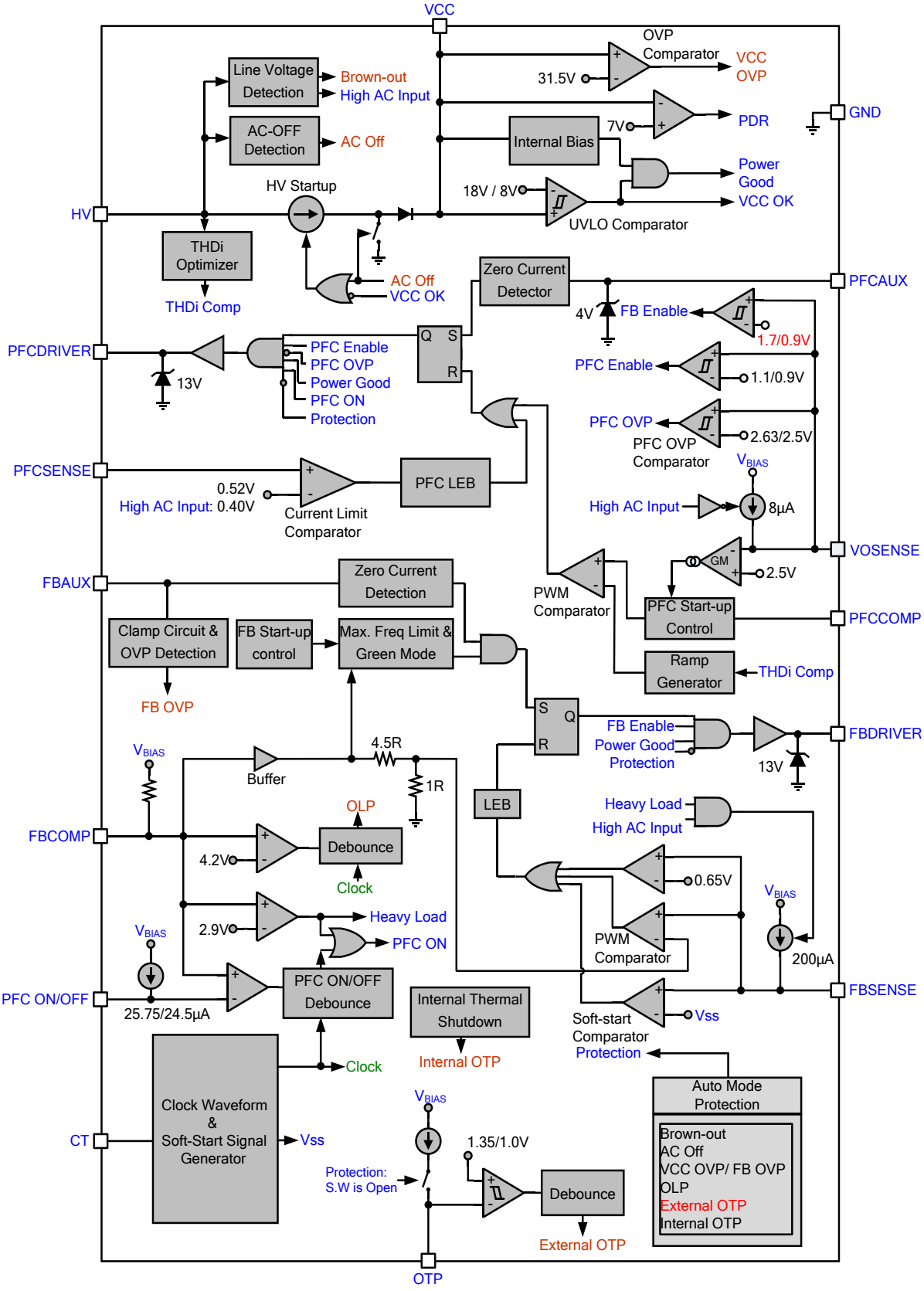
Protection Mode

Part number	OVP (VCC & FBAUX)	OLP	External OTP	Internal OTP
LD7792S GS	Auto recovery	Auto recovery	Auto recovery	Auto recovery

Pin Descriptions

Pin	NAME	FUNCTION
1	VCC	Supply voltage pin.
2	GND	Ground.
3	FBCOMP	Voltage feedback pin for Flyback stage. Connect a photo-coupler to close the control loop and achieve the regulation.
4	FBAUX	Zero current detection and over voltage protection for Flyback unit
5	OTP	External OTP protection pin.
6	PFCCOMP	Output of the error amplifier for PFC voltage loop compensation.
7	PFCONOFF	Threshold voltage setting of FBCOMP for PFC ON/OFF loading control.
8	PFCAUX	Zero current detection for PFC unit.
9	VOSENSE	Voltage sense for PFC output, regulation voltage is 2.5V.
10	FBSENSE	Current sense pin. Connect it to sense the Flyback MOSFET current.
11	PFCSENSE	Current sense pin. Connect it to sense the PFC MOSFET current.
12	PFCDRIVER	Gate drive output to drive the external MOSFET for PFC unit.
13	FBDRIVER	Gate drive output to drive the external MOSFET for Flyback unit.
14	CT	Timer setting for Open Loop Protection, PFC light-load turn-off and Flyback soft-start.
15	NC	Unconnected Pin.
16	HV	Connect this pin to Line/Neutral of AC main voltage through a resistor to provide the startup current for the controller. When VCC voltage increases to trip the point of UVLO(on), this HV loop will be turned off to reduce the power loss over the startup circuit. HV pin Internal circuit will detect the AC peak voltage, providing Brown in/out and High / Low Line Detection function. HV pin internal circuit will discharge X-cap's energy through HV current source when AC line is disconnected.

Block Diagram



Absolute Maximum Ratings

VCC	-0.3V ~ 35V
HV	-0.3V ~ 650V
FBCOMP, PFCCOMP, FBSENSE, PFCSENSE, FBAUX, PFCAUX, VOSENSE, LATCH, CT, PFCONOFF	-0.3V ~ 6V
FBDRIVER, PFCDRIVER	-0.3V ~ 20V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C ~ 150°C
Power Dissipation (SOP-16, at Ambient Temperature = 85°C)	363mW
Package Thermal Resistance (SOP-16, θ_{JA})	110°C/W
Package Thermal Resistance (SOP-16, θ_{JC})	36°C/W
Lead Temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model, (Pin 3~11 & Pin 14)	3.5KV
ESD Voltage Protection, Human Body Model, (Pin 1, 12, 13)	2.5KV
ESD Voltage Protection, Human Body Model, (Pin 16)	1.0KV
ESD Voltage Protection, Machine Model (except HV Pin)	250V

Note:

When FBSENSE, PFCSENSE, PFCAUX pin voltage< 0V ~ -0.7V, the current of FBSENSE, PFCESNSE and PFXAUX must be ≦ 20mA and t ≦ 200ns.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply Voltage VCC	10	29	V
VCC Capacitor Value	22	100	μF
HV Pin Resistor Value	2.2	20	kΩ
HV Pin Capacitor Value	10	330	pF
PFCCOMP Capacitor Value	0.1	2.2	μF
FBCOMP Capacitor Value	1	100	nF
VOSENSE Capacitor Value	-	10	nF
PFCAUX Pin Resistor Value	10	51	kΩ
PFCAUX Current Setting	-	1.5	mA
OTP Capacitor Value	4.7	100	nF

Note:

1. It's essential to connect COMP pin with a capacitor to filter out the undesired switching noise for stable operation.
2. Place the small signal components closed to IC pin as possible.

Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)						
High-Voltage Current Source for VCC Startup	VCC < PDR, VHV = 80V	I_{HV1}	1.00	1.50	2.00	mA
	VCC > PDR, VHV = 80V	I_{HV3}	2.0	3.0	4.0	mA
Off-State Leakage Current	After UVLO(on), VHV = 500V	$I_{HVOFF500}$			32	μA
Line Voltage Detection (HV Pin)						
X-Cap Discharge Current	*	I_{HVXCAP}		3		mA
Brown-in Level		V_{BNI}	95	105	115	V
Brown-out Level		V_{BNO}	79	85	91	V
Brown-in – Brown-Out Level	*	V_{BNHYS}		20		V
Brown-Out Debounce Time	*	T_{DBNO}		575		ms
High Line Trip Level		V_{HLINE}	215	230	245	V
Low Line Trip Level		V_{LLINE}	195	210	225	V
High Line Threshold - Low Line Level		V_{LINHYS}	10	20		V
Supply Voltage (VCC Pin)						
Holding Current Before UVLO (on)	VCC < UVLO (on)	I_{VCCST}		150		μA
	VCC < UVLO (on), VLATCH = 0V	I_{VCCLCH}		300		μA
Operating Current	VFBCOMP = 0V, PFC & Flyback OFF	I_{VCCBST}			1.3	mA
	VFBCOMP = 3V, PFC & Flyback ON	I_{VCC3}			2	mA
UVLO (off)	(-20°C ~125°C)	V_{UVOFF}	7.5	8.0	8.5	V
UVLO (on)	(-20°C ~125°C)	V_{UVON}	17.0	18.0	19.0	V
VCC OVP Level		V_{CCOVP}	30.5	31.5	32.5	V
VCC OVP De-bounce Time	*	$T_{DVCCOVP}$		64		μs
Power Down Reset Voltage (PDR)		PDR	6	7	8	V
PFC ON/OFF Control (PFCONOFF pin)						
Source Current for PFC OFF Threshold Setting		I_{PFCOFF}	23	24.5	26	μA
Source Current for PFC ON Threshold Setting		I_{PFCON}		25.75		μA

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PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
PFC OFF & Open Loop Protection Debounce Timer Setting (CT Pin)						
FB OLP Debounce Time on Flyback unit	CT=0.047μF, VFBCOMP > VOLP, after start-up, 4HICUPPS	T_{DOLP}		64		ms
	CT=0.047μF, VFBCOMP > VOLP, at start-up *, 4HICUPPS	T_{DOLPST}		74		ms
Soft Start Time on Flyback unit	*; CT=0.047μF , VOSENSE >1.7V	T_{FBSS}		10		ms
OSCP Debounce Time on Flyback unit	CT=0.047μF, VFBCOMP > VOLP, VCC = UVLO (off) + 2V, after start-up, 4HICUPPS	T_{DOSCP}		16		ms
PFC Turn-off Debounce Time	VFBCOMP < VPFC ON/OFF, CT=0.047μF	$T_{DPFCOFF}$		1		s
External OTP (OTP Pin)						
OTP Pin Source Current		I_{OTP}	75	80	85	μA
Turn-On Trip Level		V_{OTPON}	1.30	1.35	1.40	V
Turn-Off Trip Level		V_{OTPOFF}	0.95	1.0	1.05	V
OTP pin de-bounce time*	Disable (High to Low)	$T_{DOTPOFF}$	400	500	600	μs
PFC Output Voltage Sensing (VOSENSE pin)						
Reverence Input Voltage, V_{REF}	T_J=-20°C ~125°C	V_{FBREF}	2.47	2.50	2.53	V
PFC OVP Trip Level		V_{PFCOVP}	2.59	2.63	2.67	V
	OVP Hysteresis	$V_{PFCOVPHYS}$	0.115	0.130	0.145	V
	Debounce time *	$T_{DPFCOVP}$		50		μs
Source Current of VOSENSE	VHV_{PEAK} = 150V	$I_{FOLBTLV}$		8		μA
	VHV_{PEAK} = 250V	$I_{FOLBTHV}$		0.1		μA
Enable and Disable Threshold Voltage	PFC Enable Threshold	V_{PFCEN}	1.0	1.1	1.2	V
	PFC Disable Threshold	V_{PFCENL}	0.8	0.9	1.0	V
	Debounce Time *	T_{DPFCEN}		50		μs
VOSENSE Pull Down Resistance	*	$R_{VOSENSE}$	5	6	7	MΩ

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
PFC Error Amplifier (PFCCOMP Pin)						
Transconductance		GM	60	80	100	μmho
Output Upper Clamp Voltage	VOSENSE = V_{REF} -0.1V	$V_{PCOMPMAX}$	5.0	5.2	5.4	V
Output Minimum Clamp Voltage		$V_{PCOMPMIN}$		0.90		V
PFC Burst Mode	Trip Level for PFCDRIVER Stop	$V_{PCOMPOFF}$	0.95	1.00	1.05	V
	Trip Level for PFCDRIVER Start	$V_{PCOMPON}$	Threshold for PFCDRIVER stop + 50mV			V
PFC Maximum On-Time						
PFC Max. On-Time	*VHV=180V; FBCOMP≧ 1.5V	$T_{ONMAXPLV}$		13		μs
	*;VHV=250V;FBCOMP≧ 1.5V	$T_{ONMAXPHV}$		4.2		μs
PFC Minimum Off-Time						
PFC Minimum Off-Time	*	$T_{POFFMIN}$		1		μs
PFC Maximum Frequency						
PFC Maximum Frequency		F_{MAXPFC}	420	470	520	kHz
PFC Current Sensing (PFCSENSE Pin)						
Current Sense Input Threshold Voltage	VHV_{PEAK} = 150V	$V_{PFCCSLV}$	0.47	0.52	0.57	V
	*;VHV_{PEAK} = 250V	$V_{PFCCSHV}$	0.35	0.40	0.45	V
Leading Edge Blanking time	*	T_{LEBPFC}		250		ns
PFC Zero Current Detector (PFCAUX Pin)						
Upper Clamp Voltage	I_{PFCAUX} = 3mA	$V_{PFCAUXUC}$		4.0		V
PFC ZCD Trip Level		$V_{PFCAUXH}$		0.20		V
Delay from PFCAUX to Output *		$T_{DPFCZCD}$		200		ns
PFC ZCD Time Out	*; After PFCDRIVER Turn-off	T_{TOPFC}	35	50	65	μs
Flyback Comp Pin (FBCOMP Pin)						
Short Circuit Current	V_{COMP}=0V	$I_{FBCOMPSC}$		0.125		mA
Flyback Burst Mode	Trip Level for FBDRIVER Start	$V_{BSTONQR}$		0.8		V
	Trip Level for FBDRIVER Stop	$V_{BSTOFFQR}$		0.4		V
Heavy Load Trigger Level		$V_{IFBCSEN}$		2.9		V
Open Loop Voltage	FBCOMP pin open	V_{FBC}	5.2	5.4	5.6	V

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Over Load Protection (FBCOMP Pin)						
OLP Trigger Level (VOLP)		V_{OLP}	4.1	4.2	4.3	V
Output Short Circuit Protection						
VCC OSCP Trigger Level	*; VFBCOMP > VOLP	V_{CCOSCP}		UVLO (off) +2		V
Flyback OVP (FBAUX pin)						
OVP Trigger Current		$I_{FBAUXOVP}$	270	300	330	µA
Upper Clamp Voltage	IFBAUX = 0.3mA	V_{FBAUXH}	1.9	2.0	2.1	V
Debounce Cycle	*	$T_{DFBAUXOVP}$		4		FB PWM cycle
FBAUX OVP Detection Blanking Time	*;After FBDRIVER Turn-off	$T_{DFBOVPDET}$	1	2		µs
Zero Current Detection (FBAUX Pin)						
Lower Clamp Voltage	IFBAUX = -1mA	$V_{FBAUXLC}$	-0.3		0	V
Flyback ZCD Trip Level		V_{QRDLQR}		50		mV
Flyback ZCD Delay Time	*	T_{DFBZCD}		200		ns
Flyback ZCD Time Out1	After Max. Frequency	T_{O1QR}	4	5	6	µs
Minimum Flyback ZCD Time Out2	After FBDRIVER Turn-off	T_{O2QR}		300		µs
ZCD Blanking Time	After FBDRIVER Turn-off	$T_{OFFMINQR}$		2.0		µs
Oscillator for Switching Frequency						
Flyback Max. Frequency		F_{MAXQR}	78	85	92	kHz
Flyback Max. Frequency Mode Threshold, V_{FBCOMP}	*	$V_{FBCFMAX}$		2.2		V
Flyback Green Mode Frequency		$F_{GREENQR}$		6		kHz
Flyback Green Mode Threshold, V_{FBCOMP}	*	$V_{FBCGREEN}$		1.0		V
Flyback Maximum On Time		$T_{ONMAXQR}$	40	45	50	µs
Flyback Current Sensing (FBSENSE Pin)						
Threshold for Cycle by Cycle Current Limit, Vcs(off)	(-20°C ~125°C)	V_{OCQR}	0.62	0.65	0.68	V
Leading Edge Blanking Time	*	T_{LEBQR}		350		ns
Threshold Voltage Current Limit-2		V_{OC2QR}		1.03		V
Leading Edge Blanking Time of Current Limit-2	*; and 16 cycles into protection by 4 Hiccups	T_{LEBOC2}		250		ns

(T_A = +25°C unless otherwise stated, VCC=15.0V)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Flyback Current Sensing (FBSENSE Pin)						
OCP Compensation Current	VHV_{PEAK} = 250Vdc FBCOMP = 3V	I_{FBCSHV}	150	200	250	μA
Delay to Output	*	T_{DCS}		80		ns
PFC and Flyback Gate Drive Output (PFCDRIVER & FBDRIVER Pin)						
Output Low Level	VCC=15V, I_{SINK}=100mA	V_{OUTH1}	0		1.5	V
Output High Clamp Level	VCC=17V	V_{OUTCL}	11	13	15	V
Rising Time	*;V_{CC} =15V,CL=3000pF	T_{OUTR}		130		ns
Falling Time	*;V_{CC} =15V,CL=3000pF	T_{OUTF}		45		ns
On Chip OTP (Internal Thermal Shutdown)						
OTP Level	*	$T_{SHUTDOWN}$		140		°C
OTP Hysteresis	*	$T_{RESTART}$		40		°C

Notes:

*Guaranteed by design.

Typical Performance Characteristics

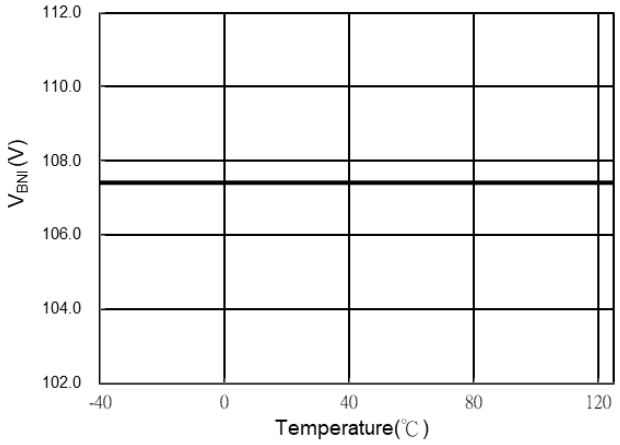


Fig.1 V_{BNI} VS. Temperature

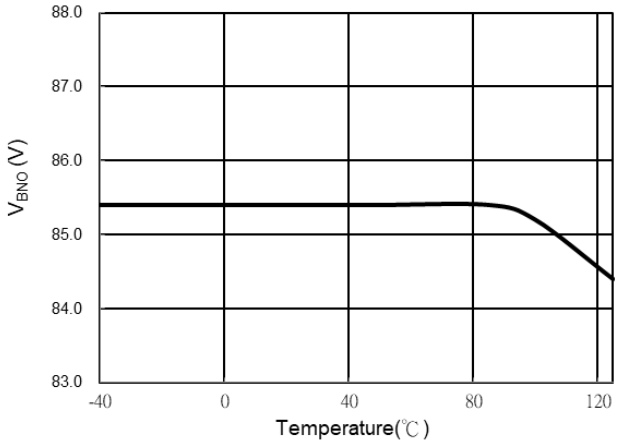


Fig.2 V_{BNO} VS. Temperature

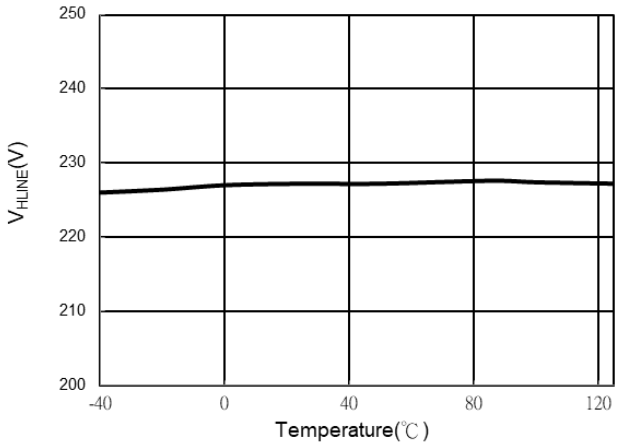


Fig.3 V_{HLINE} VS. Temperature

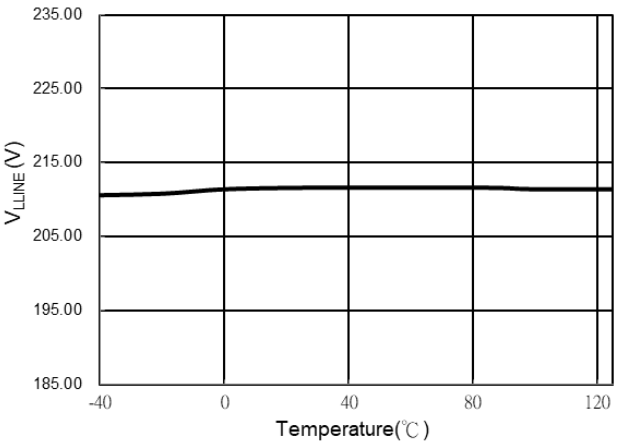


Fig.4 V_{LLINE} VS. Temperature

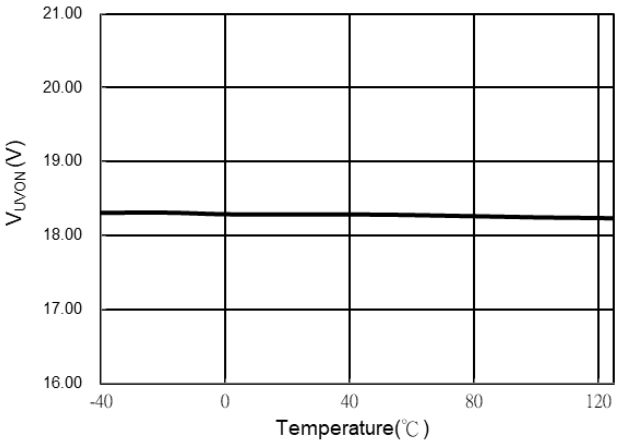


Fig.5 V_{UVON} VS. Temperature

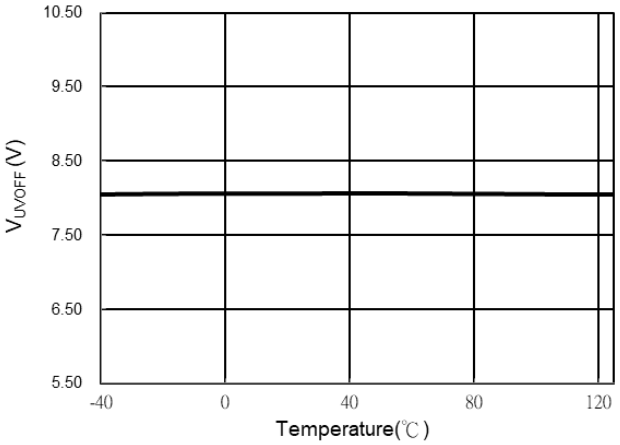


Fig.6 V_{UVOFF} VS. Temperature

Typical Performance Characteristics

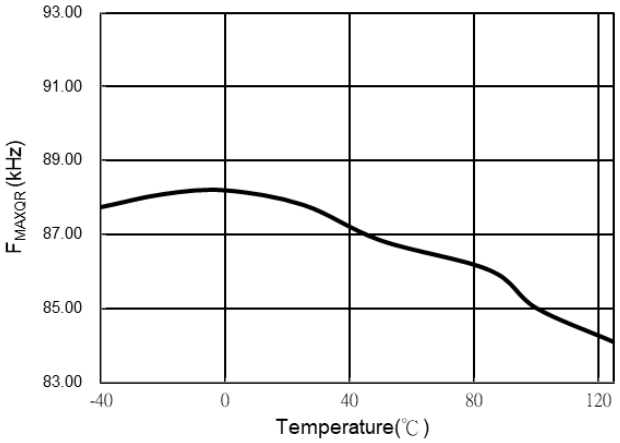


Fig.7 F_{MAXQR} VS. Temperature

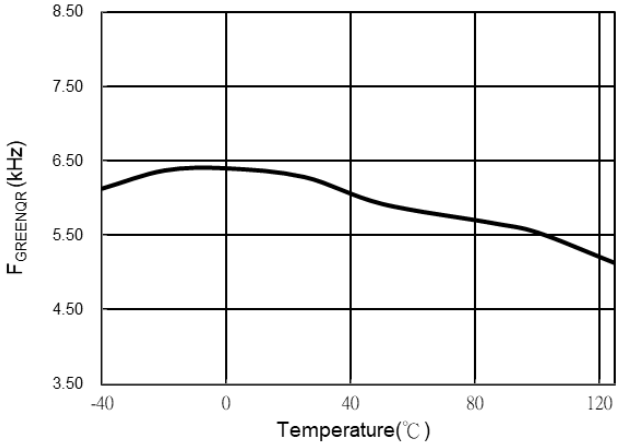


Fig.8 $F_{GREENQR}$ VS. Temperature

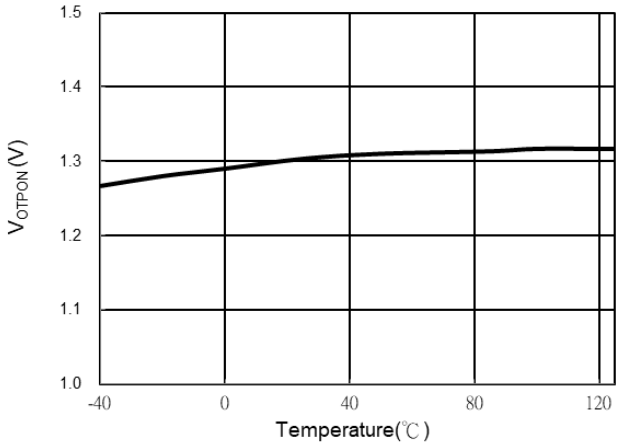


Fig.9 V_{OTPON} VS. Temperature

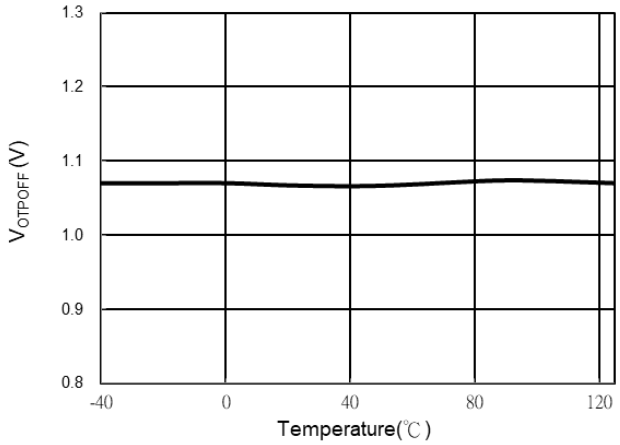


Fig.10 V_{OTPOFF} VS. Temperature

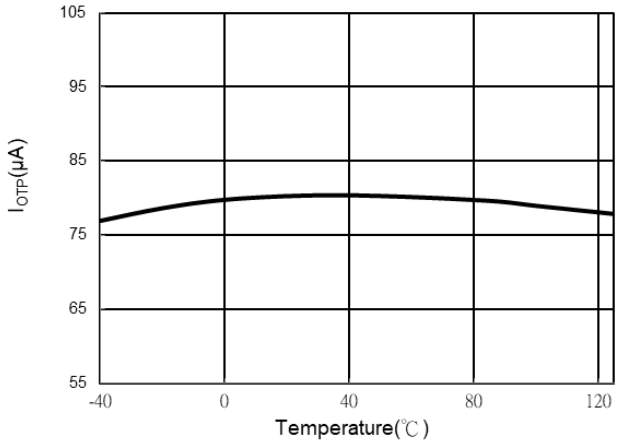


Fig.11 I_{OTP} VS. Temperature

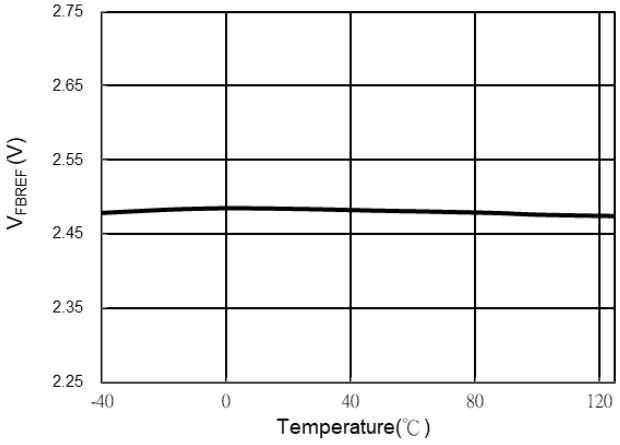


Fig.12 V_{FBREF} VS. Temperature

Typical Performance Characteristics

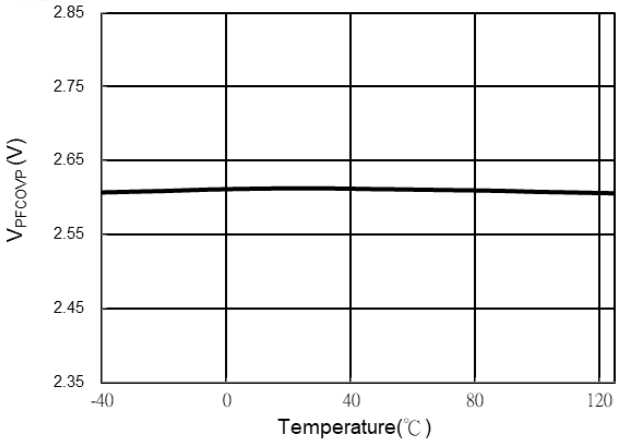


Fig.13 V_{PFCOVP} VS. Temperature

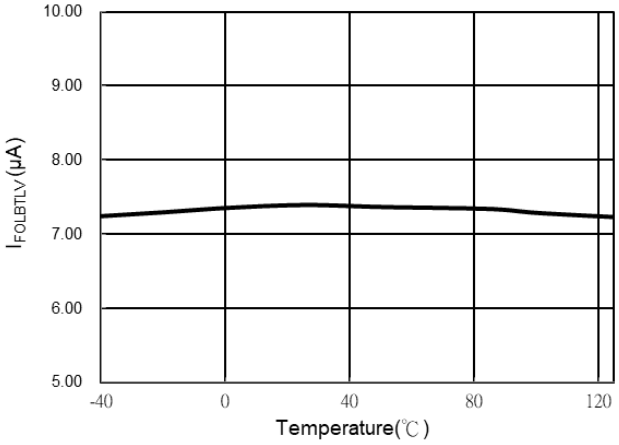


Fig.14 $I_{FOLBTLV}$ VS. Temperature

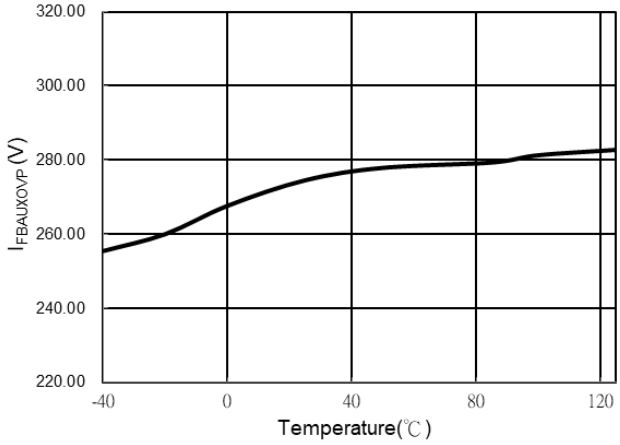


Fig.15 $I_{FBAUXOVP}$ VS. Temperature

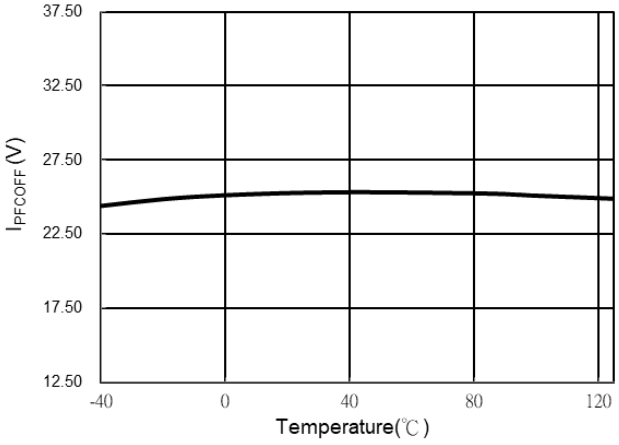


Fig.16 I_{PFCOFF} VS. Temperature

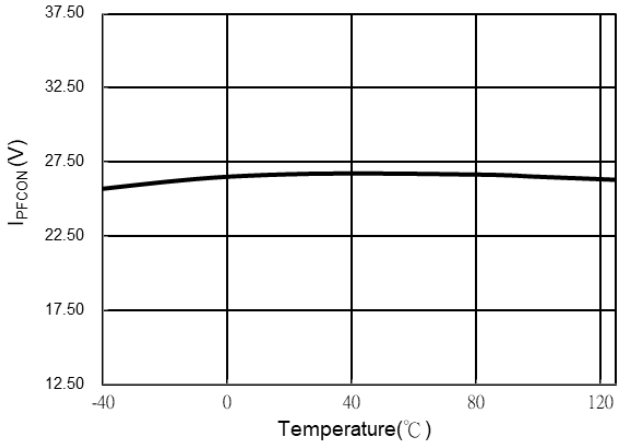


Fig.17 I_{PFCON} VS. Temperature

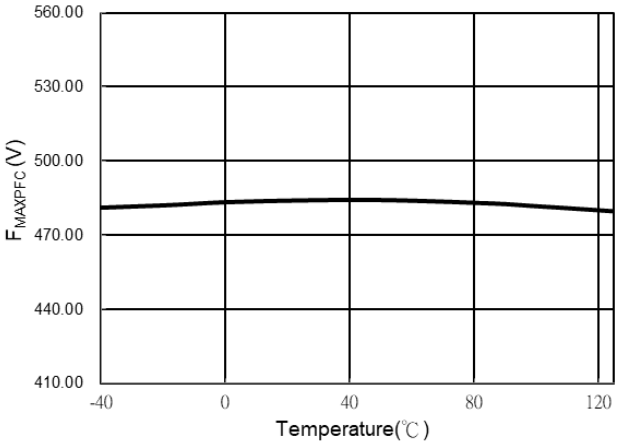


Fig.18 F_{MAXPFC} VS. Temperature

Typical Performance Characteristics

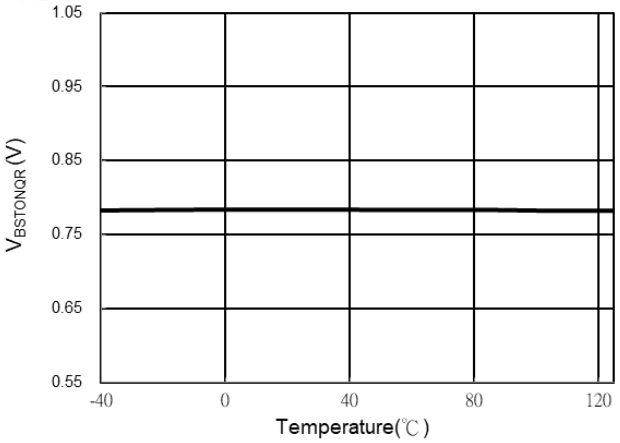


Fig.19 $V_{BSTONQR}$ VS. Temperature

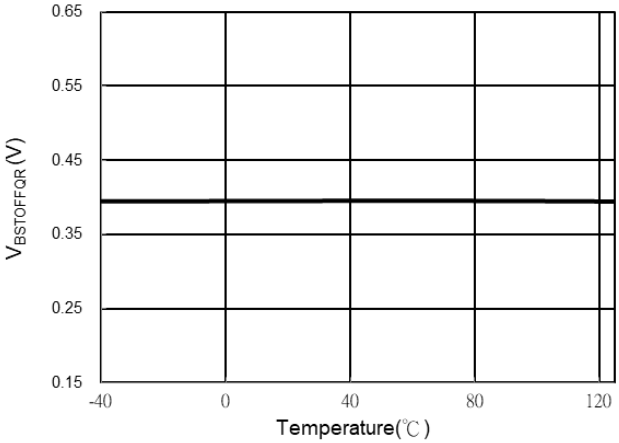


Fig.20 $V_{BSTOFFQR}$ VS. Temperature

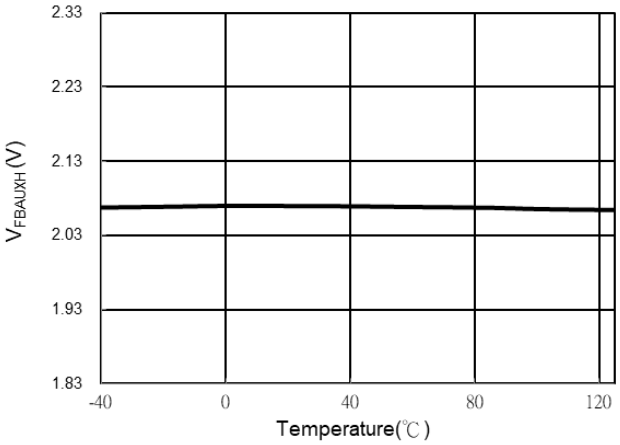


Fig.21 V_{FBAUXH} VS. Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers need to be powerful to integrate more functions to reduce the external part counts. The LD7792S is ideal for these applications to provide an easy and cost effective solution; its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes too much power to meet the current power saving requirement. In most cases, startup resistors carry larger resistance and take more time to start up.

As shown in Fig. 22, the LD7792S is implemented with a high-voltage startup circuit to minimize power loss on startup circuit. During the startup phase, a high-voltage current source sinks current from AC line or neutral to provide the startup current and charge the VCC capacitor C1 at the same time.

Refer to Fig. 23. If VCC is below PDR, the charge current is only 1.5mA and the lower charge current can protect IC if the VCC Pin is shorted to GND. Once VCC voltage rises up to reach the UVLO(on) threshold, HV pin will no longer charge the capacitor and instead, send a gate drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

An UVLO comparator is embedded to detect the voltage across VCC pin to ensure the supply voltage is high enough to power on the LD7792S and in addition to drive the power MOSFET. As shown in Fig. 23, a hysteresis is provided to prevent the LD7792S from shut down by the voltage dip during startup. The turn-on and turn-off threshold level are set at 18V and 8V respectively.

For better EMI performance, it's recommend to connect HV pin to the input terminals of bridge diode, as Fig. 22.

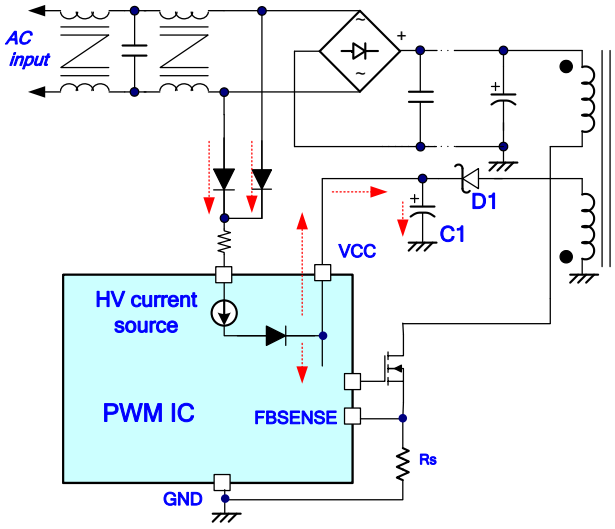


Fig. 22

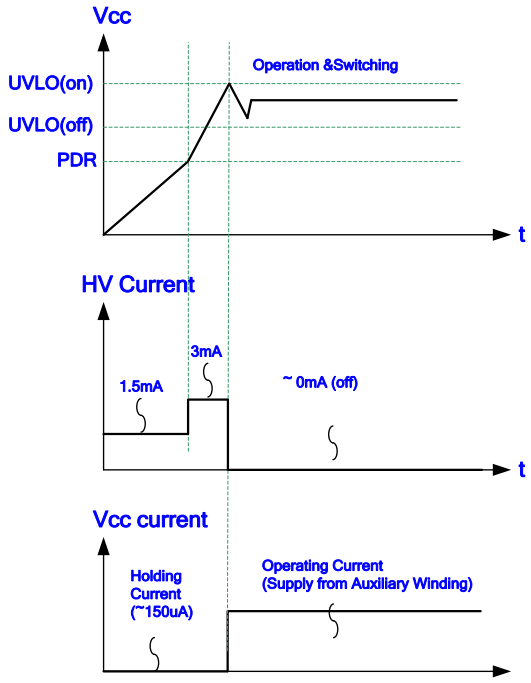


Fig. 23

Output Driver Stage

The device builds a CMOS buffer respectively in the stages of PFC and flyback, with typical 500mA/-1000mA driving capability, to drive the power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the VCC voltage is over 13V.

Brown In/ Out Protection

The LD7792S features brown-in / brown-out protection on HV pin. As the built-in comparator detects line voltage, it will turn off the controller to prevent from any damage. In case VHV < brown-out Level, the output driver will be disabled even when VCC already reaches UVLO (on). It therefore forces VCC hiccup between ULVO (on) and UVLO (off). Unless the line voltage is large enough and over brown-in level, the output driver will not start switching even if the next ULVO (on) is tripped. A hysteresis is designed to prevent from false-triggering and damage to the external components during turn-on and turn-off phase. See Fig. 24 for the operation.

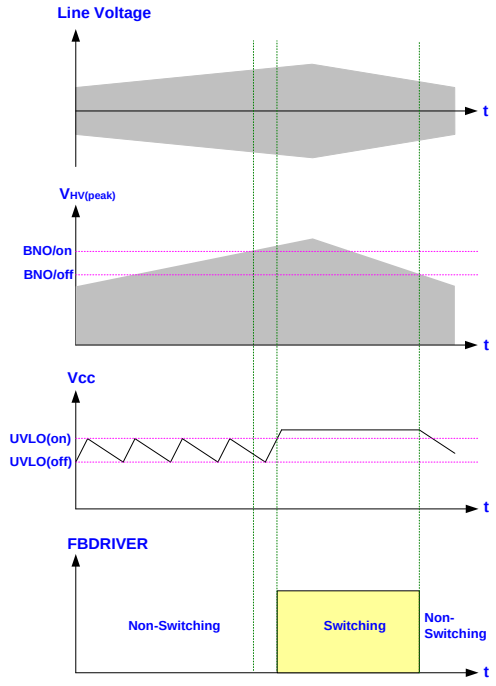


Fig. 24

High Line and Low Line Detection

As shown in Fig. 25, the HV pin can detected AC input level to control source current of VOSENSE Pin and OCP compensation logic. During AC input variations, the source current of VOSENSE and OCP compensation logic show as below.

VHV_{PEAK}	Source Current of VOSENSE	OCP Comp. Logic
≧ 230V	0A	Enable
≦ 210V	8μA	Disable

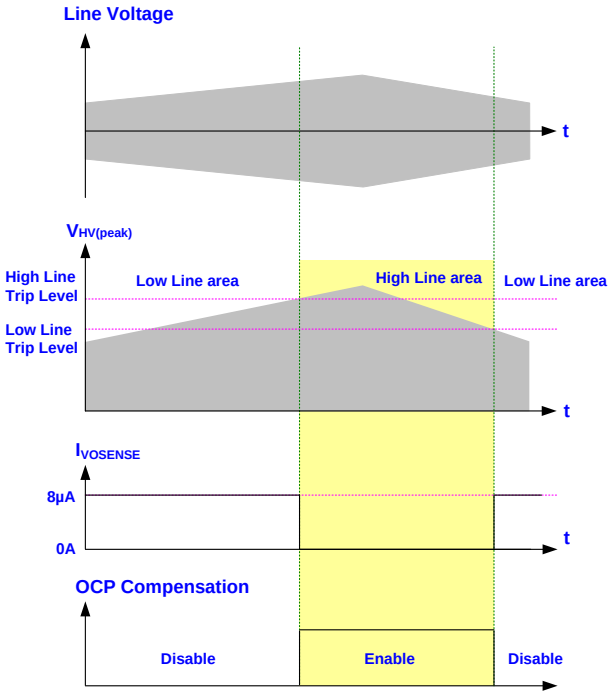


Fig. 25

X-Cap Discharge Function

The EMI filter has a paralleled discharging resistor across X-capacitor. To meet safety requirement, this component is required to be discharged in less than 1sec, that is,

$$\tau_{Discharge} = C_{X-Cap} \times R_{Discharge} \leq 1sec$$

The power loss of this resistor is in direct proportion to square of input voltage. For example, if the input voltage is 264Vac and the discharging resistance ~ 2MΩ, 35mW, we can conclude the power loss by follow equation.

$$P_{Loss} = \frac{V_{AC(RMS)}^{2}}{R_{Discharge}}$$

To eliminate the significant power loss from this discharging resistor, LD7792S applies the innovative patent technology to discharge X-cap's energy through HV current source when AC line is disconnected. Fig. 26 shows the operation.

By applying this technology, the system can easily pass the safety test without discharging resistor and reduce power loss.

If it's unplugged, the AC voltage across X-cap will still remain the same. The LD7792S detects HV pin to monitor the AC voltage across X-cap. If AC voltage across X-cap rises or falls beyond the limit of the threshold, the HV scheme will sink constant current to GND to discharge it in any load condition.

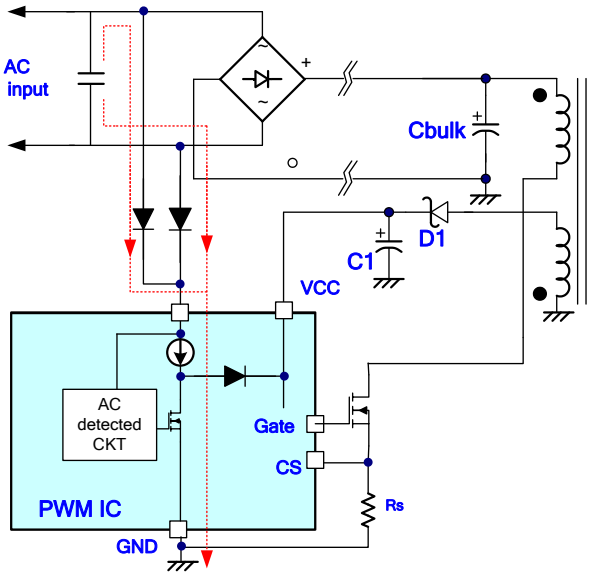


Fig. 26

Flyback Green Mode and PFC Turn-off Control

THE LD7792S uses maximum frequency limit scheme to control flyback switching frequency, and it depends on the level of FBCOMP voltage. When output loading is decreased, FBCOMP voltage becomes lower and the switch frequency can be reduced under the light load condition. This feature helps to enhance the efficiency in light load conditions. The curve shows as Fig. 27.

To meet the requirement of European 'EMC-directive', it's necessary to adopt a solution with PFC control. In order to enhance efficiency at light load, the LD7792S features PFC control and is able to shut down switching to reduce power consumption. As FBCOPM voltage falls below PFC on/off voltage threshold, the PFC controller will stop PFCDRIVER switching until FBCOMP voltage resume to its level. See Fig. 28 for the block.

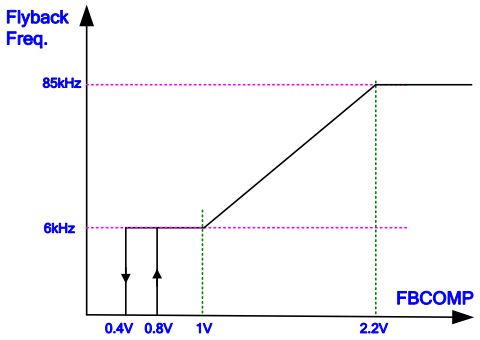


Fig. 27 Max. Frequency Limit of Flyback

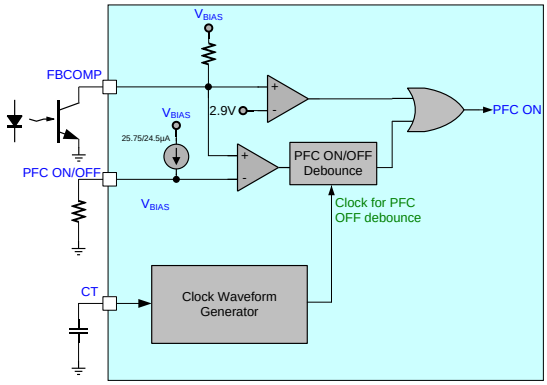


Fig. 28

PFC Output Voltage Setting

LD7792S monitors the output voltage signal from VOSENSE pin through a resistor divider pair of RA and RB. A transconductance amplifier is used for it to replace the conventional voltage amplifier. The output current of the amplifier changes according to the voltage difference of the inverting and non-inverting input of the amplifier. The output voltage of the amplifier is compared with the internal ramp signal to generate the turn-off signal. The current is flowed out of the VOSENSE pin (8μA) during low line condition. The PFC output voltage is determined by the following relationship.

High Line:

$$PFC\ V_O = 2.5V \times (1 + \frac{RA}{RB\ //\ R_{VOSENSE}}) \quad \text{.....(1)}$$

Low Line:

$$PFC\ V_O = (2.5V - 8\mu A \times RB//R_{VOSENSE}) \times (\frac{RA}{RB//R_{VOSENSE}}) + 2.5V$$

.....(2)

where RA and RB are values for top and bottom feedback resistor (as shown in the Fig. 29).

Once the value of PFC V_O is determined, then substitute the value of RA/RB obtained from the formula (1) to (2) to get the RB value.

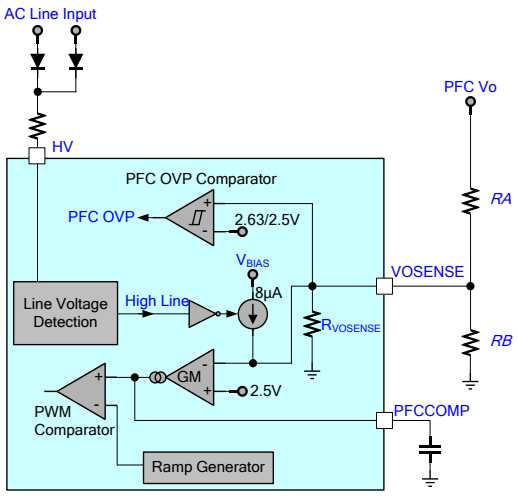


Fig. 29

PFC Over Voltage Protection

To prevent unstable voltage occurred to the PFC output capacitor under fault condition, the LD7792S is implemented with over-voltage protection on VOSENSE pin. If VOSENSE voltage rises over the OVP threshold of 2.63V, the output driver circuit will be shut down simultaneously to stop the switching of the power MOSFET until VOSENSE voltage drops to 2.5V. Fig. 30 shows its operation.

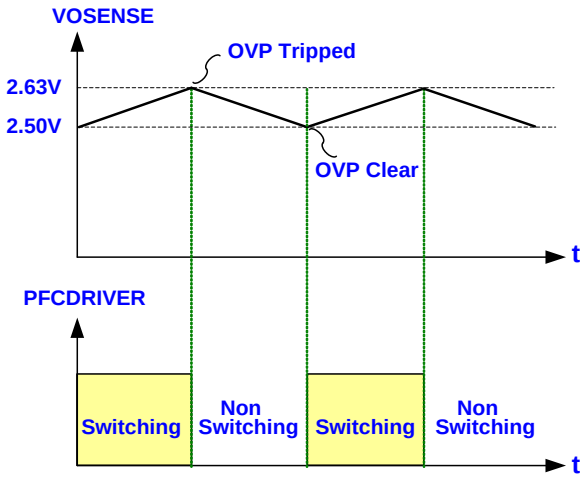


Fig. 30

PFC Zero Current Detection

Fig. 31 shows PFC Zero Current Detection (ZCD) block. As the auxiliary winding coupled with the inductor detects the current over the boost inductor drops to zero, the ZCD block will switch on the external MOSFET. This feature allows transition-mode operation. If the voltage of the PFCAUX pin rises above 0.2V, the ZCD comparator will turn on the MOSFET. The PFCAUX pin is protected internally by 4V-high clamp and 0V-low clamp. The 50μs timer will generate a MOSFET turn-on signal if the output driver has been at low level for over 50μs.

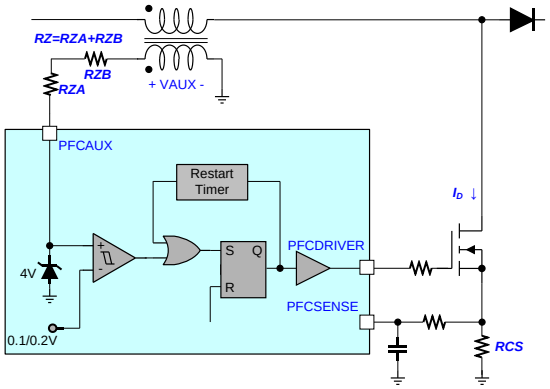


Fig. 31

Fig. 32 shows typical ZCD-related waveforms. Rz will produce some delay because of the parasitic capacitance on PFCAUX pin. Before the switch turns on with the delay, the stored charge of the C_{OSS} (MOSFET output capacitor) will be discharged to a small filter capacitor C_{IN1} with a bridge diode through the path indicated in Fig. 33. So the input current I_{IN1} drains to zero at the time. Here, it's recommended to set source current of PFCAUX pin around 1mA. Rz could be obtained from the below formula and is also adjustable to control the turn-on timing of the switch.

$$R_Z = PFC\ Vo_{MAX} \times \frac{N_{AUX,PFC}}{N_{P,PFC}} \div 1\,mA$$

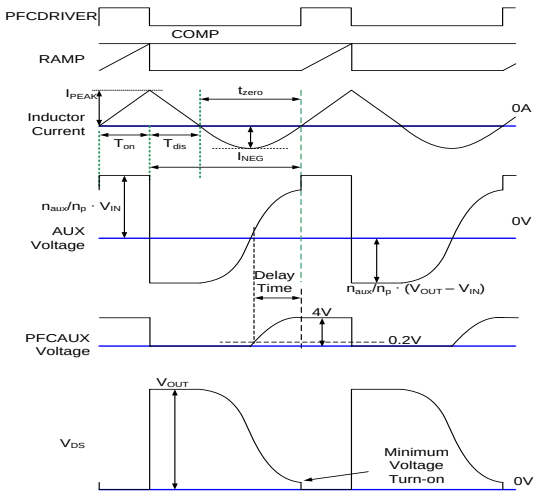


Fig. 32

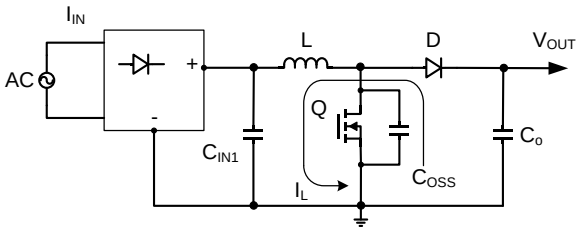


Fig. 33

PFC Current Sensing

The LD7792S detects the PFC MOSFET current across PFCSENSE pin to protect the MOSFET, which is for the cycle-by-cycle current limit. The maximum voltage threshold of PFCSENSE pin is set at 0.52V. The MOSFET peak current can be obtained as below.

$$I_{PEAK(MAX)} = \frac{0.52V}{R_{S,PFC}}$$

A 250ns leading-edge blanking (LEB) time is built in PFCSENSE pin to prevent the false-trigger from the current spike. The R-C filter is eliminable in some low power applications, such as the pulse width of the turn-on spike below 250ns and the negative spike on PFCSENSE pin is below -0.3V.

However, the pulse width of the turn-on spike is determined according to the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for high power application to avoid PFCSENSE pin being damaged by the negative turn-on spike as shown in Fig. 34.

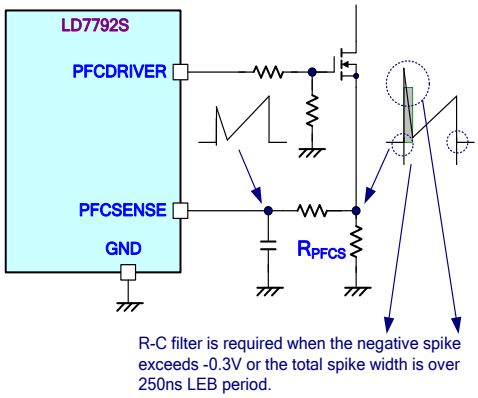


Fig. 34

Flyback Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to FBCOMP pin of the LD7792S and fed to the voltage divider with 1/5.5 ratio. That is,

$$V_{FBSENSE(PWM_{COMPARATOR})} = \frac{V_{FBCOMP}}{5.5}$$

A pull-high resistor is embedded internally to optimize the external circuit.

Flyback Burst Mode Control

The output driver of the LD7792S can be disabled immediately by pulling FBCOMP pin voltage level below FBDRIVER stop trip level. The disable-mode can be released when FBCOMP pin voltage level is pulled high above FBDRIVER start trip level.

Flyback Current Sensing & OCP Compensation Design Tip

The LD7792S features current mode of flyback control. It receives both current signal and voltage signal to form the control loop and achieve regulation. LD7792S detects the primary MOSFET current across FBSENSE pin for peak current mode and also limits the current cycle-by-cycle. The maximum voltage threshold of FBSENSE pin is set at 0.65V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.65V}{R_{S,FB}}$$

In general, the power converter provides various current signals to reflect the input voltage with propagation delay time. To compensate it, an offset voltage is added to the FBSENSE signal by an internal current source (200μA) and an external resistor (R_{OCP}) between the sense resistor (R_{FBS}) and FBSENSE pin, as shown in Fig. 35. The compensation current is only enabled when FBCOMP voltage is above 2.9V at high line condition. R_{OCP}: 100~1kΩ; C_{OCP}: 47p~470pF.

As PFC behaves in current sensing, a 350ns leading-edge blanking (LEB) time is incorporated in the input of FBSENSE pin to prevent false-triggering from the current spike.

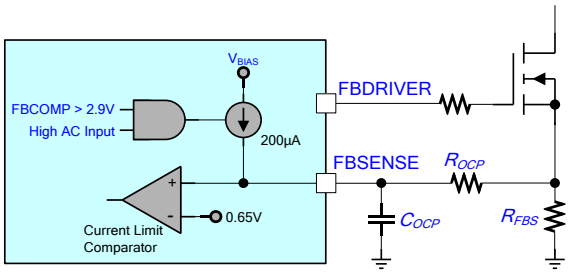


Fig. 35

Protection Mode

There is one kind of protection modes available in the LD7792S.

Auto-Recovery Protection Mode

As auto-recovery protection circuit latches the operation, the gate output will switch for a short term as every time VCC rises back to UVLO(ON). It therefore forces the VCC hiccup between UVLO(ON) and UVLO(OFF). As soon as the fault condition is removed, the system will resume it operation right away. Fig. 36 shows the operation.

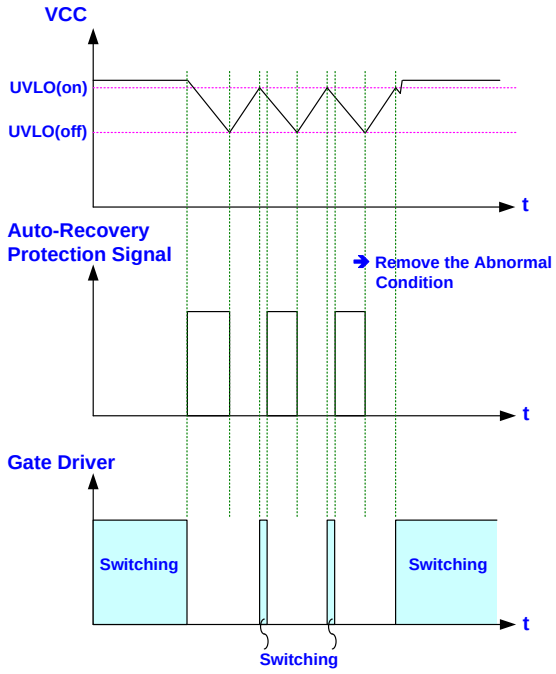


Fig. 36

Over Load Protection (OLP)– Auto Recovery

To protect the circuit from being damaged at over-load condition, short or open loop condition, the LD7792S is implemented with smart OLP function. The LD7792S features auto recovery function. See Fig. 37 for the waveform. In such fault condition, the feedback system will force the voltage loop to enter saturation and then pull high the voltage over FBCOMP pin (VFBCOMP). When VFBCOMP ramps up to the OLP tripped level (4.2V) for longer than the OLP delay time, the protection will be activated to turn off the output driver and to stop the switching of power circuit. The OLP delay time is set by CT pin. It is to prevent the false triggering during the transient condition of power-on and turn-off.

A divide-4 counter is implemented to reduce the average power under OLP behavior. Whenever OLP is activated, the output is latched off and the divide-4 counter starts to count the number of UVLO(off). The protection mode will not be released and the output will not be resumed until the 4th UVLO(off) level is tripped. With the protection mechanism, the average input power will be reduced, so that the component temperature and stress can be controlled within the safe operating area.

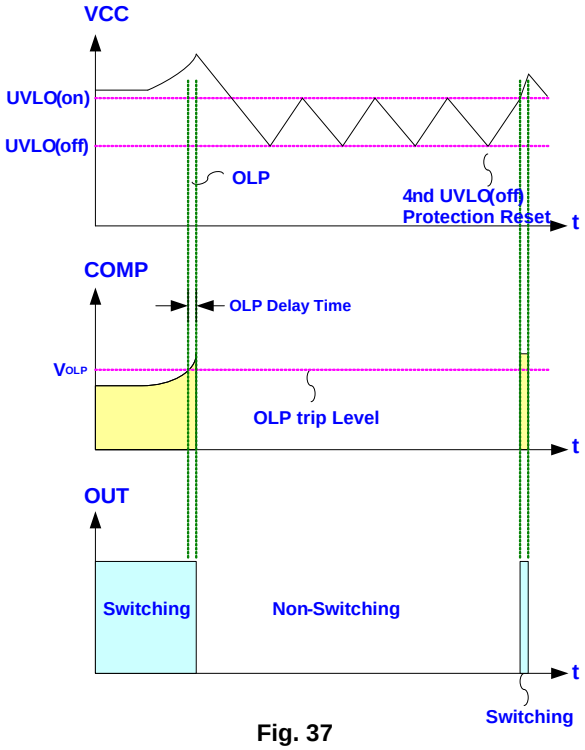


Fig. 37

Output Short Circuit Protection (OSCP)

If the output of the system is short-circuited, Vo and VCC will drop immediately. Due to the operating of the voltage loop, FBCOMP voltage will be pulled high at the same time. If the situation continues to pull FBCOMP high over 4.2V for over 16ms and VCC drops below 10V, it will activate OSCP protection against damage and turn off the gate driver.

OVP on VCC – Auto Recovery

The maximum VCC rating of the LD7792S is about 32.5V. To protect the LD7792S in over-voltage condition, it is implemented with OVP function on VCC. Once VCC voltage rises over the OVP threshold, it will turn off the output driver right away and disable the power MOSFET until the UVLO(on) is tripped.

The VCC OVP function is auto-recoverable. If the OVP condition, usually caused by open-loop of feedback, is not released, the VCC will trip the OVP level again and re-shutdown the output driver. This makes VCC work in hiccup mode. Fig. 38 shows its operation.

After the OVP condition is removed, VCC will keep in its normal operation level and the output driver also return to the normal operation.

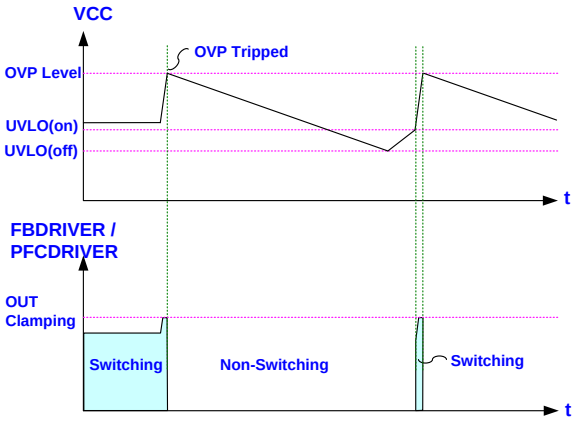


Fig. 38

Flyback Zero Current Detection

Fig. 39 shows flyback Zero Current Detection (ZCD) block. As PFC behaves in ZCD, as soon as the auxiliary winding coupled with the inductor detects the current over the flyback transformer drops to zero, the ZCD block will switch on the external MOSFET. This feature enables quasi-resonant operation. The FBAUX uses falling edge to trigger ZCD to turn on FBDRIVER and the trigger level is 0.05V as shown in Fig. 40. FBAUX pin is built-in with 2V-high clamp and 0V-low clamp.

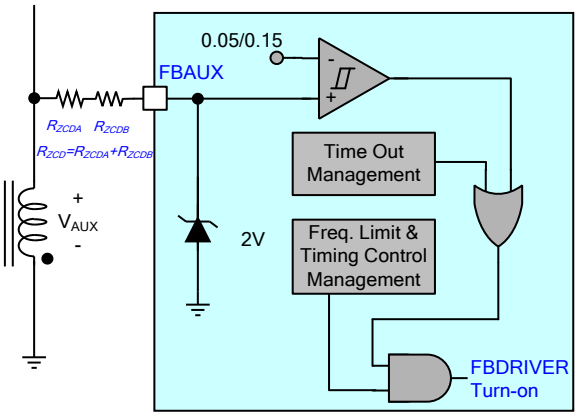


Fig. 39

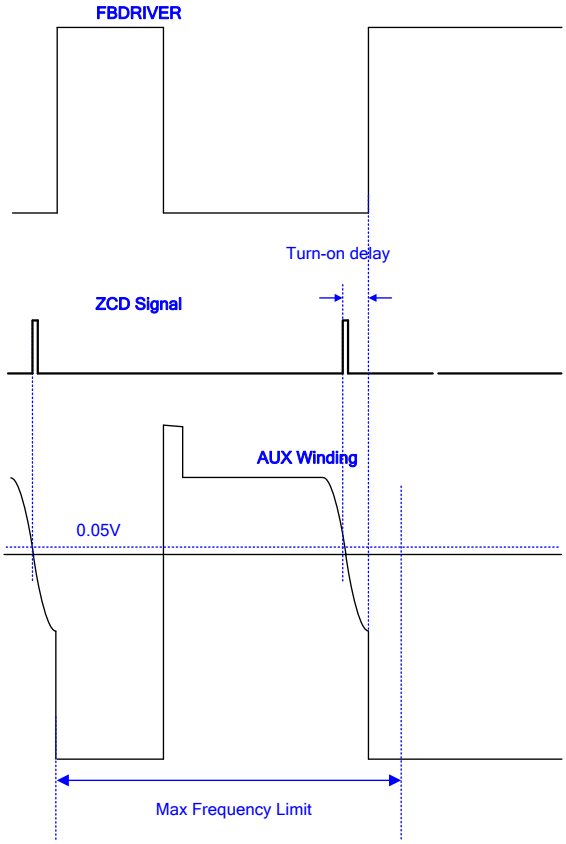


Fig. 40

OVP on FBAUX – Auto Recovery

FBAUX also provide over voltage protection (OVP). An output overvoltage protection is implemented in the LD7792S, as shown in Fig. 41 and Fig.42. It senses the auxiliary winding voltage by the resistor, R_{ZCD}. The auxiliary winding voltage is reflected on the secondary winding and therefore the flat voltage on FBAUX pin is in proportion to the output voltage. The flat voltage can be transformed into a current signal. The sinking current of FBAUX is,

$$I_{FBAUX} = [(V_O + V_D) \times \frac{N_{AUX}}{N_S} - 2V] / R_{ZCD}$$

The LD7792S samples the signal after FBDRIVER turn-off with 2µs delay to perform output over voltage protection. This 2µs delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampled current level is compared with internal threshold current 300µA. If the sampled current exceeds the OVP trip level, an internal counter will start to count the subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If 4 flyback PWM cycles of the subsequent OVP events are detected, the OVP circuit will switch the power MOSFET off.

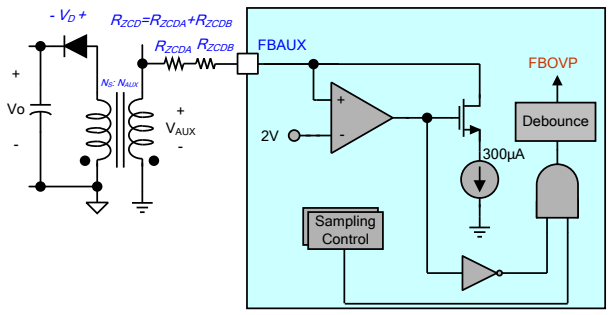


Fig. 41

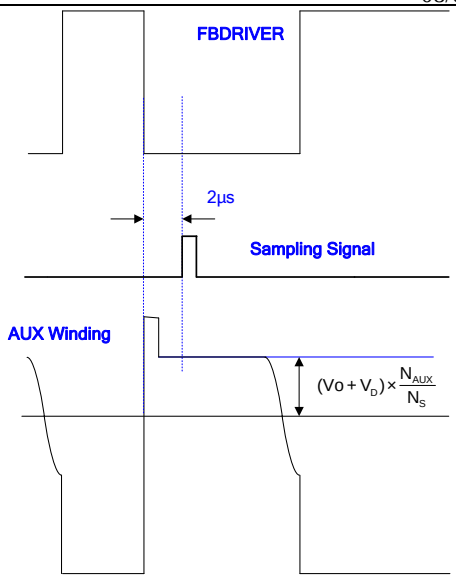


Fig. 42

On-Chip OTP – Auto Recovery

An internal OTP circuit is embedded in the LD7792S to provide the worst-case protection. When the chip temperature rises over the trip OTP level, the output driver will be disabled until the chip is cooled down below the hysteresis temperature.

External OTP

The external OTP function is implemented to sense whether there is any hot-spot of power circuit like power MOSFET or output rectifier. Once an over-temperature condition is detected, the OTP will be activated to shut down the LD7792S, as shown in Fig. 43. When all protections is operation to stop switching output, internal bias current on OTP pin is turned off at the same time.

Typically, an NTC is recommended to connect to OTP pin. The NTC resistance will decrease as the device or ambient stays in high temperature. The relationship is shown below.

$$V_{OTP} = 80\mu A \times R_{NTC}$$

When V_{OTP} < Turn-off Trip (typ. 1.0V), it will trigger the protection to shut down the output driver and auto recovery when temperature is cooling down.

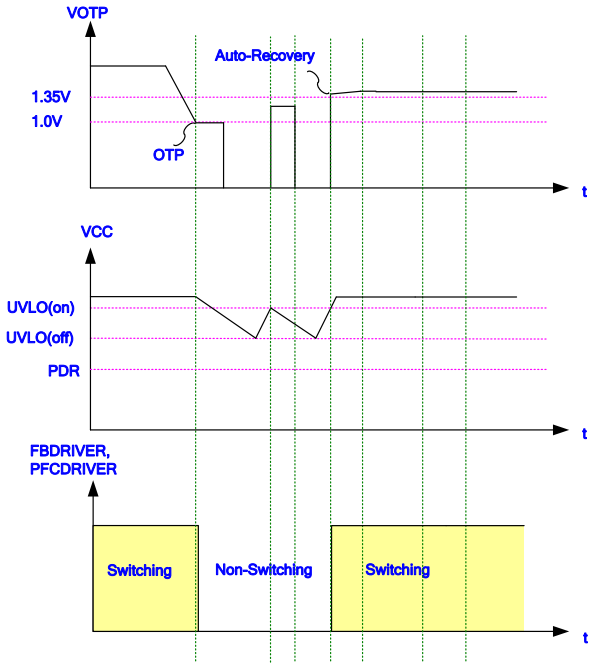


Fig. 43

Adjustable Timer on CT Pin

Connect CT pin with an external capacitance to generate clock for timer. The OLP debounce, PFC Turn-off debounce and flyback Soft-start period are set according the below table.

C_{CT}	FB Soft-start period	FB_OLP Debounce Time	PFC Turn-off Debounce
22nF	4.6ms	30ms	0.47s
47nF	10.0ms	64ms	1.00s
68nF	14.0ms	93ms	1.45s
100nF	21.2ms	136ms	2.13s
150nF	31.8ms	204ms	3.2s
220nF	42.4ms	272ms	4.26s

Pull-Low Resistor on the Gate Pin of MOSFET

The LD7792S consists of an anti-floating resistor at PFCDRIVER and FBDRIVER pin to prevent the output driver in any abnormal condition which may false trigger MOSFET. Even so, we still recommend adding an external one at the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as shown in Fig. 44, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the gate of MOSFET should be always pulled low and kept in the off-state as the gate resistor is disconnected or opened in any case.

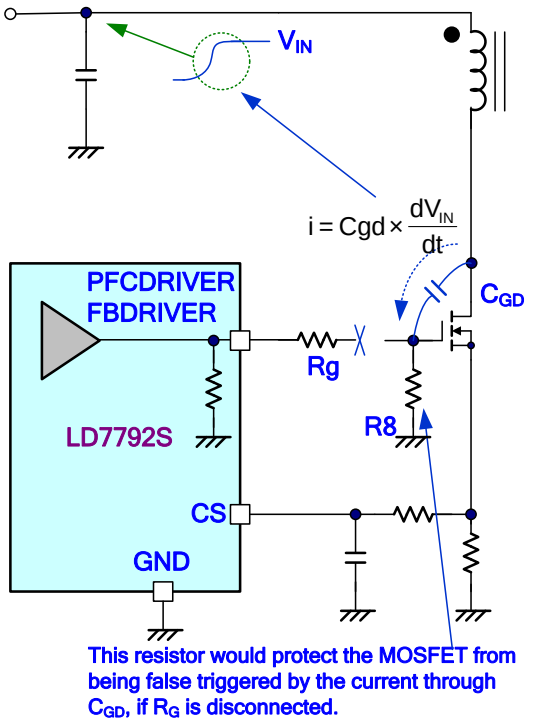


Fig. 44

Protection Resistor on the HV Path

In some other Hi-V process and design, there may be a parasitic SCR formed between HV pin, VCC and GND. As shown in Fig. 45, a small negative spike on the HV pin may trigger this parasitic SCR and cause latch-up between VCC and GND. It may damage the chip because of the equivalent short-circuit induced by such latch-up behavior.

Leadtrend's proprietary of Hi-V technology will eliminate parasitic SCR in the LD7792S. Fig. 46 shows the equivalent Hi-V structure circuit of LD7792S. LD7792S is more capable to sustain negative voltage than similar products. However, a 10KΩ resistor is recommended to be added in the Hi-V path to play as a current limit resistor whenever a negative voltage is applied.

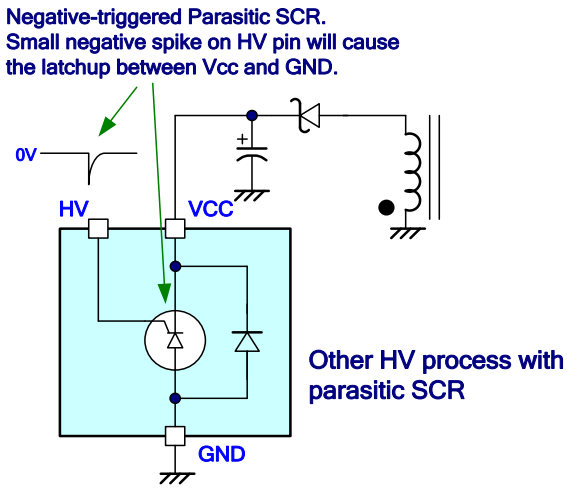


Fig. 45

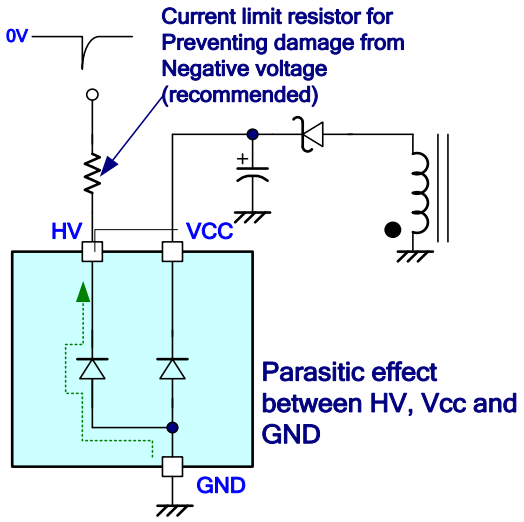


Fig. 46

THDi Optimization

LD7792S introduces a THDi optimizer which greatly reduces THDi than LD7792 does. As shown in Fig. 47, the AC signal is introduced to THDi optimizer and a THDi compensation signal is produced to compensate the PFC turn-on time. When the AC voltage is at its low phase, the PFC turn-on time is increased to compensate the AC input current reduction caused by maximum frequency limit and PFC input capacitor C_{IN}. Low THDi performance makes LD7792S suitable for the lighting application.

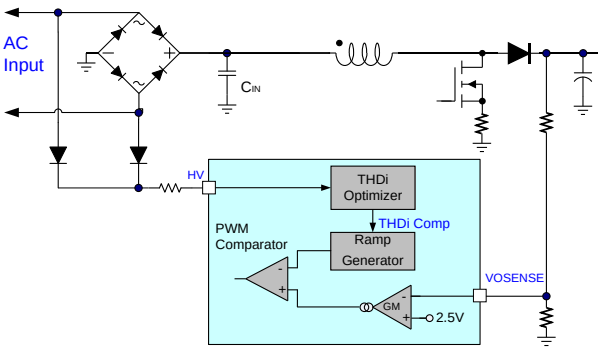


Fig. 47

Start-up Audible Noise Elimination

LD7792S implements a new start-up control sequence to eliminate the start-up audible noise. LD7792S no longer switches into audible frequency and the switching discontinuity is also eliminated.

Frequency Reduction Mode Selection

There are two control schemes in the frequency reduction region, PWM & QRM respectively, as shown in Fig. 48. Each of these control schemes has their pros and cons. The QRM control scheme features valley switch to reach the best efficiency performance but the valley jumping caused by input voltage fluctuation produces audible noise. On the contrary, the PWM mode scheme features no audible noise but the efficiency drops a little due to the loss of non-valley switch.

LD7792S offers both PWM and QRM for users to select. As shown in Fig.49 , LD7792S is set to PWM in frequency reduction region when $R_{PFCSENSE}$ is not more than 220 Ohm while QRM is set when $R_{PFCSNSE}$ is more than 820 Ohm.

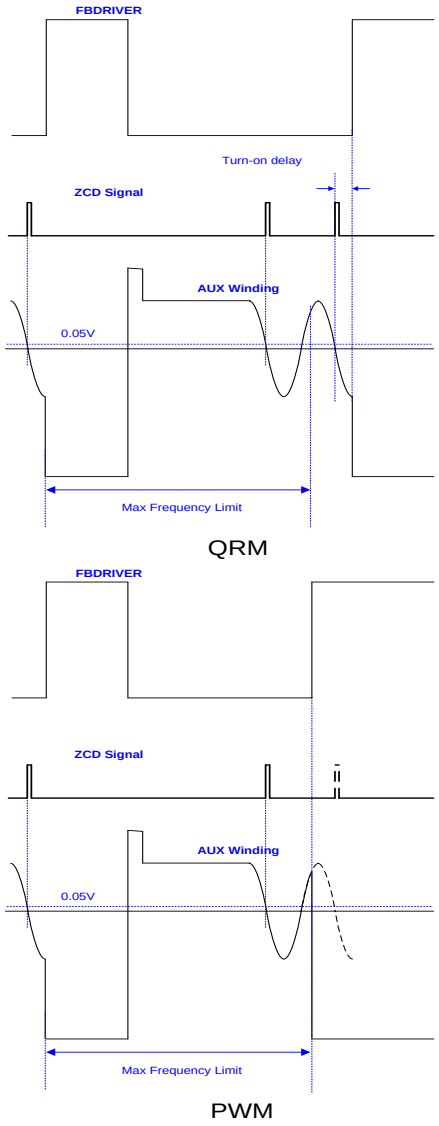


Fig. 48

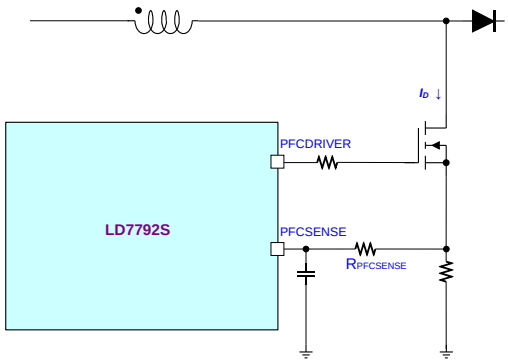


Fig. 49

PCB Layout Guideline

The LD7792S consists of a pair of gate drivers. Here are some guide lines to layout the PCB to suppress the noise caused from the effects between PFC and flyback. The PCB layout diagram is shown as Fig. 50.

1. Separate small signal current loop from gate driver or VCC current loop.
2. Separate VCC current loop from PFC gate driver to minimize the effect from flyback ZCD.
3. Minimize the trace length between GND pin and the current sense resistor.
4. Be aware to route the HV pin AWAY from the other traces for it possesses high voltage.

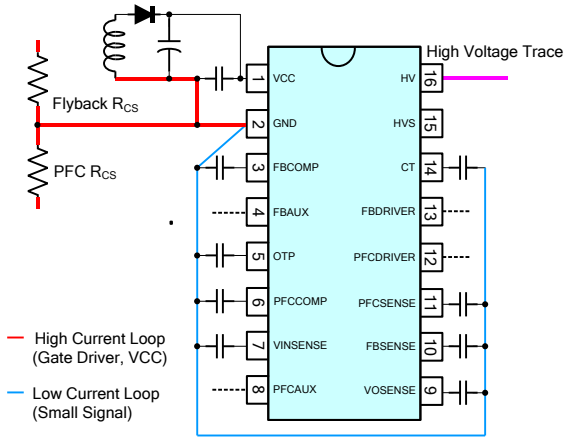


Fig. 50

Inrush Current of PFC

During fast AC powers on/off, inrush current will flow through PFC choke if bulk capacitor voltage is lower than AC line voltage. Once PFC controller remains operation in such condition, large current will flow in PFC MOSFET during gate turn-on phase, shown as Fig. 51. So, it's necessary to select a MOSFET of proper current stress to avoid damage.

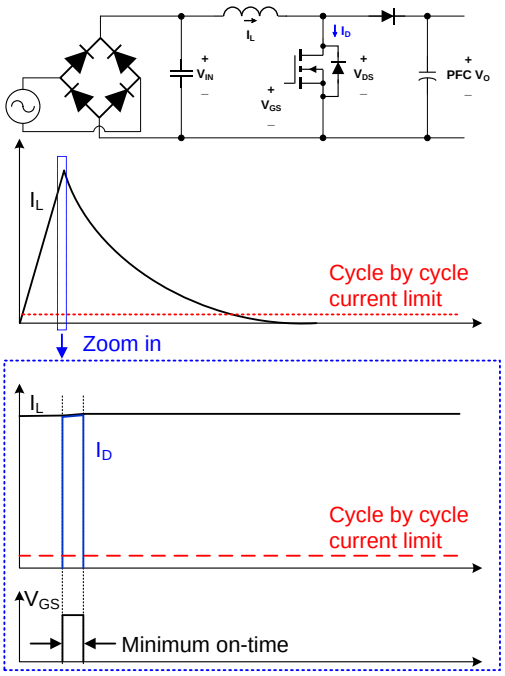


Fig. 51

Under this condition, during MOSFET gate turn-on and turn-off period, some MOSFET will couple with the high frequency energy, generated from parasitic element as inrush current resonates into the controller. See Fig. 52 for it. The gate driver of controller could be damaged by the external energy. Add a bead core in the gate driver current loop to blank the high frequency energy from damage, shown as Fig. 53. And place an extra by-pass diode here to limit inrush current of PFC choke helps to minimize the risk, shown as Fig. 54.

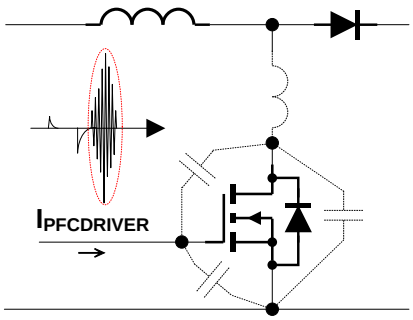


Fig. 52

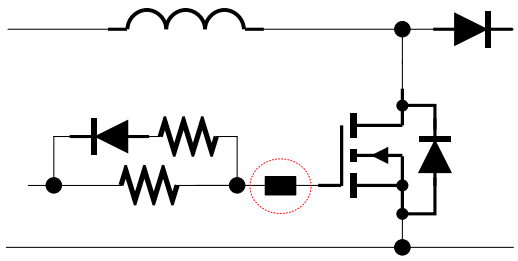


Fig. 53

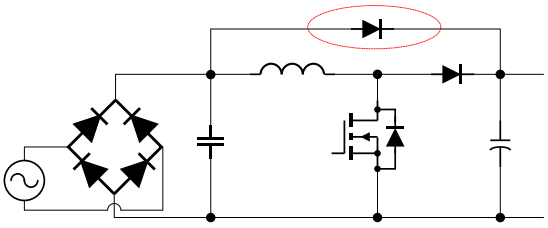
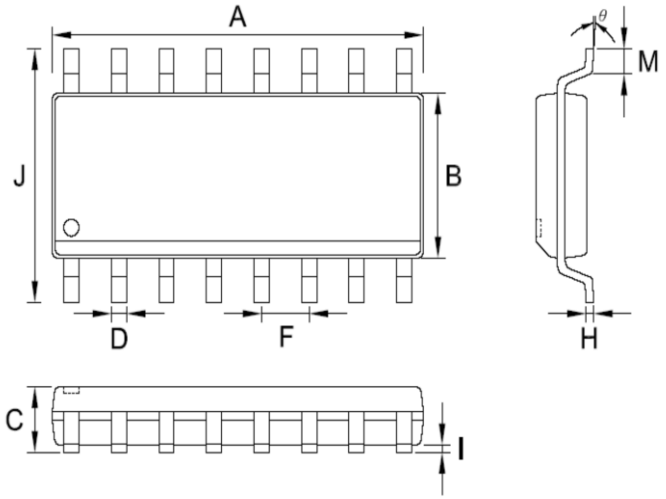


Fig. 54

Package Information

SOP-16



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	9.800	10.010	0.386	0.394
B	3.800	4.000	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.510	0.013	0.020
F	1.27 TYP.		0.05 TYP.	
H	0.178	0.254	0.007	0.010
I	0.100	0.254	0.004	0.010
J	5.790	6.200	0.228	0.244
M	0.380	1.270	0.015	0.050
θ	0°	8°	0°	8°

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

REV.	Date	Change Notice
00	08/06/2018	Original Specification