High Efficiency 1MHz 3.5A Synchronous Step Down Regulator

Description

The FP6392 is a high-efficiency 1MHz synchronous step-down DC-DC regulator and capable of delivering output current up to 3.5A. The FP6392 operates over wide input voltage range from 2.7V to 6V, and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple, small external inductor and capacitor sizes are achieved with 1MHz switching frequency.

The FP6392 is offered in TDFN-10 (3mmx3mm) Package.

Features

- Low $R_{DS(ON)}$ for Internal Switch (Top/Bottom): 95/75mΩ
- 2.7V-6V Input Voltage Range
- Adjustable Output Voltage Down to 0.6V
- Internal Compensation Function
- 1MHz Switching Frequency
- Internal Soft-Start Limits the Inrush Current
- 100% Dropout Operation
- Over-Temperature Protection with Auto Recovery
- Cycle-by-Cycle Current Limit
- Input Under Voltage Lockout
- RoHS Compliant and Halogen Free
- Compact Package: TDFN-10 (3mm x 3mm)

Applications

- Set Top Box
- LCD TV
- Tablet
- Portable Equipment

Pin Assignments

DA Package (TDFN-10)(3mm x 3mm)

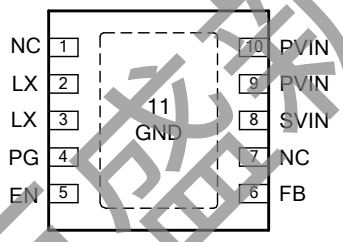


Figure 1. Pin Assignment of FP6392

Ordering Information

FP6392□

Package Type
DA: TDFN-10 (3mm x 3mm)

Typical Application Circuit

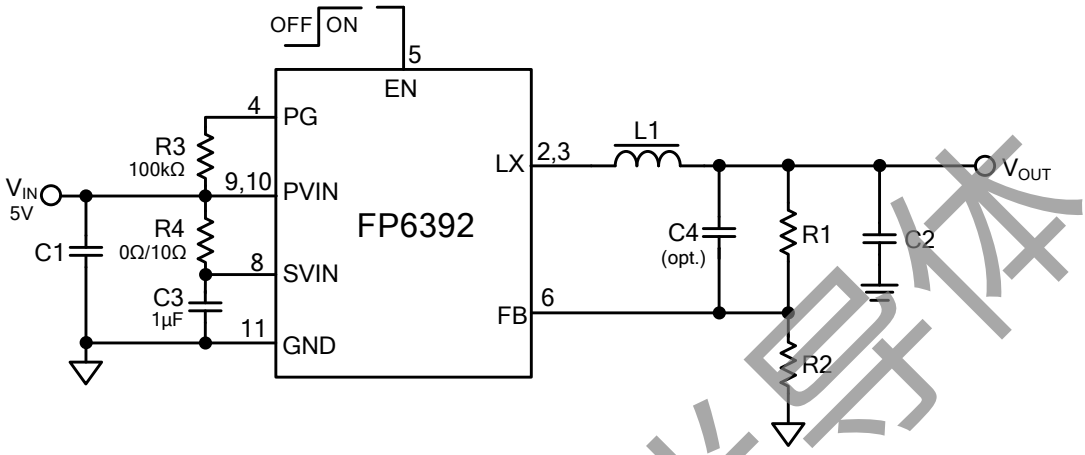


Figure 2. Schematic Diagram

V_{IN}=5V, the recommended BOM list is as below.

V_{OUT}	C1	R1	R2	L1	C2
3.3V	10μF MLCC	453kΩ	100kΩ	2.2μH	22μF MLCC x2
2.5V	10μF MLCC	316kΩ	100kΩ	2.2μH	22μF MLCC x2
1.8V	10μF MLCC	200kΩ	100kΩ	1.8μH	22μF MLCC x2
1.5V	10μF MLCC	150kΩ	100kΩ	1.5μH	22μF MLCC x2
1.2V	10μF MLCC	100kΩ	100kΩ	1.5μH	22μF MLCC x2
1.05V	10μF MLCC	75kΩ	100kΩ	1.2μH	22μF MLCC x2

Table 1. Recommended Component Values

Functional Pin Description

Pin Name	Pin No.	Pin Function
NC	1, 7	No connection.
LX	2, 3	Power switching node. Connect an external inductor to this switching node.
PG	4	Open drain power good output pin.
EN	5	Enable control. Pull high to turn the IC on, and pull low to disable the IC.
FB	6	Output feedback pin. Connect FB and V_{OUT} with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.6V.
SVIN	8	Signal input pin. Decouple this pin to GND pin with 0.1μF~1μF ceramic capacitor.
PVIN	9, 10	Power input pin. Decouple this pin to GND pin with at least 4.7μF ceramic capacitor.
Exposed Pad	11	Ground pad.

Block Diagram

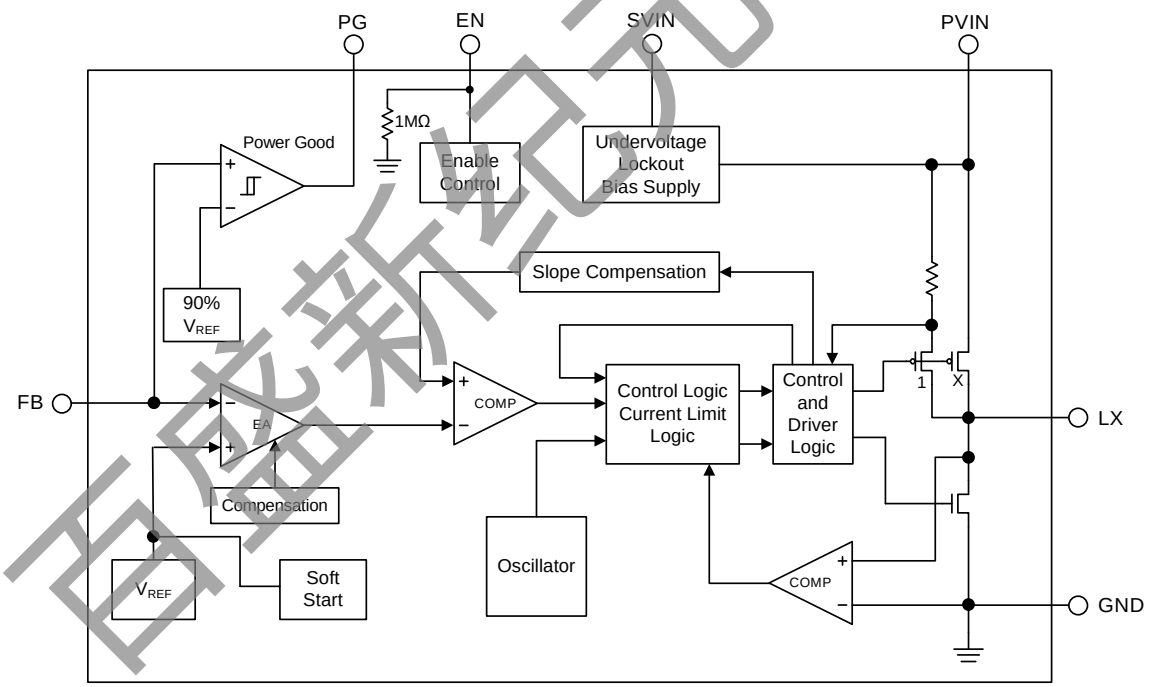


Figure 3. Block Diagram of FP6392

Absolute Maximum Ratings (Note 1)

- PVIN, SVIN to GND ---------- -0.3V to +6.5V
- LX to GND (DC) ---------- -0.3V to V_{IN}+0.3V
- EN, FB, PG to GND ---------- -0.3V to V_{IN}
- Package Thermal Resistance (θ_{JA})

  TDFN-10 (3mmx 3mm) ---------- 70°C/W
- Package Thermal Resistance (θ_{JC})

  TDFN-10 (3mmx 3mm) ---------- 30°C/W
- Junction Temperature Range ---------- +150°C
- Lead Temperature (Soldering, 10 sec.) ---------- +260°C
- Storage Temperature Range ---------- -65°C to +150°C

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions (Note 2)

- Supply Input Voltage (PVIN, SVIN) ---------- +2.7V to +6V
- Junction Temperature Range ---------- -40°C to +125°C
- Ambient Temperature Range ---------- -40°C to +85°C

Note 2: The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{IN}=5V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.7		6	V
Shutdown Current	I_{SD}	EN=GND		0.1	1	μA
Quiescent Current	I_Q	V_{FB}=0.65V, I_{OUT}=0A	50	100	150	uA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=V_{IN}	-50		50	nA
PFET RON	$R_{DS(ON),P}$			95		mΩ
NFET RON	$R_{DS(ON),N}$			75		mΩ
PFET Current Limit	I_{LIM}		4			A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				2.7	V
UVLO Hysteresis	V_{HYS}			0.2		V
Oscillation Frequency	F_{OSC}	I_{OUT}=350mA	0.8	1	1.2	MHz
Minimum ON Time				50		ns
Maximum Duty Cycle			100			%
PG Rising Threshold	$V_{PG(H)}$	V_{FB} Rising		90		%
PG Sink Current	I_{PG}	V_{PG}=0.1V		1		mA
Internal Soft Start Time	T_{SS}			1		ms
VOUT Discharge Resistance				100		Ω
Thermal Shutdown Temperature	T_{SD}			150		°C

Typical Performance Curves

V_{IN}=5V, V_{OUT}=1.2V, C1=10μF, C2=22μFx2, C4=22pF, L1=1.5μH, TA=+25°C, unless otherwise noted.

V_{OUT}=1.2V

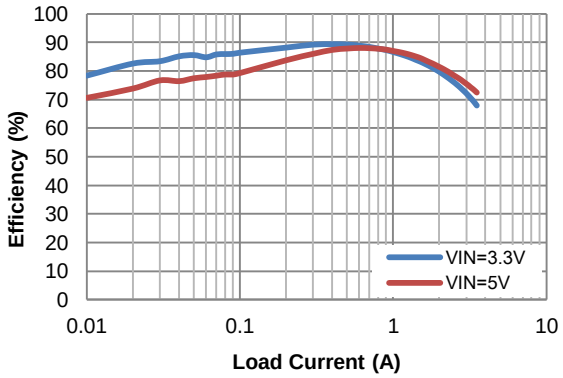


Figure 4. Efficiency vs. Load Current

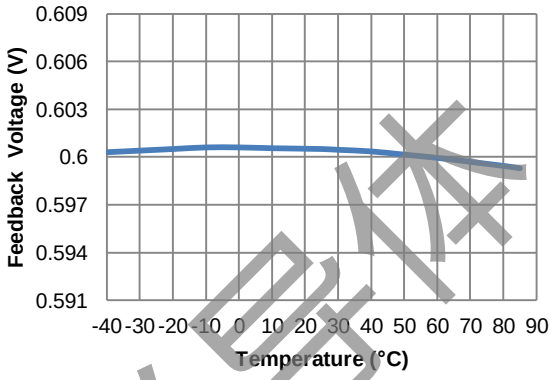


Figure 5. Feedback Voltage vs. Temperature

I_{OUT}=0A

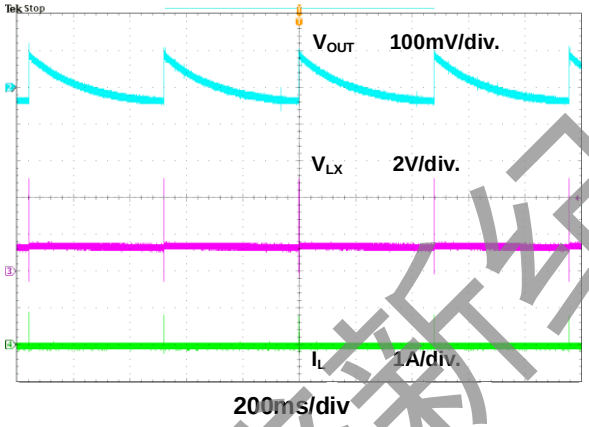


Figure 6. Steady State Waveform

I_{OUT}=3.5A

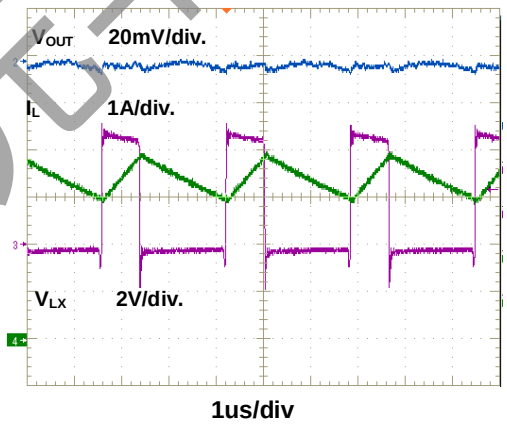


Figure 7. Steady State Waveform

I_{OUT}=0A

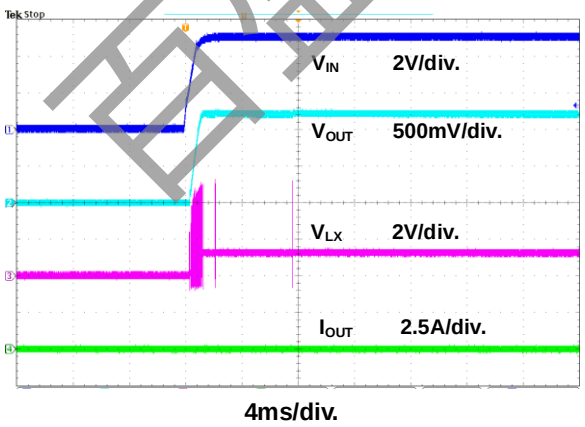


Figure 8. Power On through VIN Waveform

I_{OUT}=3.5A

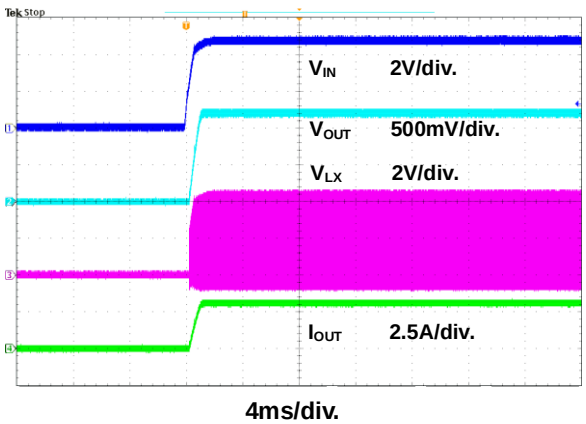


Figure 9. Power On through VIN Waveform

Typical Performance Curves (Continued)

V_{IN}=5V, V_{OUT}=1.2V, C1=10μF, C2=22μFx2, C4=22pF, L1=1.5μH, TA=+25°C, unless otherwise noted.

I_{OUT}=0A

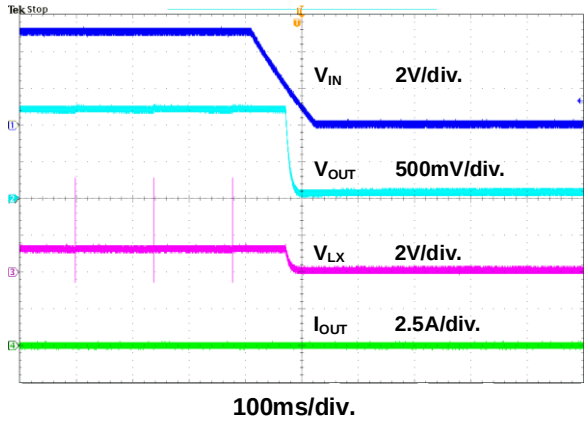


Figure 10. Power Off through VIN Waveform

I_{OUT}=3.5A

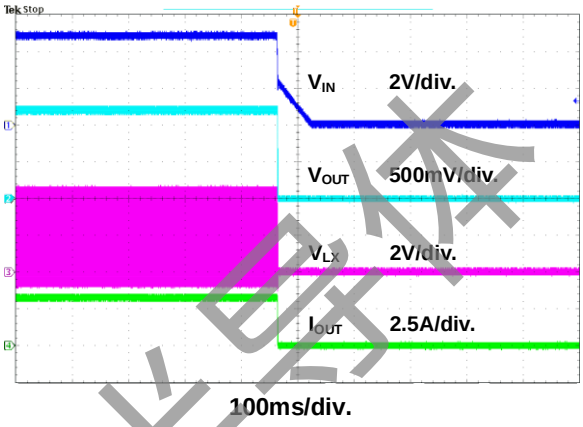


Figure 11. Power Off through VIN Waveform

I_{OUT}=0.5A to 3A

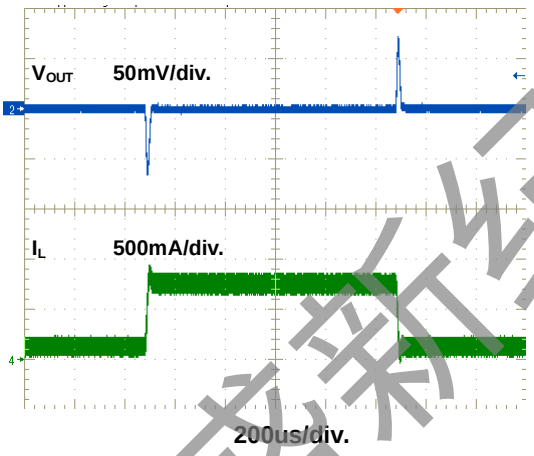


Figure 12. Load Transient Waveform

Function Description

The FP6392 is current mode control step-down synchronous DC/DC converter with a high efficiency, internal compensation. It has integrated high-side (95mΩ, typ) and low-side (75mΩ, typ) switch, and provides 3.5A continuous load current. The input voltage ranges from 2.7V to 6V and the output voltage could be regulated to the lowest 0.6V.

Control Loop

The current mode control with the slope compensation avoids sub-harmonic oscillation during the high duty cycle. The cycle-by-cycle current limit prevents the internal switches from damage in abnormal conditions. During each cycle, the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. With each rising edge of the internal oscillator, the high-side switch will be turned on for a certain time and the inductor current is increased. While the inductor current is higher than the error voltage, the high-side switch will be turned off until the next rising edge of the internal oscillator.

Power Saving Mode

The light load efficiency of buck converter is dominated by switching loss including the loss of gate driver circuit and internal switches. Therefore, intuitive approach of improve the efficiency at light load is reducing the switching frequency.

The FP6392 will automatically enter power saving mode (PSM) from PWM at light load. In PSM, the output voltage is directly compared with internal reference voltage. When the output voltage is larger than the internal reference voltage, the FP6392 will skip the internal clock and high-side switch will not be turned on until the output voltage drops below the internal reference voltage.

However, the minimum on time in PSM and the selected inductor will directly influence the average inductor current. Hence, In FP6392, the PSM to PWM transition happens at 270mA when input voltage is 5V, output voltage is 1.2V, and the inductance is 1.5μH. In this manner, the PSM is effectively optimizing the light load efficiency of buck converter.

Soft Start

The FP6392 employs internal soft start function to reduce input inrush current during start up. The internal soft start time will be 1ms.

Enable

The FP6392 EN pin provides digital control to turn on/off the regulator. When the voltage of EN exceeds the threshold voltage, the regulator will start the soft start function. If the EN pin voltage is below the shutdown threshold voltage, the regulator will turn into the shutdown mode and the shutdown current will be smaller than 1μA. For auto start-up operation, connect EN to VIN.

Under Voltage Lockout

When the FP6392 is power on, the internal circuits will be held inactive until V_{IN} voltage exceeds the UVLO threshold voltage. And the regulator will be disabled when V_{IN} is below the UVLO threshold voltage. The hysteretic of the UVLO comparator is 200mV (typ).

Over Current Protection

The FP6392 over current protection function is implemented by using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side MOSFET series sense resistor voltage. When the load current increases, the inductor current will also increase. When the peak inductor current reaches the current limit threshold, the output voltage will start to drop. When the over current condition is removed, the output voltage will return to the regulated value.

Short Circuit Protection

The FP6392 provides short circuit protection function to prevent the device damaged from short condition. When the short condition occurs and the feedback voltage drops lower than 50% of the regulation level, this will activate the latch protection circuit. Then output will be forced shutdown to prevent the inductor current runaway and to reduce the power dissipation within the IC under true short circuit conditions. Once the short condition is removed, reset EN or VIN to restart IC.

Over Temperature Protection

The FP6392 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 30°C (typ).

Application Information

PG Signal Output (PG)

PG pin is an open-drain output and requires a pull up resistor. PG is actively held low in soft-start, standby and shutdown. It will be released when the output voltage rises above 90% of nominal regulation point.

Output Voltage Setting

The output voltage V_{OUT} is set by using a resistive divider from the output to FB. The FB pin regulated voltage is 0.6V. Thus the output voltage is:

$$V_{OUT}=0.6V\times\left(1+\frac{R1}{R2}\right)$$

Table 2 lists recommended values of R1 and R2 for most used output voltage.

Table 2 Recommended Resistance Values

V_{OUT}	R1	R2
3.3V	453kΩ	100kΩ
2.5V	316kΩ	100kΩ
1.8V	200kΩ	100kΩ
1.5V	150kΩ	100kΩ
1.2V	100kΩ	100kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

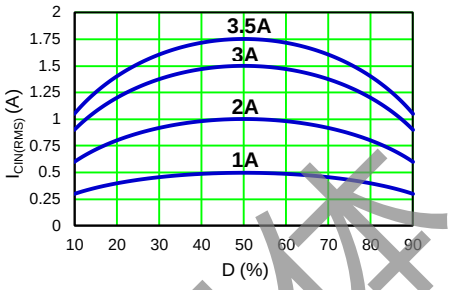
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{CIN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)}$$

$$D=\frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice.

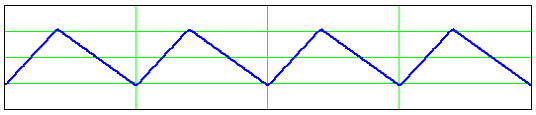
Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t)=V_{RIPPLE(C)}(t)+V_{RIPPLE(ESR)}(t)+V_{RIPPLE(ESL)}(t)+V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.

$V_{RIPPLE(ESR)}(t)$



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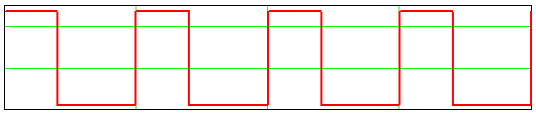
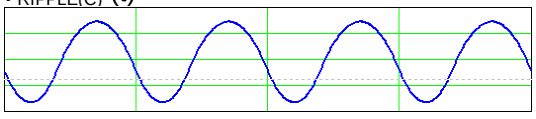
$V_{RIPPLE(ESL)}(t)$



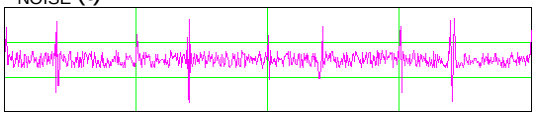
+

$V_{RIPPLE(C)}(t)$



+

$V_{NOISE}(t)$



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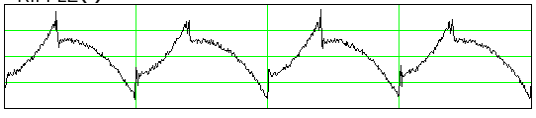
$V_{RIPPLE}(t)$



(t)

Application Information (Continued)

$$V_{RIPPLE(ESR)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR$$

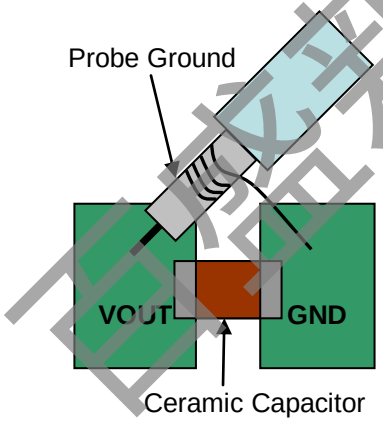
$$V_{RIPPLE(ESL)}=\frac{ESL}{L}\times V_{IN}$$

$$V_{RIPPLE(C)}=\frac{V_{OUT}}{8\times F_{OSC^2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirements. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Remove the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminates noise.



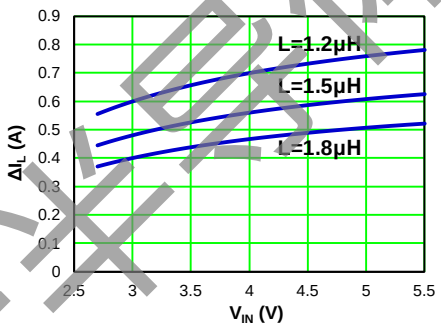
Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode.

That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to-peak ripple current:

$$\Delta I_L=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The following diagram is an example to graphically represent ΔI_L equation.



V_{OUT}=1.2V, F_{OSC}=1MHz

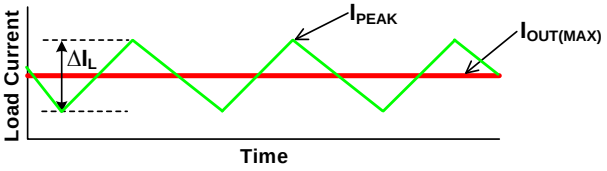
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L=0.3\times I_{OUT(MAX)}$$

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times F_{OSC}\times\Delta I_L}$$

To guarantee sufficient output current, peak inductor current must be lower than the FP6392 high-side MOSFET current limit. The peak inductor current is shown as below:

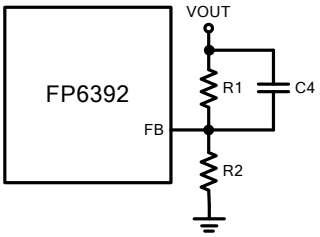
$$I_{PEAK}=I_{OUT(MAX)}+\frac{\Delta I_L}{2}$$



Application Information (Continued)

Feedforward Capacitor Selection

Internal compensation function allows users saving time in design and saving cost by reducing the number of external components. The use of a feedforward capacitor C4 in the feedback network is recommended to improve transient response or higher phase margin.



For optimizing the feedforward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feedforward capacitor identified, the value of feedforward capacitor C4 can be calculated with the following equation:

$$C4=\frac{1}{2\pi\times F_{CROSS}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feedforward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and causes more ringing. In the other hand, if more phase margin is desired, the feedforward capacitor value can be decreased to push the cross frequency to lower region. In general, the feedforward capacitor range is between 10pF to 330pF.

PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.

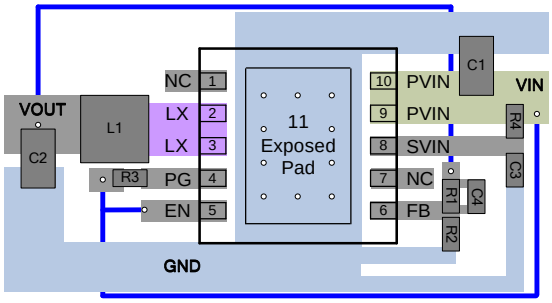
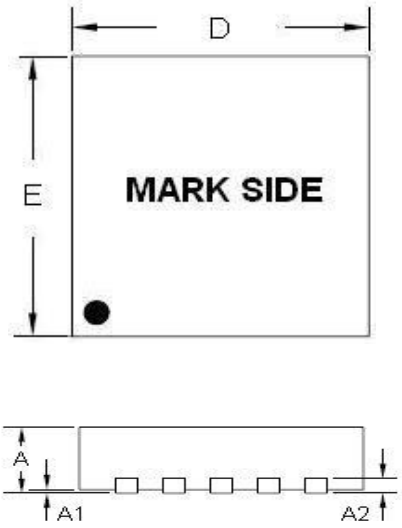
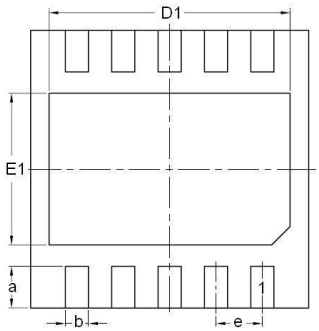


Figure 13. Recommended Layout Diagram

Outline Information

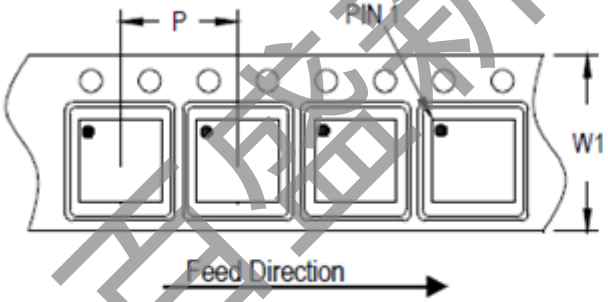
TDFN-10 (3mm x 3mm) Package (Unit: mm)

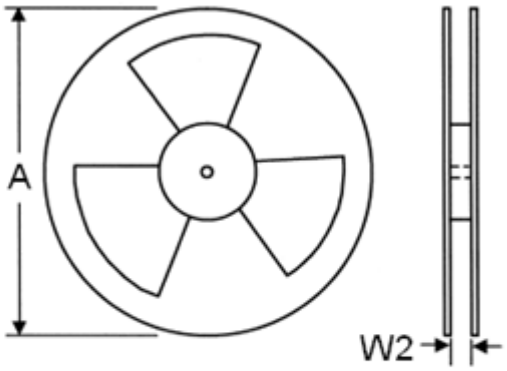




SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A2	0.18	0.25
D	2.95	3.05
E	2.95	3.05
a	0.30	0.50
b	0.18	0.30
e	0.45	0.55
D1	2.20	2.70
E1	1.40	1.75

Carrier Dimensions





Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000