

## NCE N-Channel Enhancement Mode Power MOSFET

### Description

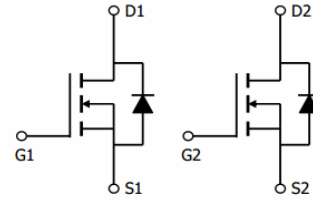
The NCE30ND35Q uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

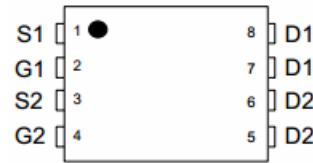
- $V_{DS} = 30V, I_D = 35A$   
 $R_{DS(ON)} < 13m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 19m\Omega @ V_{GS} = 4.5V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

### Application

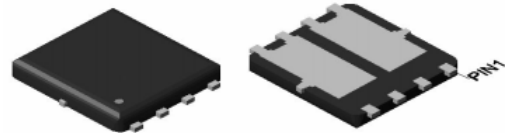
- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic Diagram



pin assignment



Top View

Bottom View

**100% UIS TESTED!**  
**100% ΔVds TESTED!**

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE30ND35Q	NCE30ND35Q	DFN3.3X3.3-8L	-	-	-

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	35	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	24.8	A
Pulsed Drain Current	$I_{DM}$	140	A
Maximum Power Dissipation	$P_D$	30	W
Derating factor		0.24	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	72	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	4.17	$^\circ C/W$
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## Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)

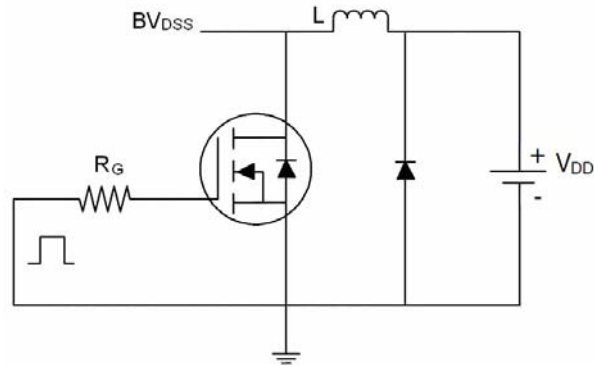
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.9	1.3	2.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	11	13	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	14.5	19	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	26	-	-	S
<b>Dynamic Characteristics</b> (Note4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, F=1.0MHz	-	1000	-	PF
Output Capacitance	C <sub>oss</sub>		-	180.8	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	164.4	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =15V, R <sub>L</sub> =0.75Ω V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω	-	5	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	12	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	19	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	6	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	17	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.8	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	3.9	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	35	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> =20A di/dt = 100A/μs (Note3)	-	19	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	10	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

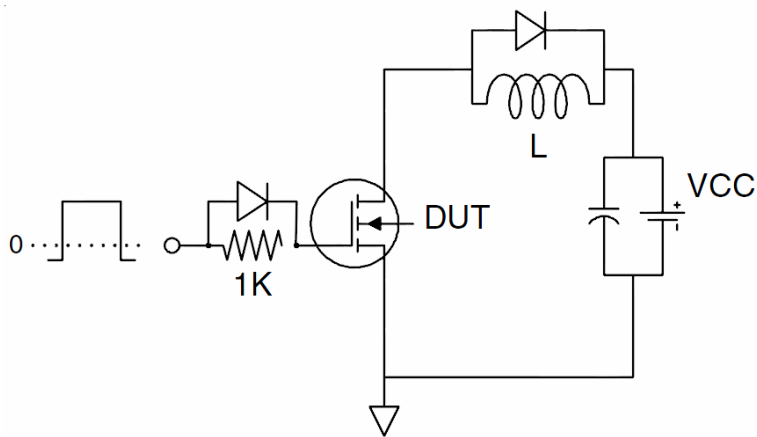
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=15V, V<sub>G</sub>=10V, L=0.5mH, R<sub>G</sub>=25Ω

## Test circuit

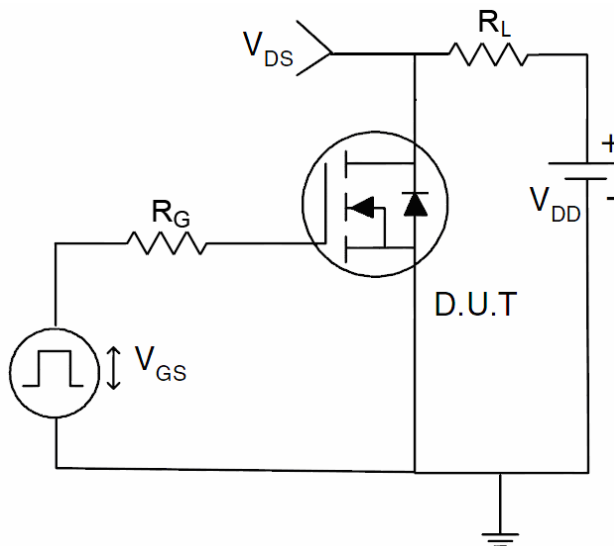
### 1) $E_{AS}$ test Circuits



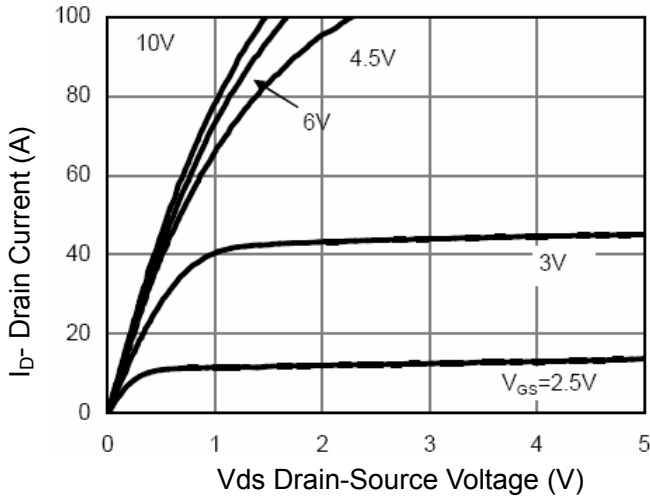
### 2) Gate charge test Circuit:



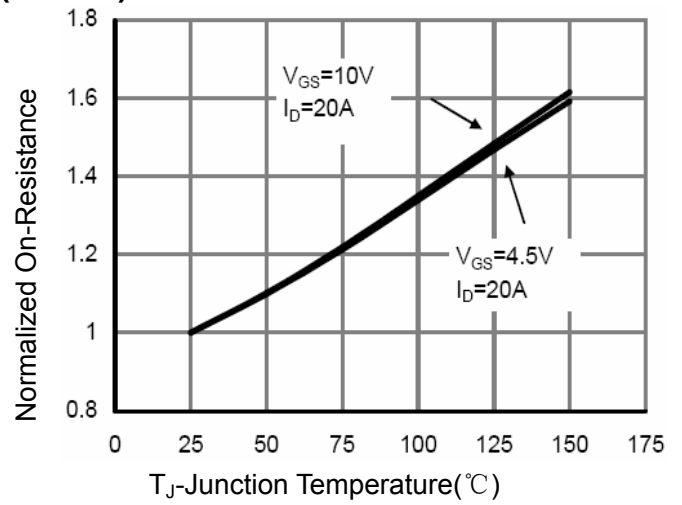
### 3) Switch Time Test Circuit:



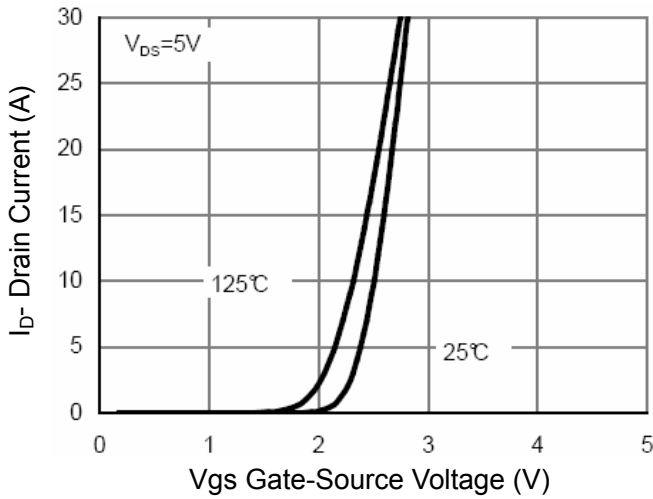
**Typical Electrical and Thermal Characteristics (Curves)**



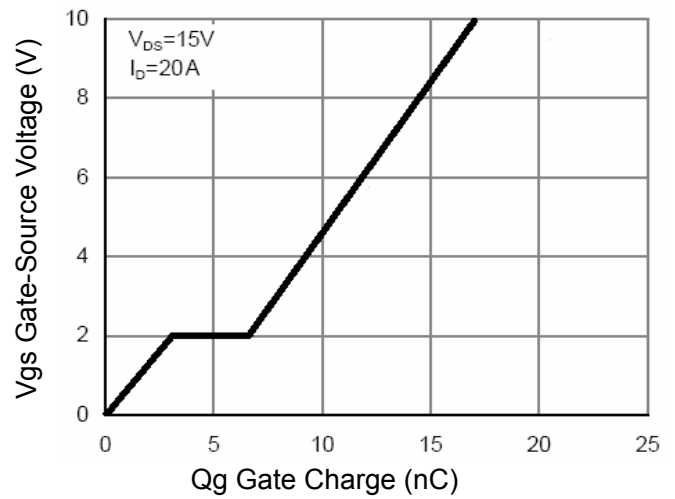
**Figure 1 Output Characteristics**



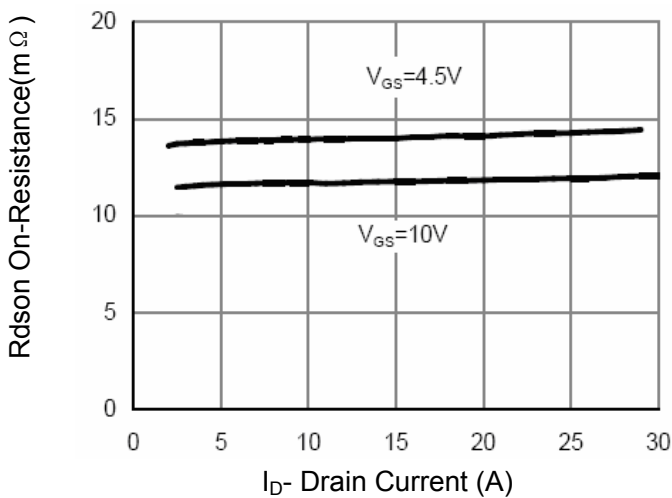
**Figure 4 Rdson-Junction Temperature**



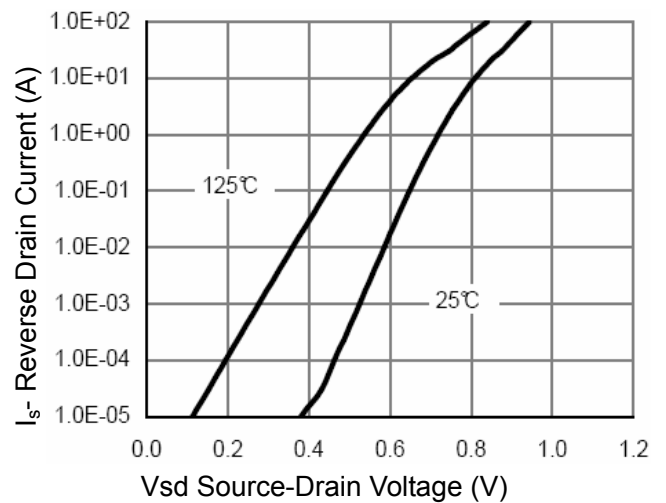
**Figure 2 Transfer Characteristics**



**Figure 5 Gate Charge**



**Figure 3 Rdson- Drain Current**



**Figure 6 Source- Drain Diode Forward**

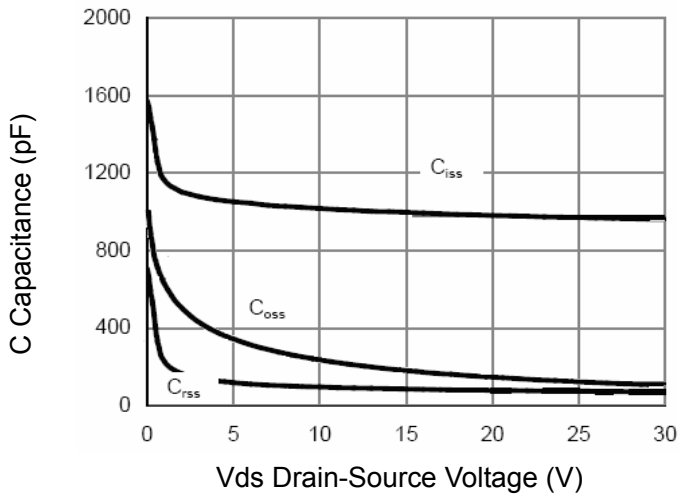


Figure 7 Capacitance vs Vds

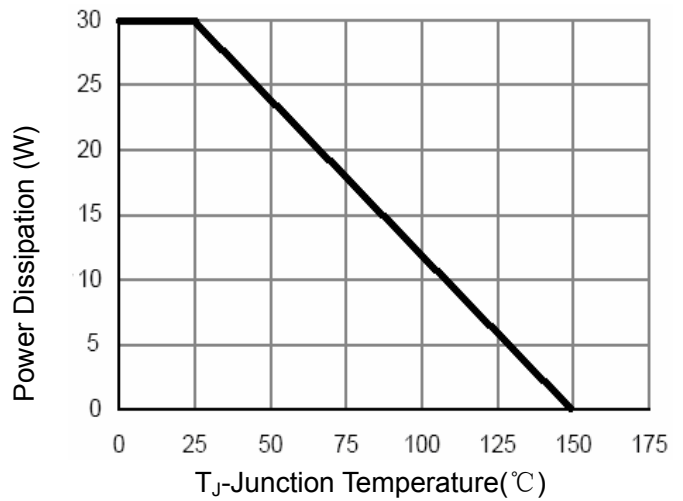


Figure 9 Power De-rating

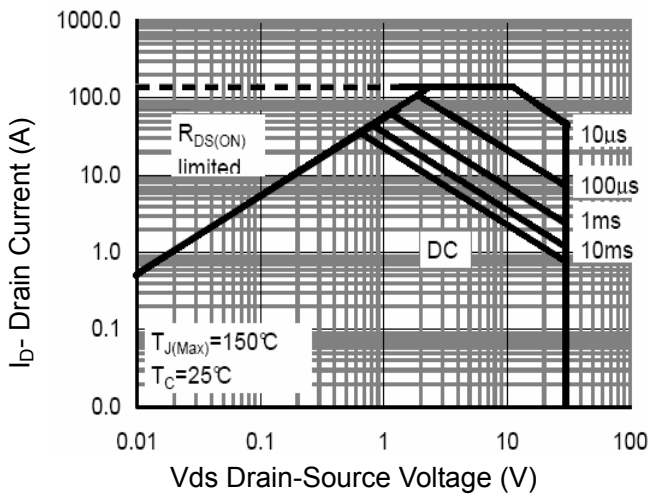


Figure 8 Safe Operation Area

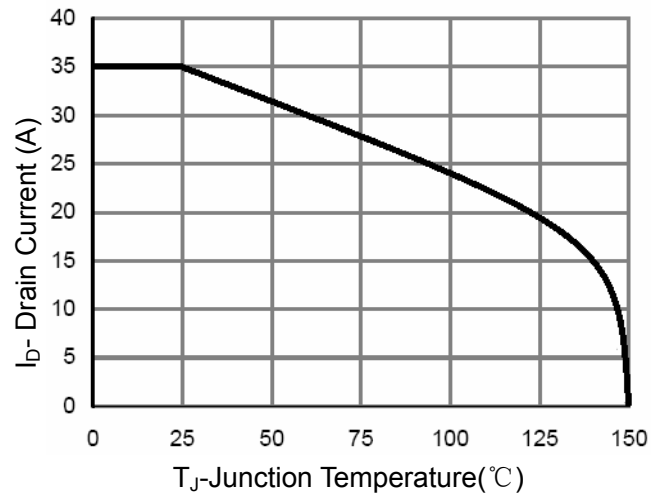


Figure 10  $I_D$  Current De-rating

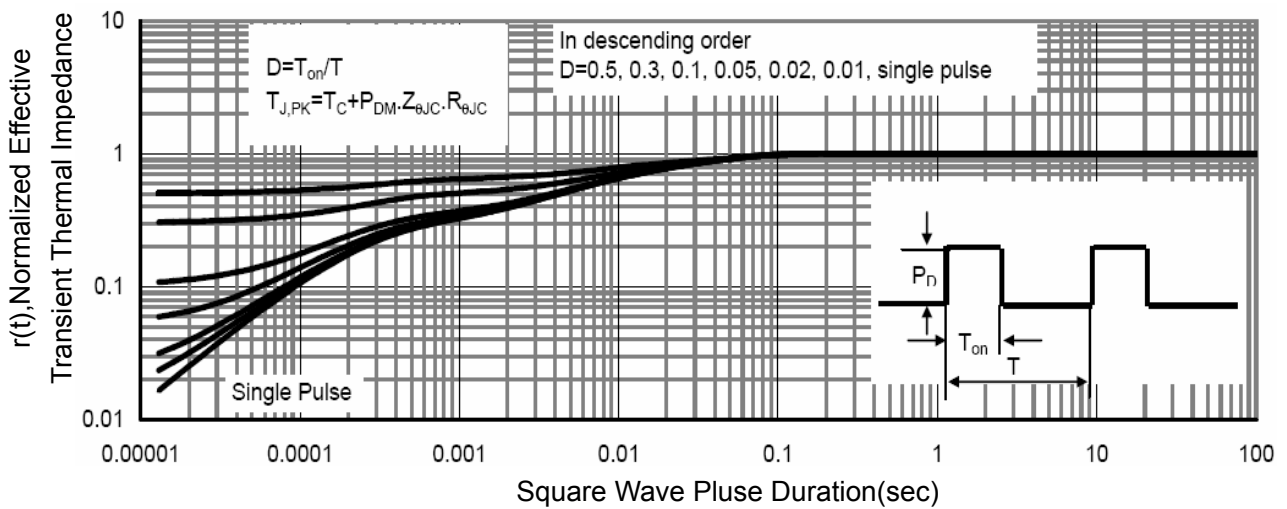
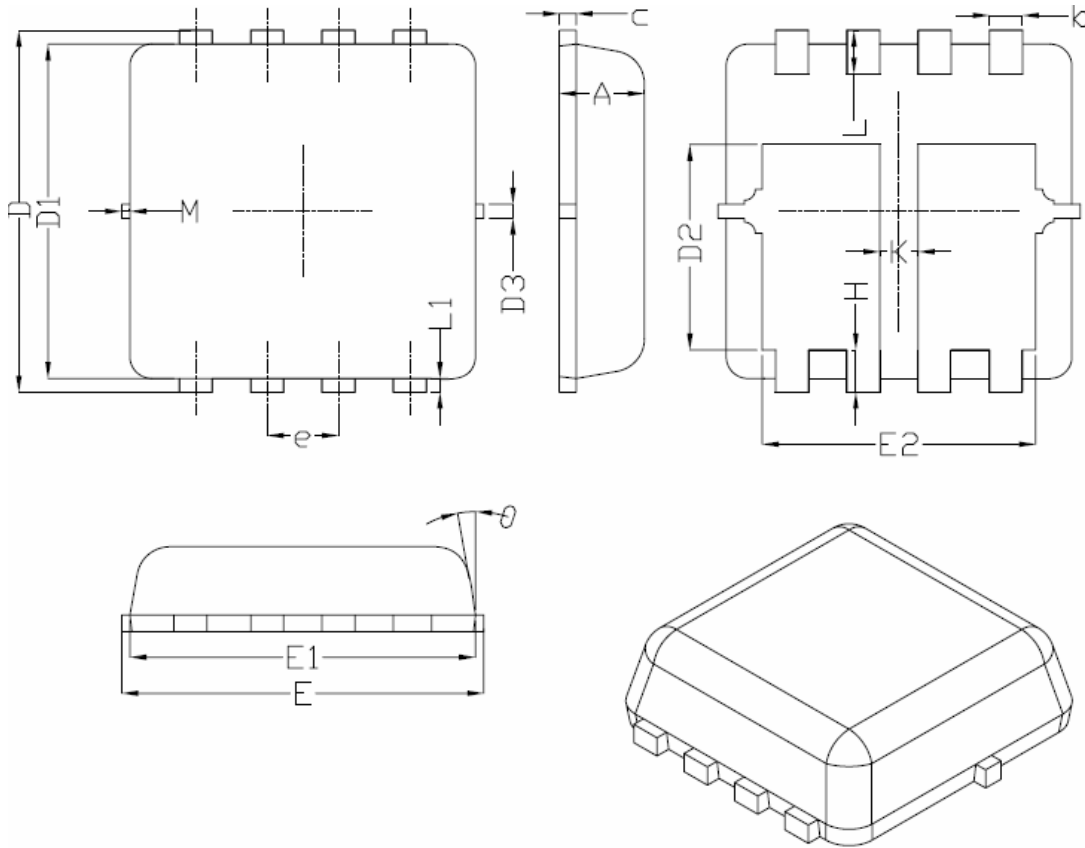


Figure 11 Normalized Maximum Transient Thermal Impedance

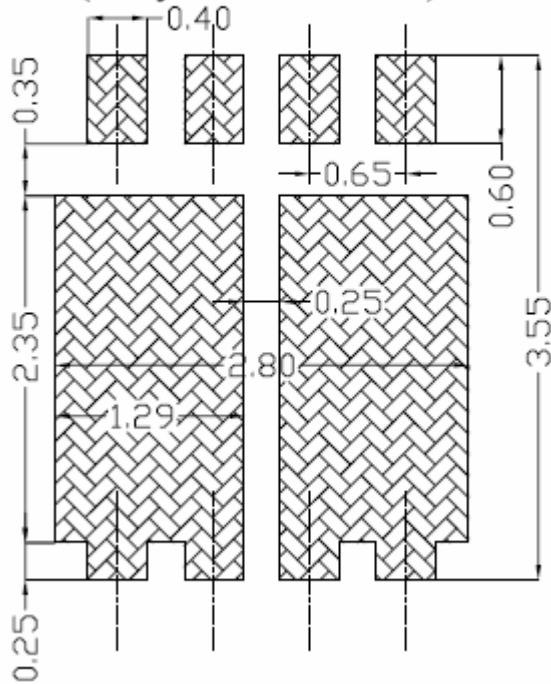
## DFN3.3X3.3-8L Package Information



### Land Pattern (Only for Reference)

SYMBOL	DIMENSIONAL REOMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
K	0.30	---	---
θ	---	10°	12°
M	*	*	0.15

\* Not specified



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